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Energy-efficiency and Performance Innovation of Chips with 2-Dimensional Materials (EPIC 2-D Materials) and Applications

Jeongwon Park, PhD., P.Eng., SMIEEE
Associate Professor,
Department of Electrical and Biomedical Engineering,
University of Nevada, Reno, NV 89557, USA
E-mail: jepark@unr.edu

Date and Time: Thursday, August 22, 2024
Noon-1 PM: Seminar

Department of Electrical & Biomedical Engineering Associate Professor Jeongwon Park's research in the Davidson Foundation ISO Class 5 (Class 100) Cleanroom ranges from biomedicine to advanced manufacturing. Supported by a mechanical room with 10 independent air and water systems, the cleanroom is a carefully calibrated and maintained laboratory that reduces air contaminants from an average of between 500,000 and 1,000,000 parts per cubic foot in ordinary indoor spaces down to 100.

https://www.unr.edu/engineering/about/news/magazine/2020/wpeb

Energy-efficiency and Performance Innovation of Chips with 2-Dimensional Materials (EPIC 2-D Materials) and Applications

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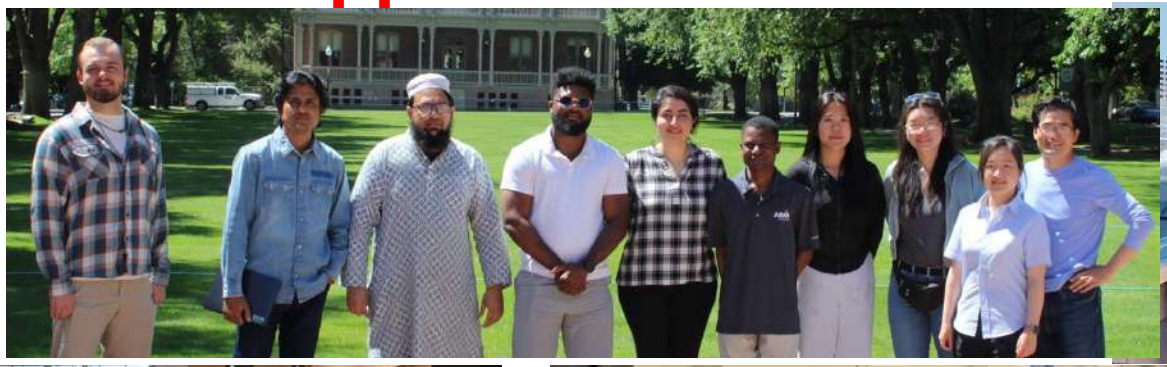
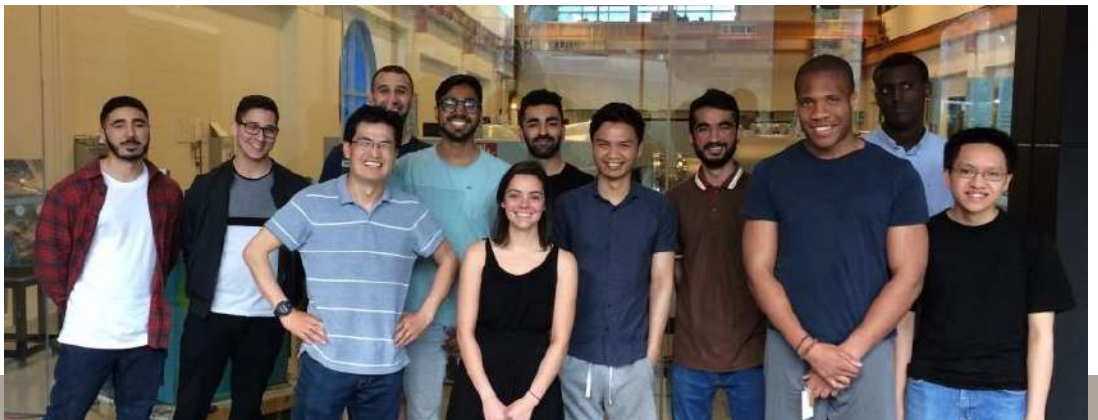
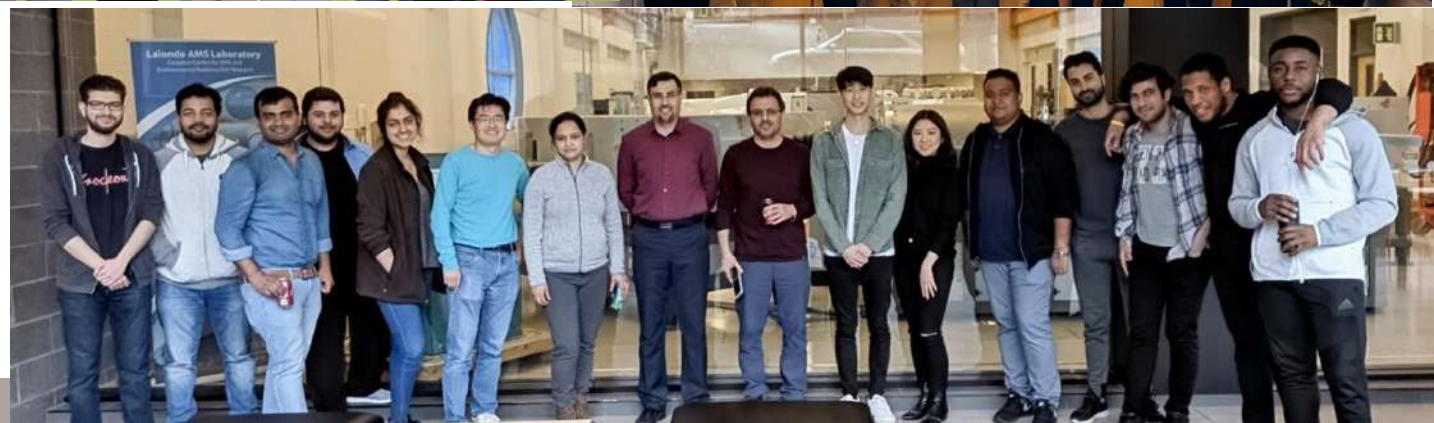
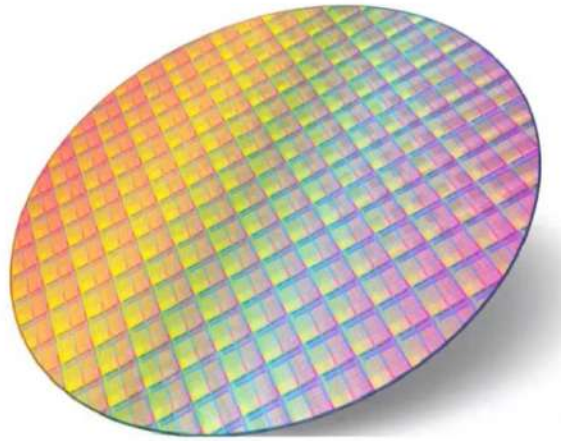






Agenda

- Introduction
- Semiconductor R&D Trends
- Transistor Scaling
- 2D Materials and Devices
- Negative Capacitance FETs
- Brief Introduction of Other Research Areas in My Group
  - Wide-Bandgap Semiconductors
  - Wireless Power Transfer
  - Brain-Computer Interface
- Challenges and Prospects

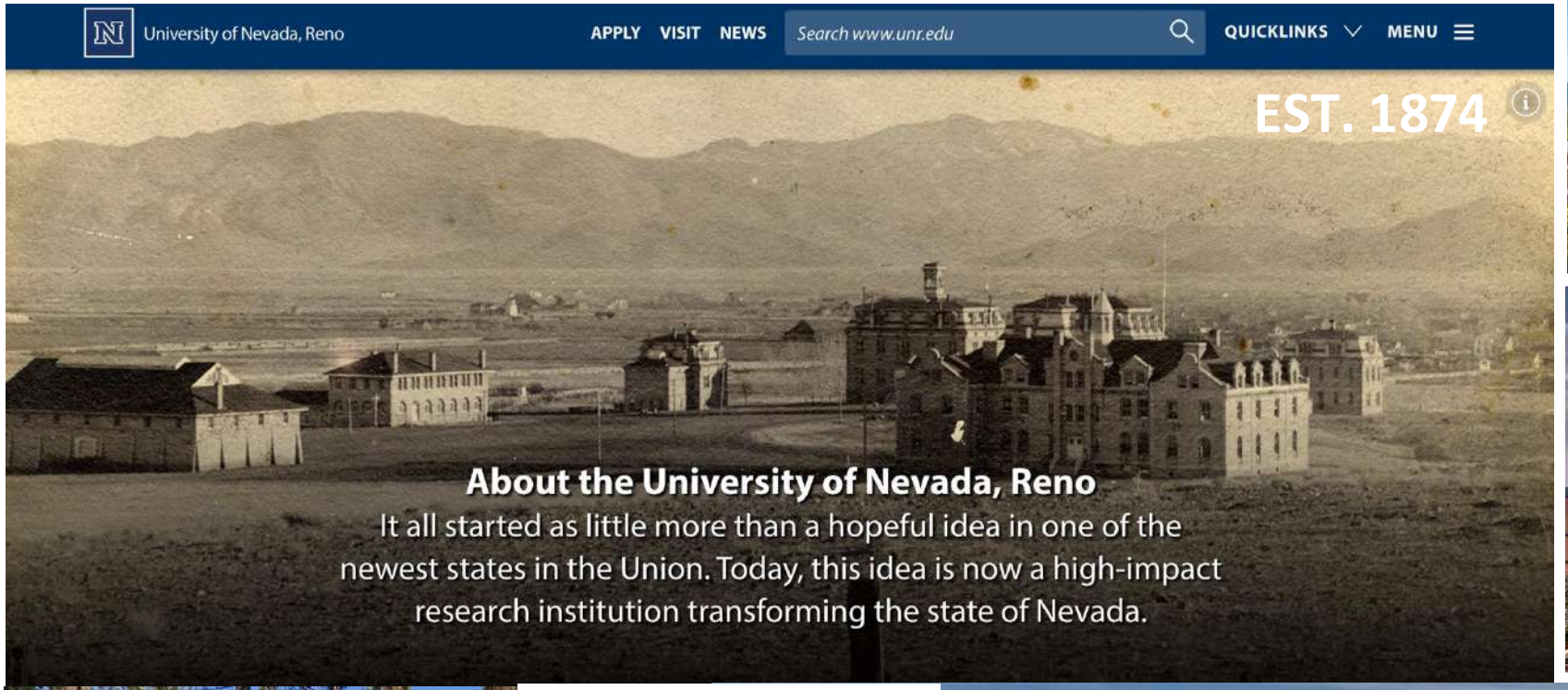



Medford
Redding
NEVADA
Reno
Sacramento
Yosemite National Park
Go-to destination for
outdoor activities
San Francisco
San Jose
Fresno
Death Valley
National Park
CALIFORNIA
Las Vegas
Bakersfield
Los Angeles
Anaheim
Long Beach
San Diego
Mexicali
Tijuana
Google
Satellite


Lake Tahoe


Yosemite national park

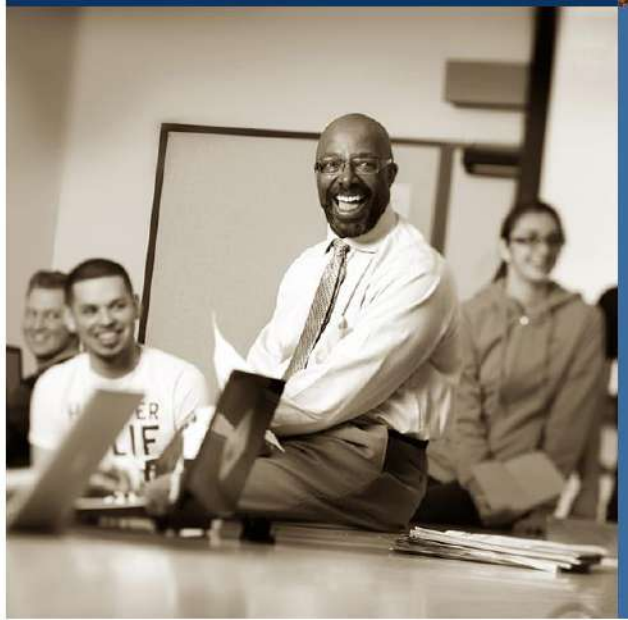
University of Nevada, Reno (UNR)



University of Nevada, Reno
AT LAKE TAHOE

Founded in 1874

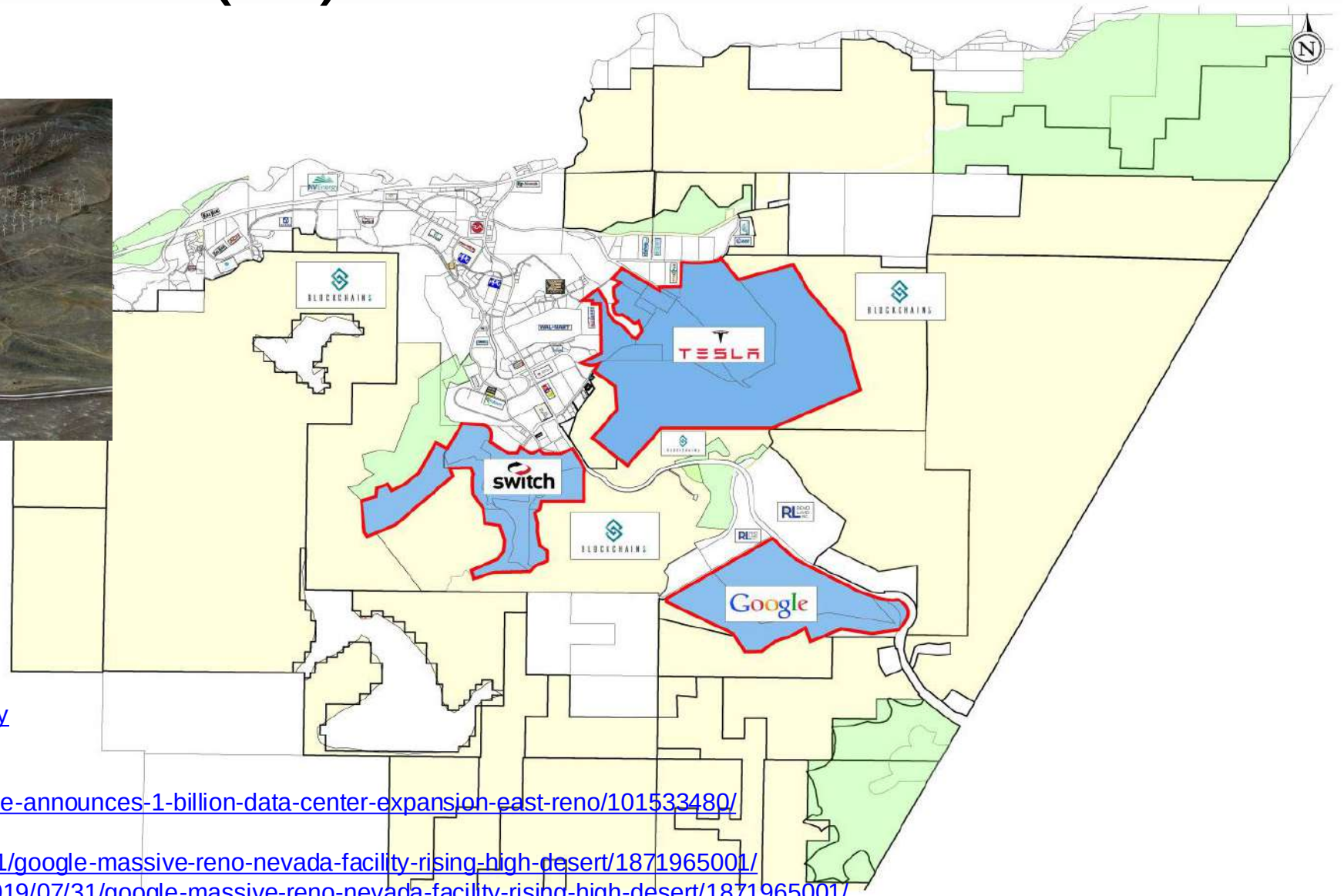
21,000+ students



1,049 academic faculty

19:1 student-to-faculty ratio

Tahoe Reno Industrial Center (TRI)



- TESLA Gigafactory: https://www.tesla.com/gigafactory
- Apple data center:
- https://www.datacenters.com/apple-inc-reno
- https://www.usatoday.com/story/tech/2017/05/10/apple-announces-1-billion-data-center-expansion-east-reno/101533480/
- Google data center
- https://www.rgj.com/story/money/business/2019/07/31/google-massive-reno-nevada-facility-rising-high-desert/1871965001/
- NCAR : https://www.rgj.com/story/money/business/2019/07/31/google-massive-reno-nevada-facility-rising-high-desert/1871965001/

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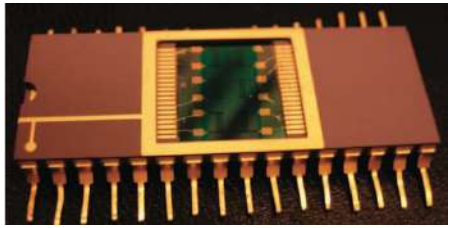
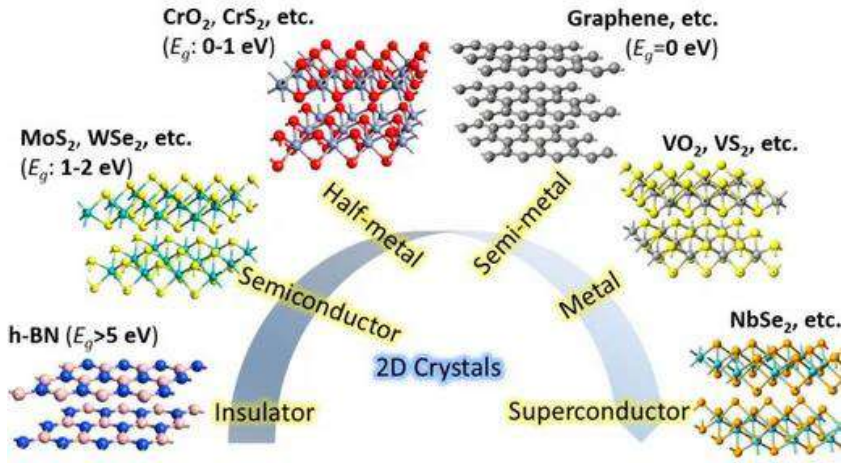
Cell: 1 (775) 225-6726

University of Nevada, Reno

Research Areas:
Materials, Sensors and Devices

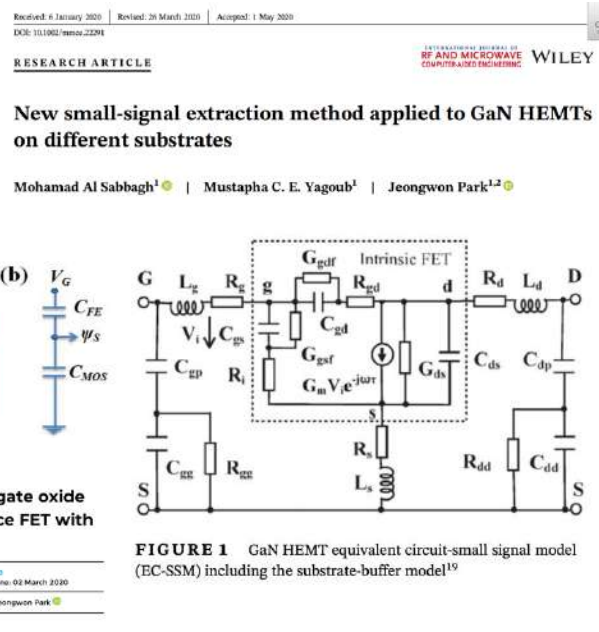


Novel Materials



Personal care

Medical applications



RESEARCH ARTICLE

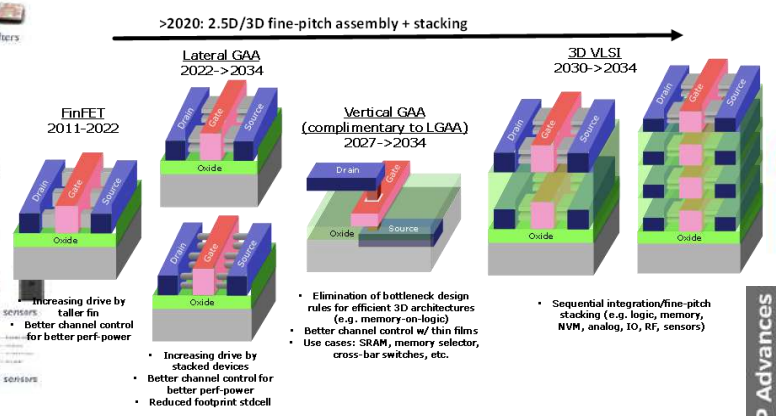
RF AND MICROWAVE COMPUTER-AIDED ENGINEERING WILEY

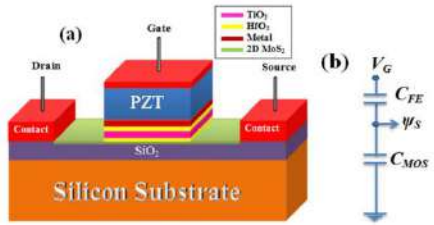
New small-signal extraction method applied to GaN HEMTs on different substrates

Mohamad Al Sabbagh[1] | Mustapha C. E. Yagoub[1] | Jeongwon Park[1,2]

FIGURE 1 GaN HEMT equivalent circuit-small signal model (EC-SSM) including the substrate-buffer model[19]

Novel Devices





AIP Advances

$HfO_2/TiO_2/HfO_2$ tri-layer high-K gate oxide based MoS_2 negative capacitance FET with steep subthreshold swing

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ELECTRICAL & BIOMEDICA ENGINEERING

Associate Professor Jeongwon Park

Research Areas:

- Semiconductors and nanofabrications
- IoT sensors and sensor networks
- Quantum information and science (QIS)
- Nano-scale 2-D materials, nanowires, and quantum dots
- Biomedical devices (wearable, deep brain stimulation, etc.)

Research Achievements and Impact:

- Funded research grants from governments and industry (over $10M)
- H-index of 26, and cited more than 5300 times
- Senior Member of IEEE, Professional Engineer
- 6 US patents and 94 peer-reviewed papers in high-impact journals
- Contributed to high-impact research projects in nanotechnology at the University of Nevada Reno, University of Ottawa, SLAC National Accelerator Laboratory, Stanford University, Lawrence Berkeley National Laboratory, University of California, San Diego, and Applied Materials, Inc.

Jeongwon Park, Ph.D. P.Eng.

Ph.D., University of California, San Diego, 2008
Topics: semiconductors, nanoelectronics, sensors, and nanotechnology

E-mail: jepark@unr.edu

What is Exascale and Why Zettascale

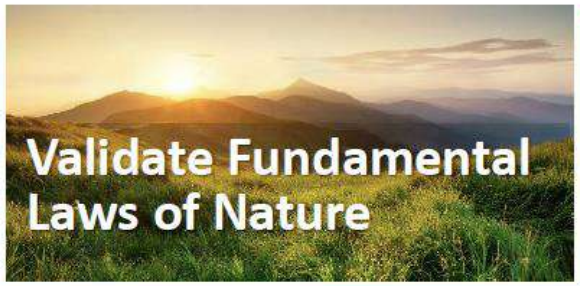
Performance (FP64-tensor)
> 1 Exaflop

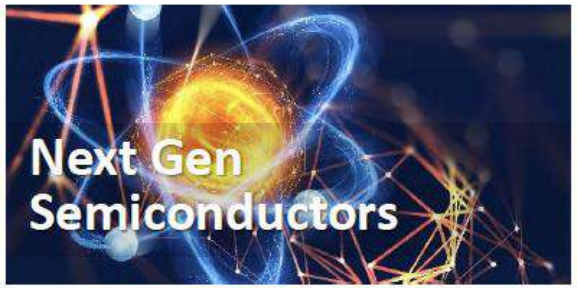
Performance (FP32 -tensor)
> 1 Exaflop

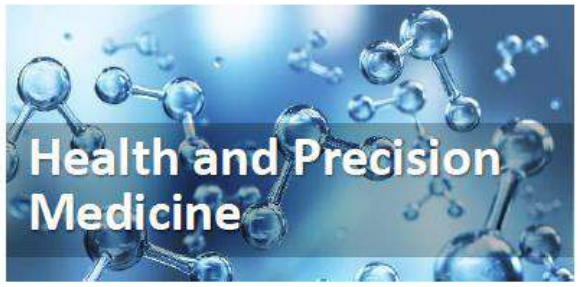
Peak Performance (BF16/Int8 -tensor)
> 8-16 Exaflop

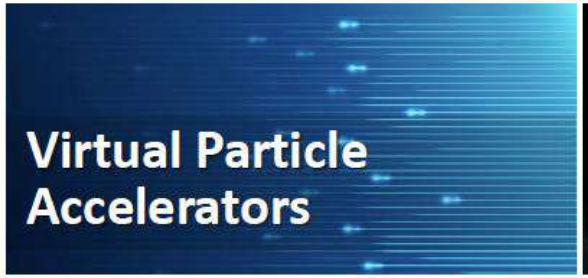
Power
20-30 MW/Exaflop

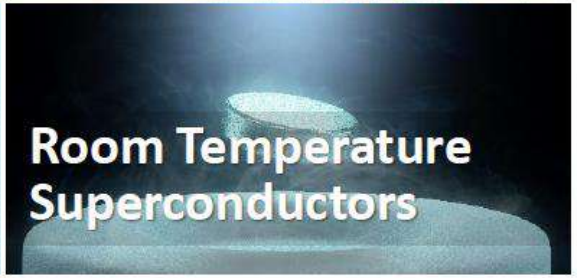
Goal: Solve fundamental problems from first principles

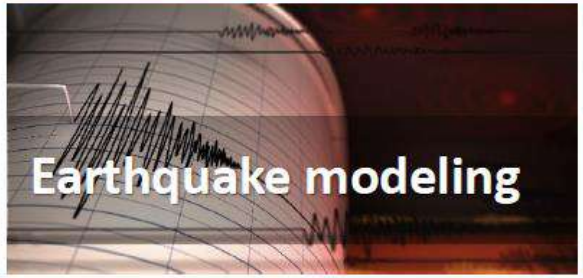






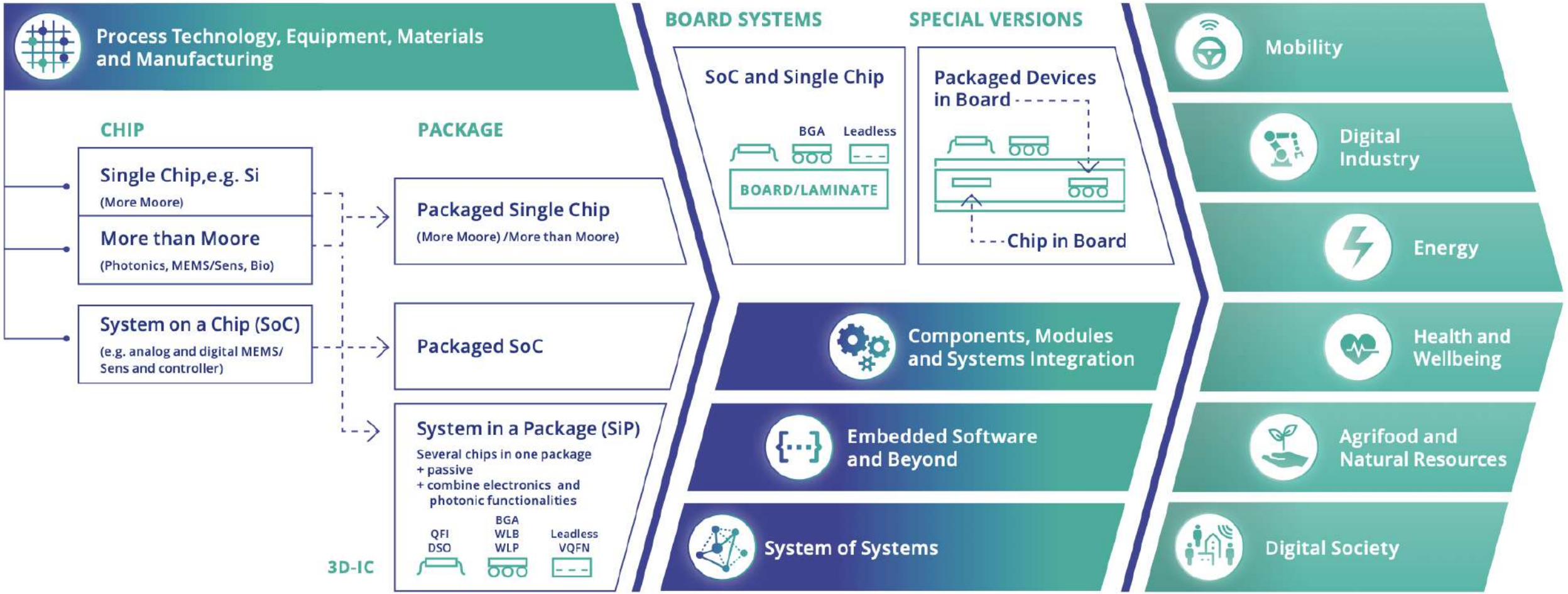






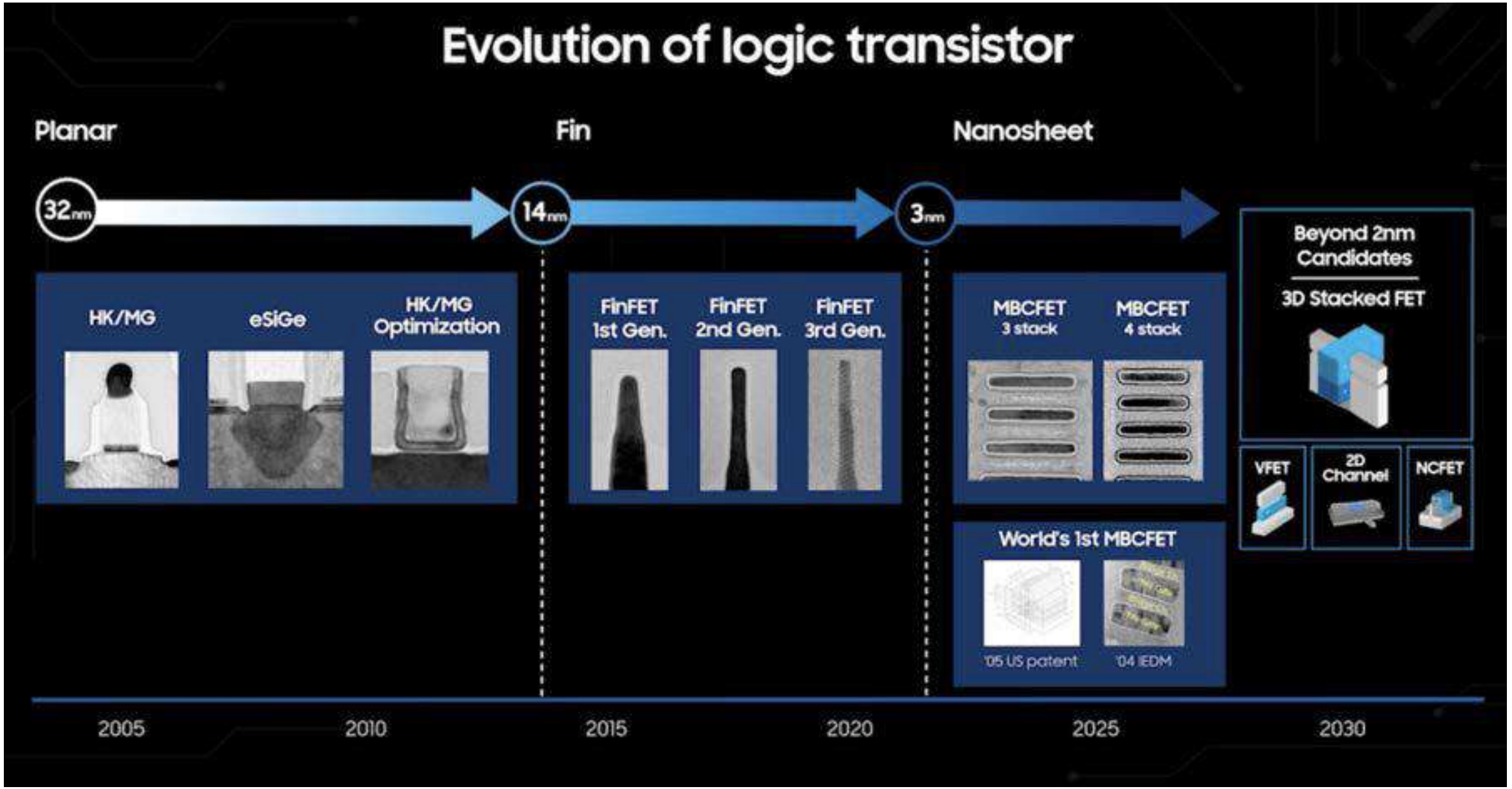
Zettascale technologies will make Exascale mainstream

Ecosystem of semiconductors



Materials to Systems in Semiconductor Manufacturing and Beyond

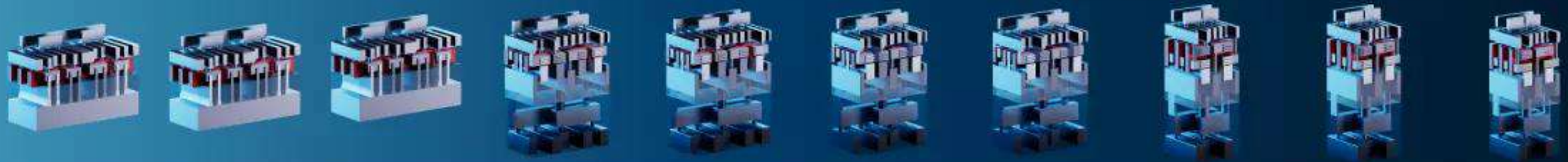
Transistor 2003-2025 evolution: From 2D Equivalent scaling to 3D Power scaling



Source: Intel investor meeting 2022

Potential logic scaling roadmap extension

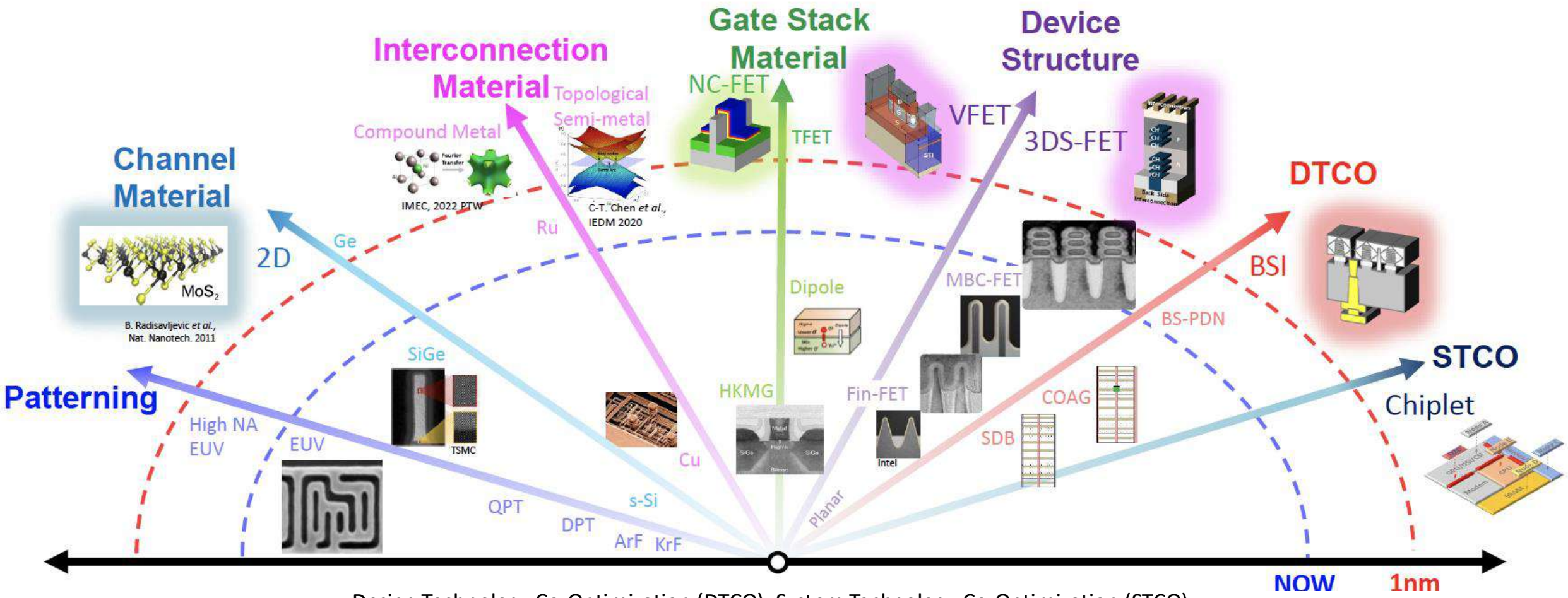
	2018	2020	2022	2024	2026	2028	2030	2032	2034	2036
	N7	N5	N3	N2	A14	A10	A7	A5	A3	A2
Metal Pitch (nm)	40	28	21	21	18	18	16	16	16	16-12
							Continued dimensional scaling			
Metal Tracks	6	6	6	6	5	5	5	4	<4T	<4T
	finFET	finFET	finFET	GAA NSFET	GAA NSFET	FSFET	FSFET	CFET	CFET	CFET atomic
							Device and material innovations			
										Context-aware interconnect



imec https://www.tomshardware.com/news/imec-reveals-sub-1nm-transistor-roadmap-3d-stacked-cmos-20-plans ITF WORLD

Candidates for Energy Efficient CMOS Devices

" Innovations in structures, materials & processes to shrink standard cell area without decreasing effective device width & minimum metal width "



Design Technology Co-Optimization (DTCO), System Technology Co-Optimization (STCO)

Agenda

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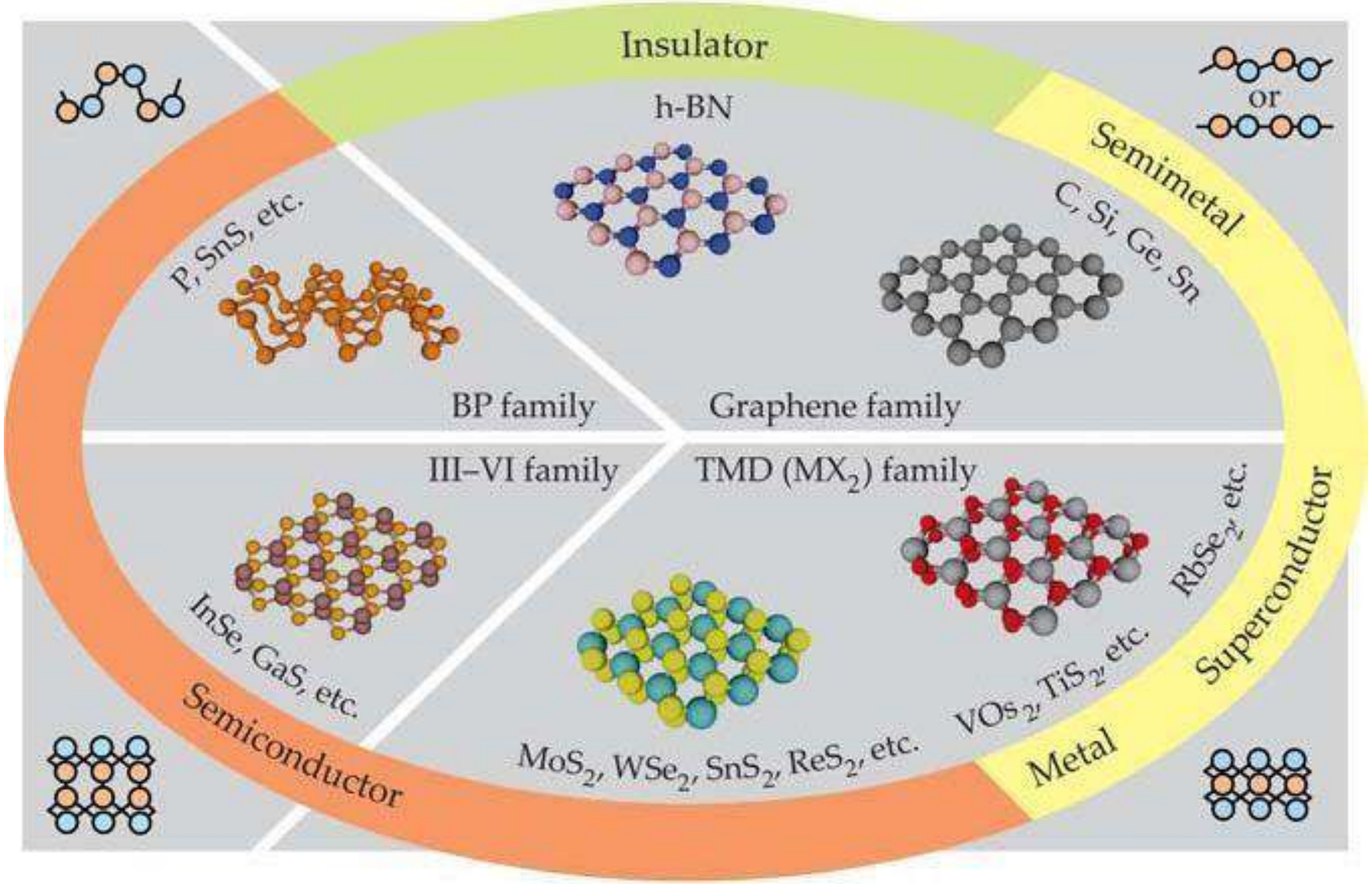
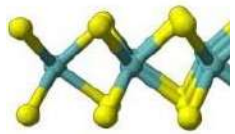
  - Wireless Power Transfer
  - Brain-Computer Interface
- Challenges and Prospects

Introducing 2D materials



Ajayan, Kim, Banerjee - Physics Today (2016)

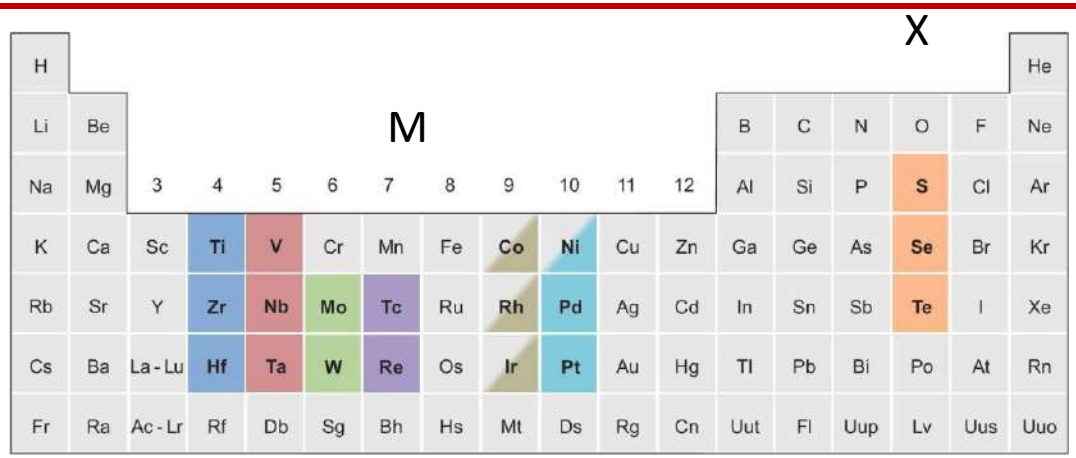


Introducing Transition Metal Dichalcogenides

- MX_2 with M = Mo, W, Re,…
  X = S, Se, Te
- Well documented in the bulk

Wilson and Yoffe Adv. Phys. 1969

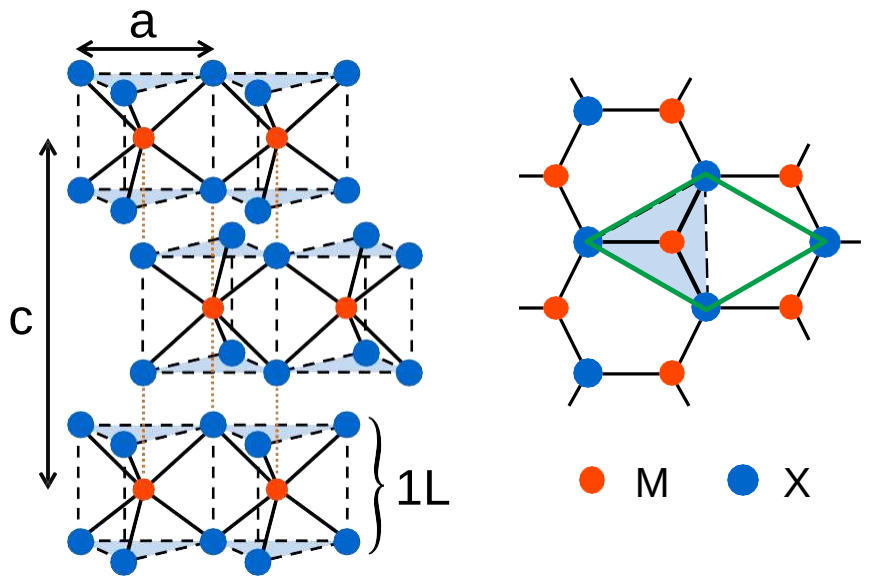
•In this talk:
Semiconducting MX_2 only



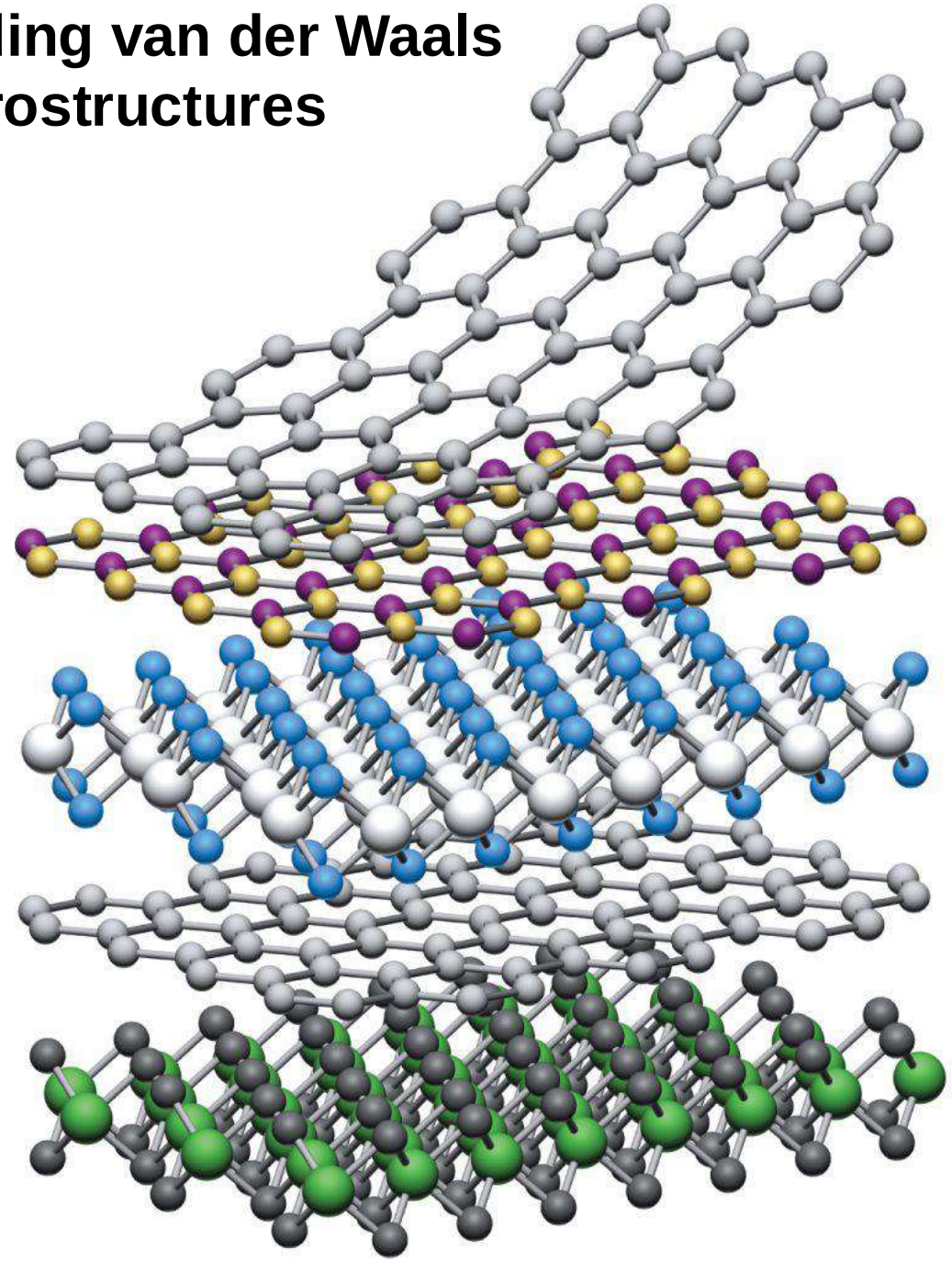
M. Chhowalla *et al.,* Nat. Chem. **5**, 263 (2013)

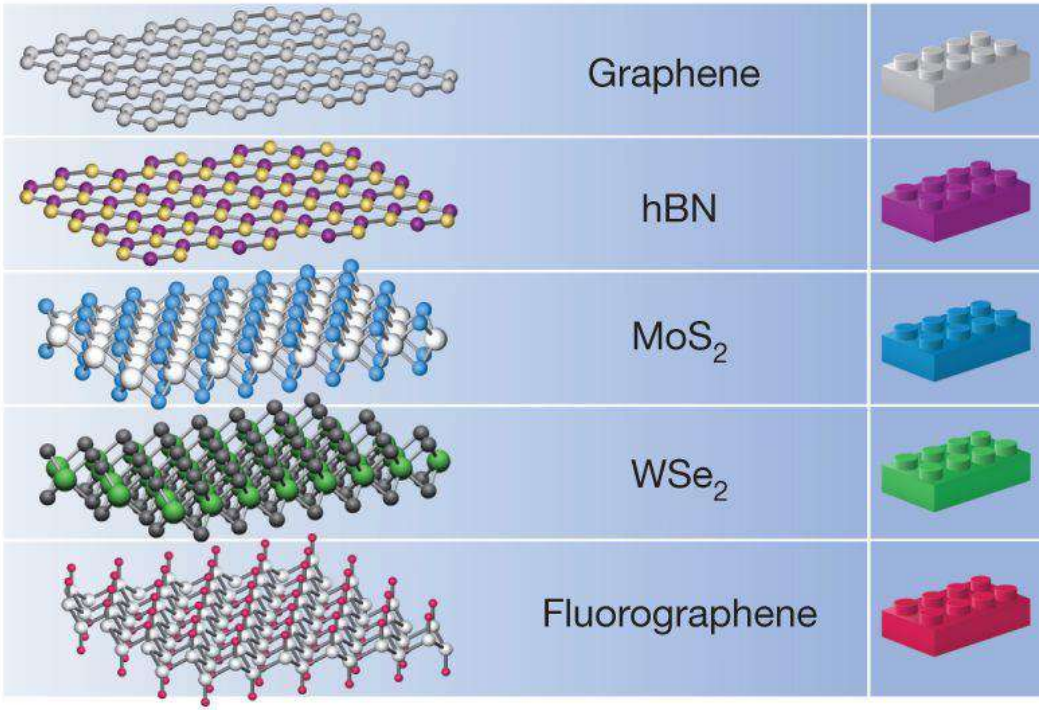
- Trigonal prismatic phase
- 2*Hc*-MX_2 (AbA,BaB stacking)

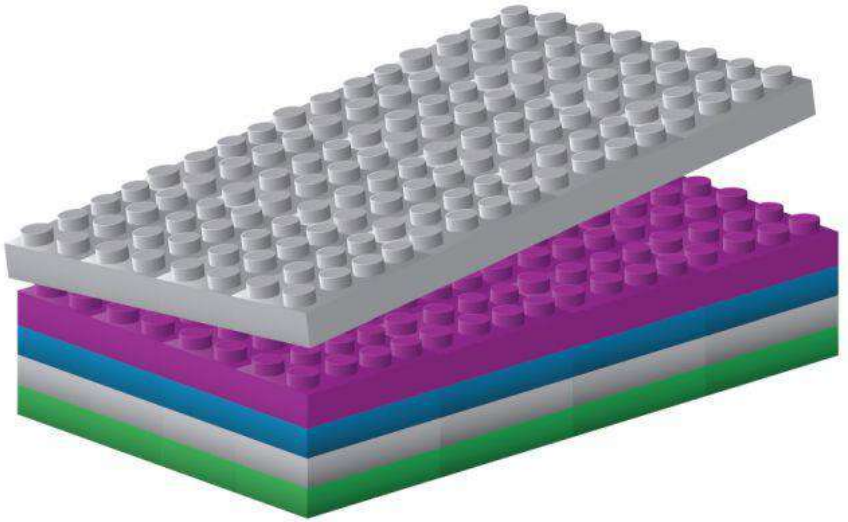
→ MoS_2, $MoSe_2$, WS_2, WSe_2, $MoTe_2$

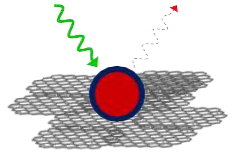


Building van der Waals heterostructures

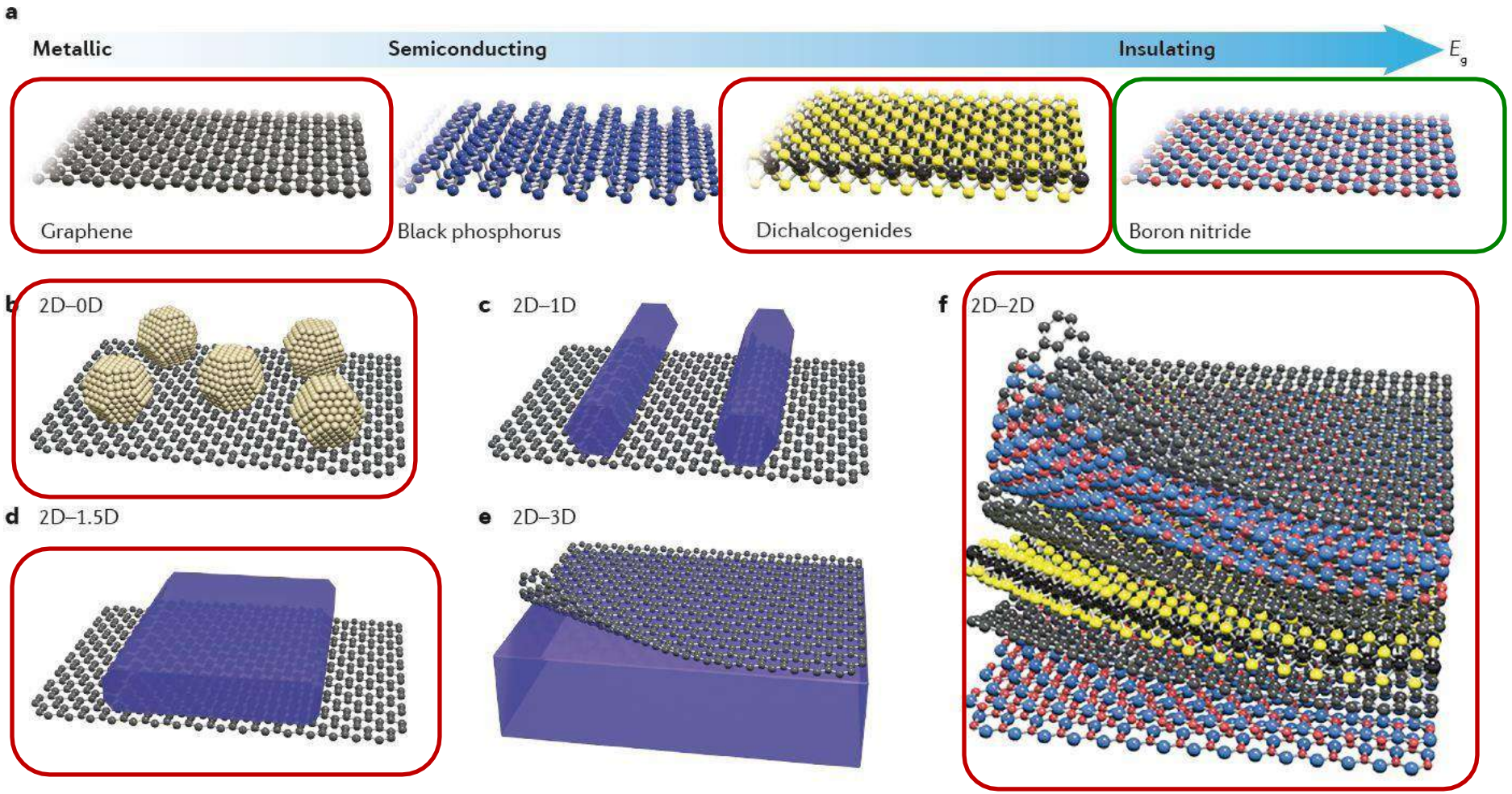








Hybrid systems and heterostructures



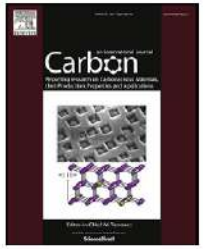
Y. Liu *et al.*, Nature Review Materials doi: 10.1038/natrevmats.2016.42

Carbon 168 (2020) 22–31

Contents lists available at ScienceDirect

Carbon

journal homepage: www.elsevier.com/locate/carbon



Combined effect of ^{13}C isotope and vacancies on the phonon properties in AB stacked bilayer graphene

Khalid N. Anindya [a, b, 1], Md. Sherajul Islam [a, 1, *], Akihiro Hashimoto [c], Jeongwon Park [b, d]

[a] Department of Electrical and Electronic Engineering, Khulna University of Engineering &Technology, Khulna, 9203, Bangladesh
[b] School of Electrical Engineering and Computer Science, University of Ottawa, Ottawa, ON K1N 6N5, Canada
[c] Graduate School of Engineering, University of Fukui, Fukui, 910-8507, Japan
[d] Department of Electrical and Biomedical Engineering, University of Nevada, Reno, USA

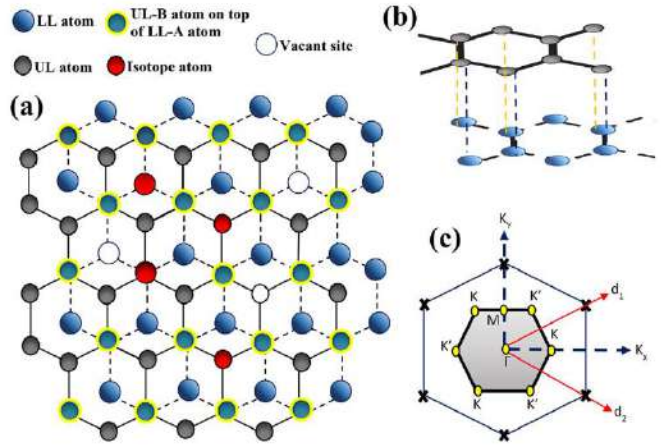


Fig. 1. (a) Top view of A-B stacked bilayer graphene. Upper layer A and B type atoms are represented by U-A and U–B while L-A and L-B denote lower layer A and B type atoms, respectively. The shadowed red and unfilled black circle shows the randomly induced ^{13}C isotope and vacancy sites, respectively. (b) Side view of A-B stacked bilayer graphene lattice. (c) Reciprocal lattice of graphene (single layer), where crosses represent the lattice points and d_1 and d_2 are reciprocal lattice vectors. The shadowed hexagon is the first Brillouin zone of graphene with high symmetry points Γ, K, M. (A colour version of this figure can be viewed online.)

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Keywords:
Phonon localization
Bilayer graphene
Isotope
Vacancy
Combined defect

ABSTRACT

The combined effects of ^{13}C isotope and vacancies on the phonon properties in AB stacked bilayer graphene (BLG) are explored theoretically. We have calculated the phonon density of states (PDOS) by varying the isotope contents (0–100%) and vacancies (0–30%) in both layers and only in the upper layer of the BLG using forced vibrational method. We found that both isotope and vacancy or merging of these two defects significantly affect the PDOS, especially, E_{2g} mode phonon, which is responsible for the Raman G band, shifted downward with the increase of defect concentrations. Moreover, when ^{13}C isotopes are induced only in the upper layer, E_{2g} peak splits into two peaks which corresponds well with the experimental results of $^{13}C/^{12}C$ dependence G peak splitting in the Raman spectra of BLG. We also explored the defect induced phonon localization in BLG. Our calculated typical mode patterns show that high frequency optical phonons are strongly localized in the vacancy as well as merging ^{13}C isotope and vacancy defected BLG. The calculated average localization length noticed that strong phonon localization exists at 60% ^{13}C isotope concentration. These findings are important for understanding the experimentally observed Raman spectra as well as thermal transport in BLG.

scientific reports

(Nature) Scientific Reports, 12, 761 (2022)

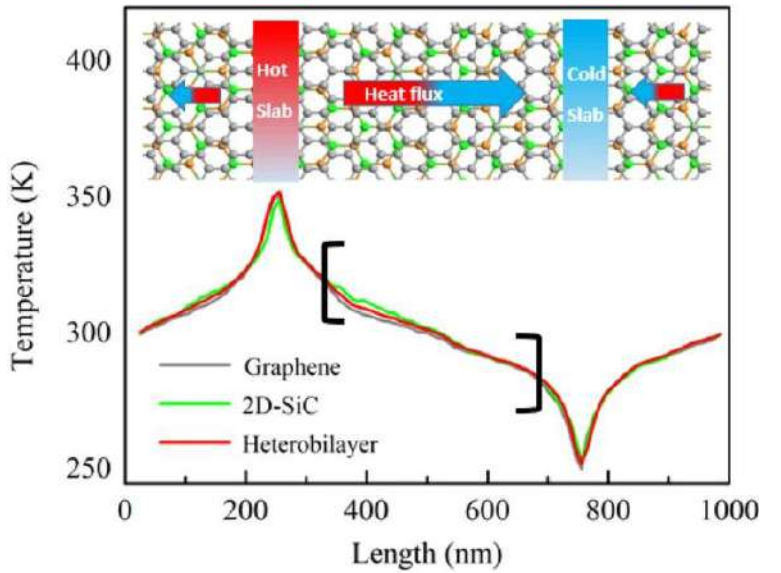
Check for updates

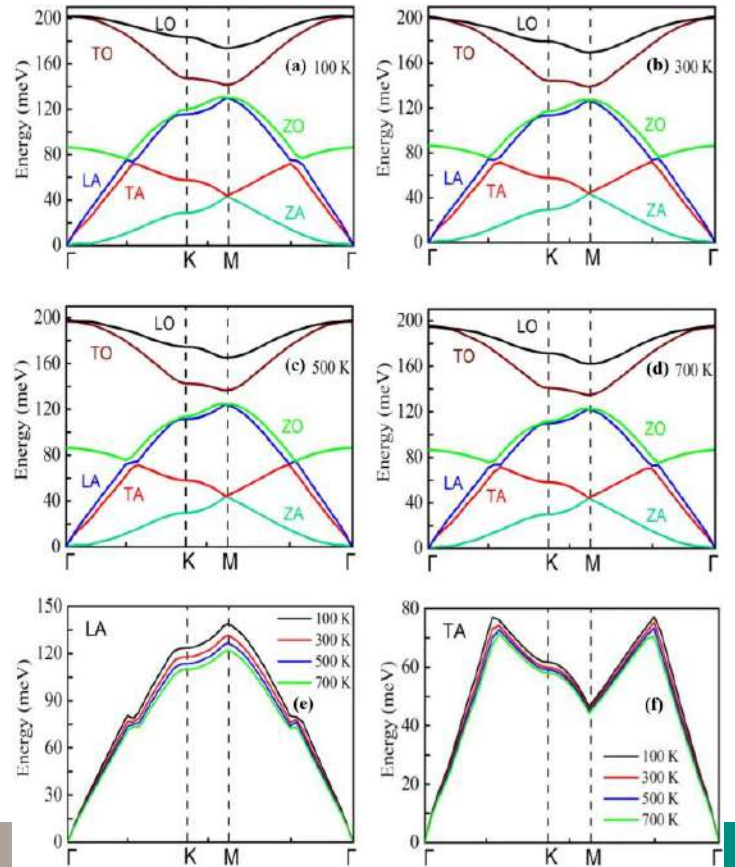
OPEN

Temperature and interlayer coupling induced thermal transport across graphene/2D-SiC van der Waals heterostructure

Md. Sherajul Islam[1,3]✉, Imon Mia[1], A. S. M. Jannatul Islam[1], Catherine Stampfl[2] & Jeongwon Park[3,4]

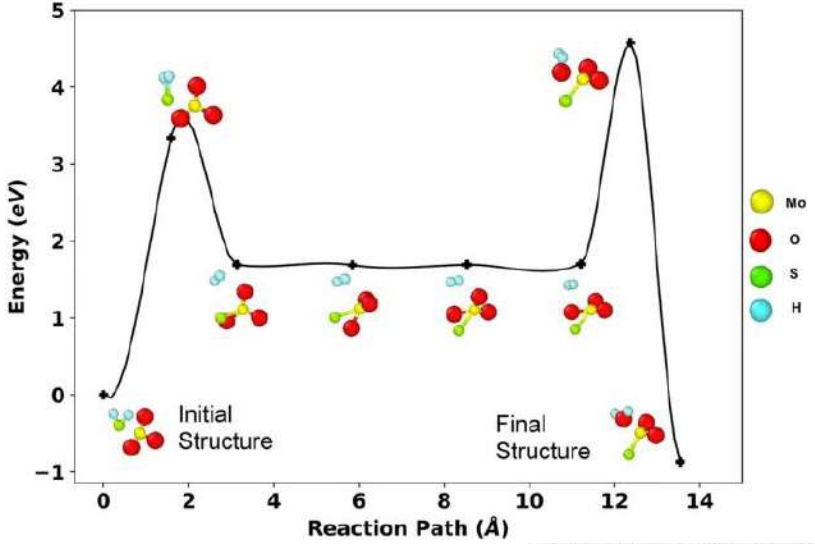
Graphene based two-dimensional (2D) van der Waals (vdW) materials have attracted enormous attention because of their extraordinary physical properties. In this study, we explore the temperature and interlayer coupling induced thermal transport across the graphene/2D-SiC vdW interface using non-equilibrium molecular dynamics and transient pump probe methods. We find that the in-plane thermal conductivity κ deviates slightly from the $1/T$ law at high temperatures. A tunable κ is found with the variation of the interlayer coupling strength χ. The interlayer thermal resistance R across graphene/2D-SiC interface reaches 2.71×10^{-7} Km^2/W at room temperature and $\chi = 1$, and it reduces steadily with the elevation of system temperature and χ, demonstrating around 41% and 56% reduction with increasing temperature to 700 K and a χ of 25, respectively. We also elucidate the heat transport mechanism by estimating the in-plane and out-of-plane phonon modes. Higher phonon propagation possibility and Umklapp scattering across the interface at high temperatures and increased χ lead to the significant reduction of R. This work unveils the mechanism of heat transfer and interface thermal conductance engineering across the graphene/2D-SiC vdW heterostructure.

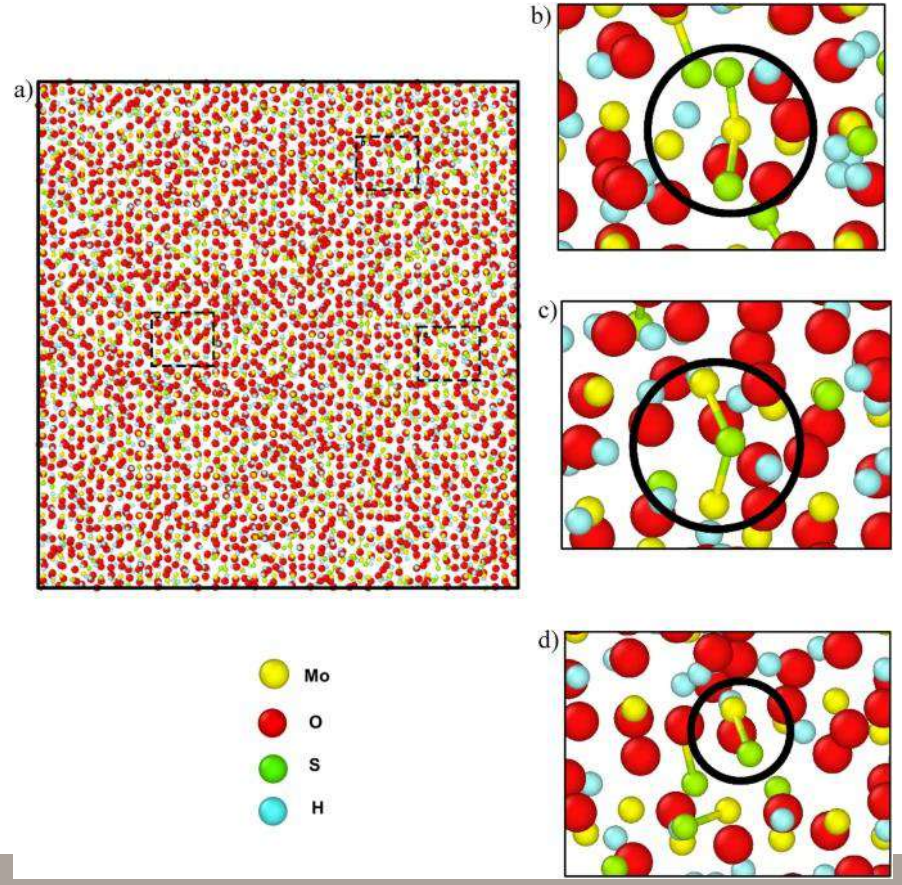




scientific reports

(Nature) Scientific Reports, 12, 16085 (2022)





OPEN

Atomistic reaction mechanism of CVD grown MoS_2 through MoO_3 and H_2S precursors

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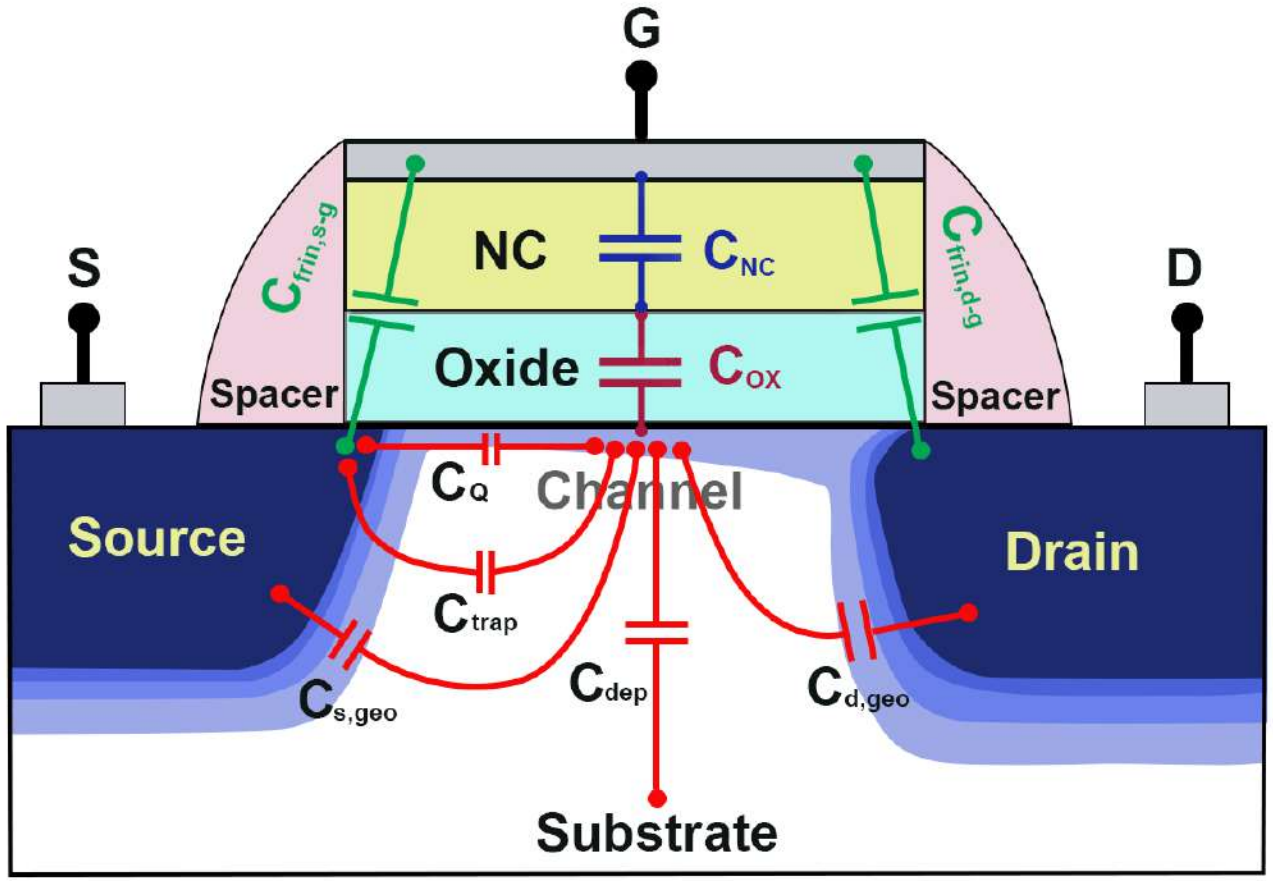
Chemical vapor deposition (CVD) through sulfidation of MoO_3 is one of the most important synthesis techniques to obtain large-scale and high-quality two-dimensional (2D) MoS_2. Recently, H_2S precursor is being used in the CVD technique to synthesize 2D MoS_2. Although several studies have been carried out to examine the mechanism of MoS_2 growth in the presence of sulfur and MoO_3 precursors, the growth of MoS_2 in the presence of H_2S precursor has largely remained unknown. In this study, we present a Reactive molecular dynamics (RMD) simulation to investigate the reaction mechanism of MoS_2 from MoO_3 and H_2S precursors. The intermediate molecules formation, the reason behind those formations, and the surface compositions of $MoO_xS_yH_z$ during the initial steps of CVD have all been quantified. Surprisingly, a sudden separation of sulfur atoms from the surface was observed in the H_2S precursor system due to the substantial oxygen evolution after 1660 K. The sulfur detachments and oxygen evolution from the surface were found to have a linear relationship. In addition, the intermediate molecules and surface bonds of MoS_2 synthesized by MoO_3 and H_2S precursors were compared to those of a system using S_2 and MoO_3 precursors. The most stable subsidiary formation from the H_2S precursor was found to be H_2O, whereas in case of S_2 precursor it was SO. These results provide a valuable insight in the formation of large-scale and high-quality 2D MoS_2 by the CVD technique.

Agenda

- Introduction
- Semiconductor R&D Trends
- Transistor Scaling
- 2D Materials and Devices
- Negative Capacitance FETs
- Brief Introduction of Other Research Areas in My Group
  - Wide-Bandgap Semiconductors
  - Wireless Power Transfer
  - Brain-Computer Interface
- Challenges and Prospects

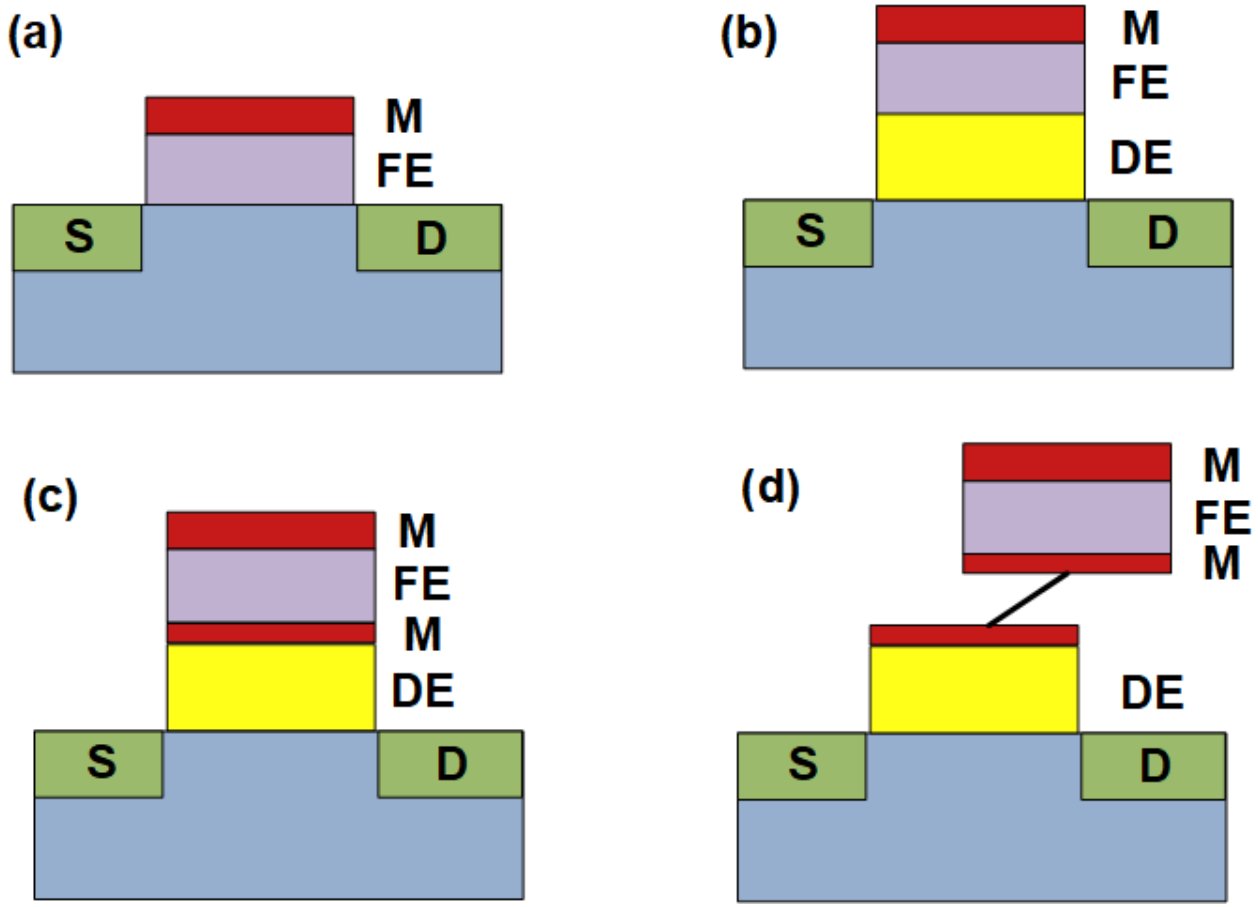
Capacitors in generic NCFET structure



The quantum-, trap-, s/d geometrical-, and depletion- induced capacitors are designated as C_Q, C_{trap}, $C_{s/d,geo}$, and C_{dep}, respectively. The capacitance of the NC and oxide layers is represented by C_{NC} and C_{OX}, respectively. However, the influence of fringing capacitance, $C_{frin,s/d-g}$, on channel potential regulation is irrelevant as it is screened by power rails.

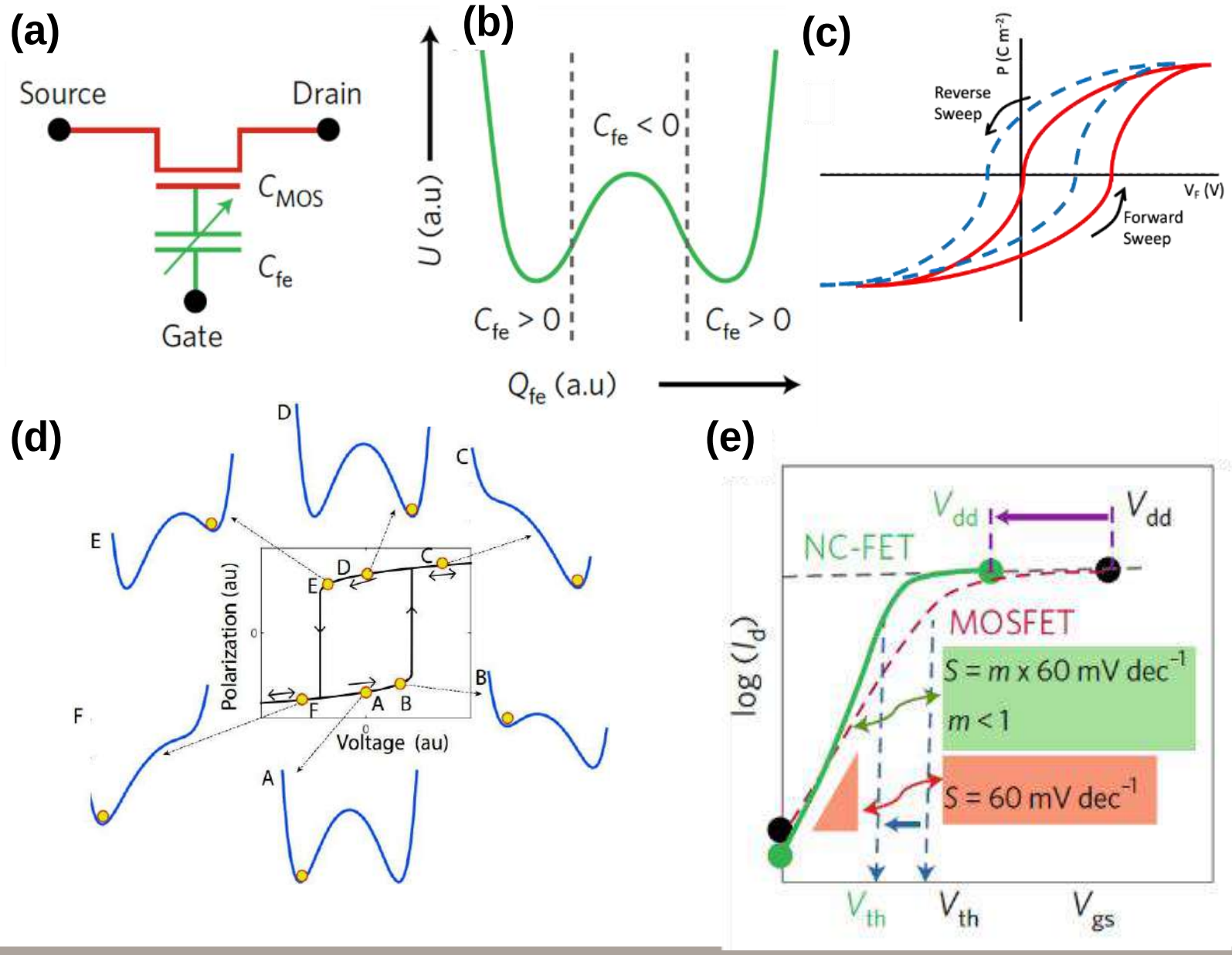
W. Cao and K. Banerjee, "Is negative capacitance FET a steep-slope logic switch?," *Nat. Commun.*, vol. 11, no. 1, pp. 1–8, 2020.

Schematic device structures of the NCFETs reported in experimental works



(a) The FE layer is directly contacted with the channel materials; (b) A dielectric layer is used as a buffer layer and capacitance matching layer between the ferroelectric layer and the channel materials; (c) A metal electrode is inserted between the ferroelectric and dielectric layer; (d) A FE capacitor is externally connected with the conventional FET with a dielectric layer.

Negative Capacitance Field Effect Transistor (NCFET)



(a) Circuit representation of a Negative Capacitance Field Effect Transistor (NCFET).

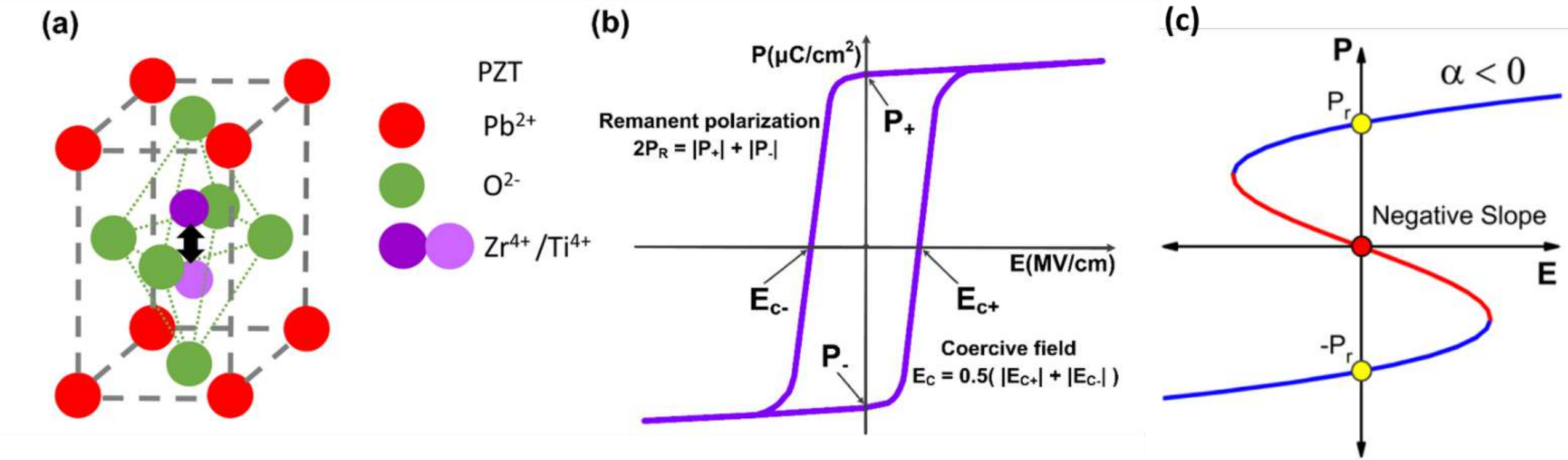
(b) Energy versus charge behavior of a typical NCFET.

(c) Schematic illustration of the ferroelectric polarization *P(t)* as a function of the ferroelectric voltage (V_F),

(d) Ferroelectric capacitor polarization-voltage hysteresis showing energy landscapes at various positions, and

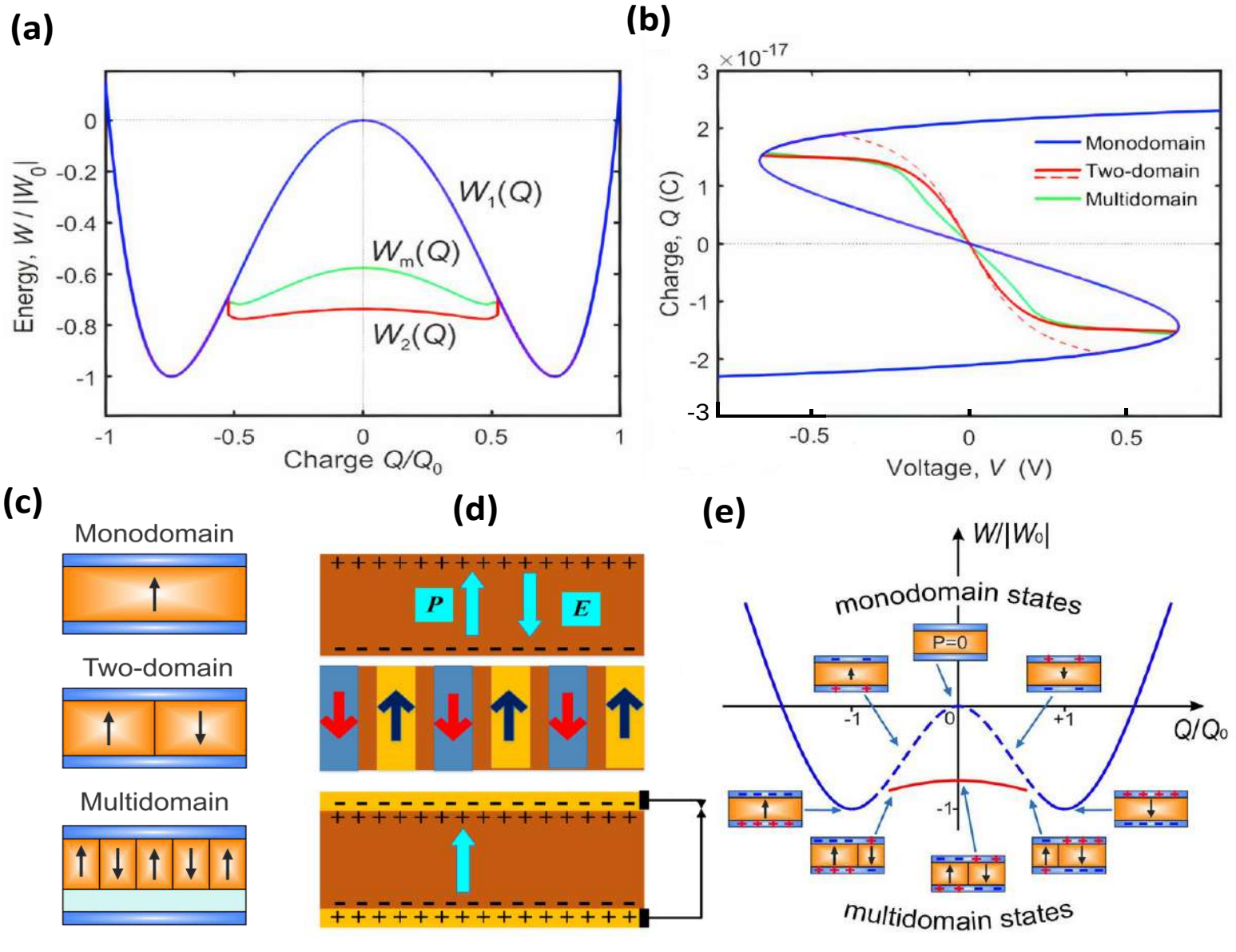
(e) effect of NC performance on the subthreshold slope.

PZT crystal Structure and a typical ferroelectric hysteresis curve



(a) Illustration of the two stable locations of a core Zr^{4+} or Ti^{4+} ion in a PZT crystal [23]. (b) A typical ferroelectric hysteresis curve (PE loop), depicting the essential features of remnant polarization and coercive field. (c) Ferroelectric $P(E)$ behavior showing negative slope in the region where P and E are in opposite directions.

The negative capacitance characteristic of a typical FE (PZT) material.



(a) The FE free energy vs. applied charge (*W*-*Q*) relation.

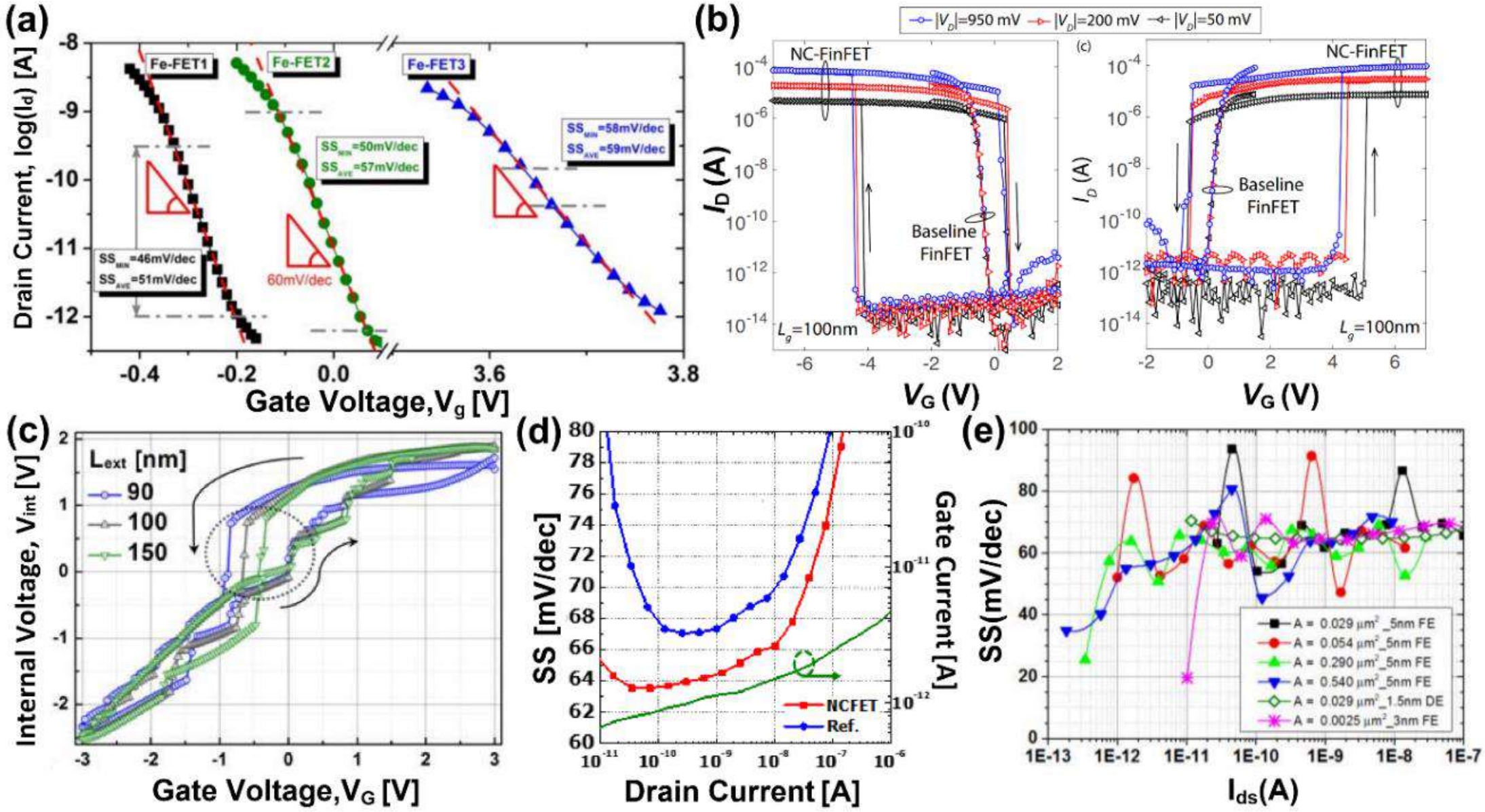
(b) The charge-voltage characteristics (*Q*-*V)* are obtained from (a)

(c) An illustration of a ferroelectric layer's domain arrangements. Monodomain, two-domain, and multidomain states are shown from top to bottom [30].

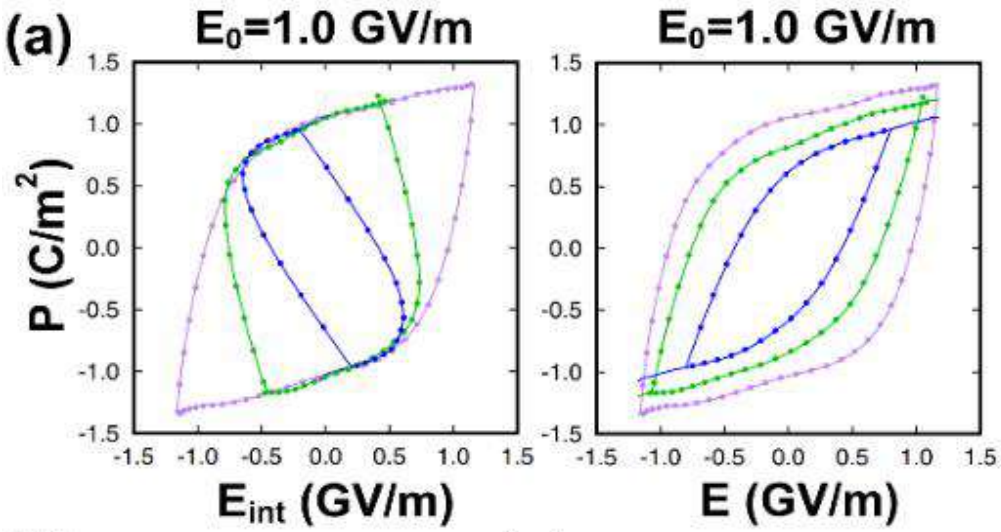
(d) FE monodomain samples where polarization (*P*) and surface charges induce depolarization field (*E*) are shown. (middle) Formation of the periodic domain structure with the up/down oriented polarization and (bottom) the FE sample with short-circuited electrodes vanishes the depolarization field. As a result, the monodomain structure with uniform polarization is formed again [31].

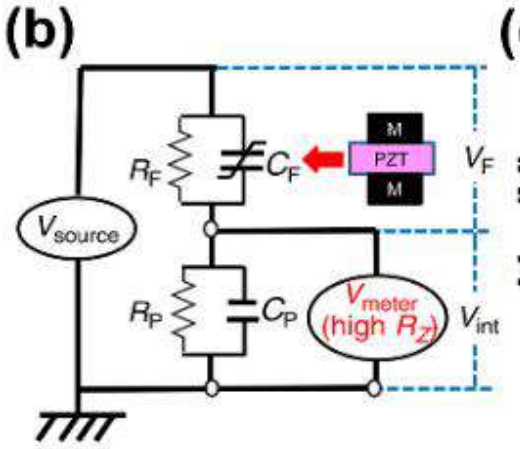
(e) The normalized energy and polarization states of the ferroelectric (orange) capacitor as a function of the normalized driving charge. The equilibrium charge and energy of the monodomain short-circuited capacitor are represented by Q_0 and W_0, respectively. The dashed line demonstrates the unstable energy of the monodomain state. The red curve depicts the energy of a stable two-domain state [30].

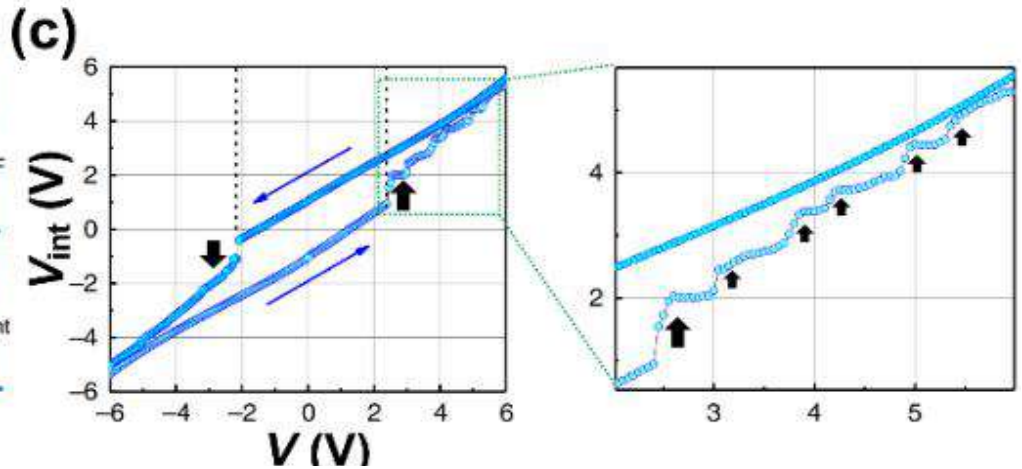
Examples of negative-capacitance-based device characteristics

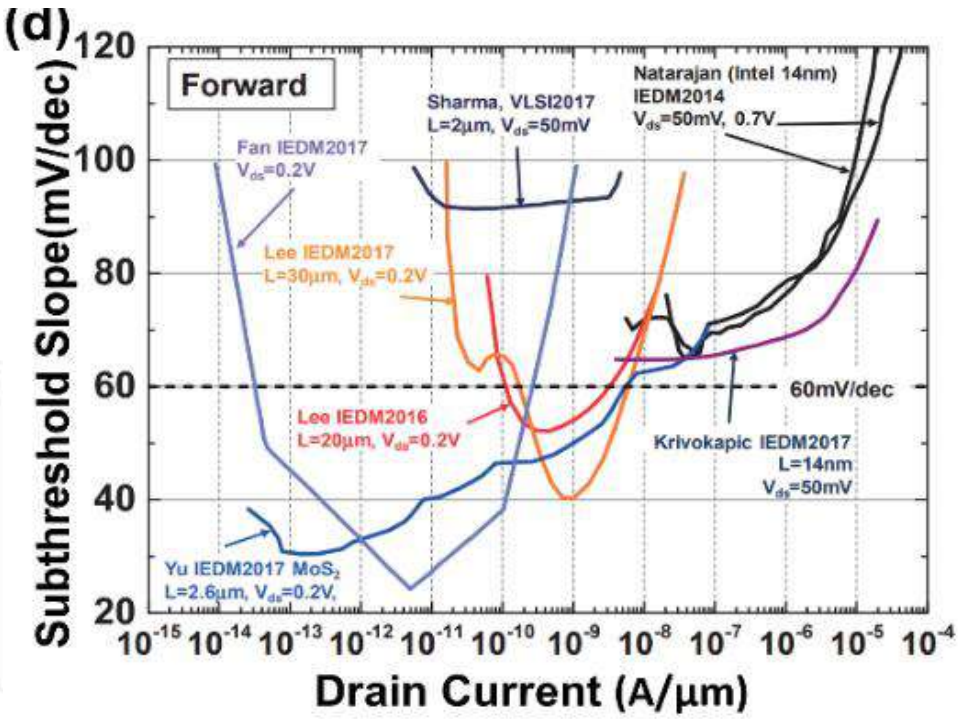


Examples of NCFET characteristics



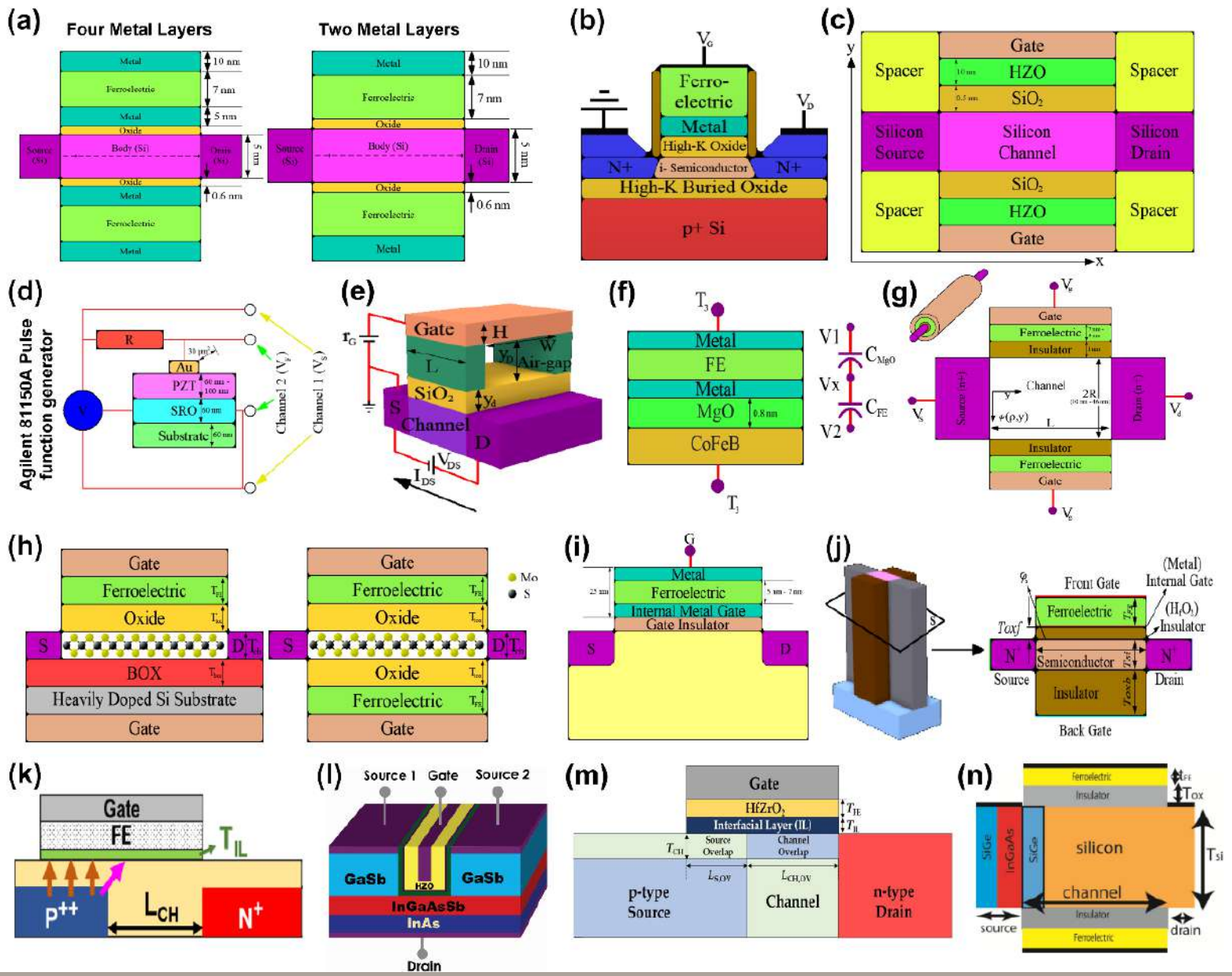






(a) Dependence of the polarization on the internal field and applied field in the $PbTiO_3$ film [93].
(b) Equivalent circuit of V_{int} measurement in FE/DE system. R_F and R_P are the insulating resistance of the FE- and DE capacitors, respectively. Note that a high impedance system is required to obtain the accurate V_{int} [94].
(c) V_{int}-V characteristics during V sweeping of FE/DE system, V_{int} jump occur along with V_F drop at V_F= ~$\pm V_c$ [94].
(d) Benchmark of SS values of some reported NC FETs [84].

Examples of negative-capacitance-based device structures



a) metal-ferroelectric-metal-insulator-semiconductor (MFMIS) and the metal-ferroelectric-insulator-semiconductor (MFIS) configurations[26], b) schematic cross-section view of a NCFET with high-k buried oxide (BOX) over a degenerately doped Si ground plane[28], c) a physics-based model for ferroelectric/negative capacitance transistors (FEFETs/NCFETs) that does not include an interlayer metal between the ferroelectric and dielectric in the gate stack[31], d) negative capacitance in a thin epitaxial ferroelectric layer was observed where the voltage across the ferroelectric capacitor is discovered to be lowering with time when a voltage pulse is applied[27], e) MOSFETs with ferroelectric gate stacks were used to investigate the effects of negative capacitance on various device properties[29], f) an all spin logic device with voltage controlled magnetic anisotropy (VCMA-ASL) that uses negative capacitance (NC) effect as an unique technique to increase the VCMA effect[34], g) gate-all-around negative capacitance transistor (GAA-NCFET)[35], h) double-gate metal-ferroelectric-insulator-semiconductor NCFETs using a 2-D semiconducting transition-metal-dichalcogenide (TMD) channel[99], i) schematic of NCFET[37], j) negative-capacitance independent multi-gate FinFET (NC-IMG-FinFET)[38], k) schematic of nominal NCVT-FET[92], l) schematic of dual source negative capacitance GaSb/InGaAsSb/InAs heterostructure based vertical TFET[93], m) schematic of NCTFET[94], and n) schematic of ferroelectric NCTFET[95].

AIP Advances

$HfO_2/TiO_2/HfO_2$ tri-layer high-K gate oxide based MoS_2 negative capacitance FET with steep subthreshold swing

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Submitted: 05 January 2020 . Accepted: 14 February 2020 . Published Online: 02 March 2020

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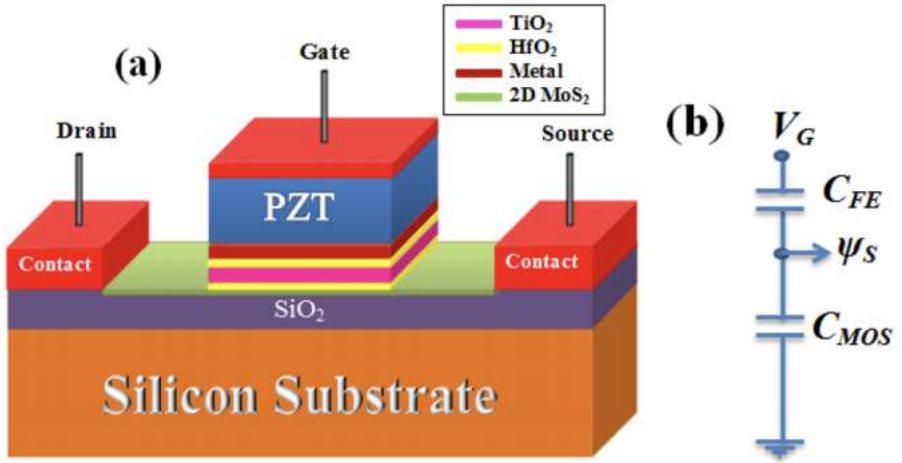

FIG. 1. (a) Schematic diagram for the MoS_2 negative capacitance FET and (b) the capacitance model, where the total equivalent capacitance of the 2D MoS_2 FET (C_{MOS}) and FE layer (PZT) capacitance (C_{FE}) are in a series combination and V_G acts as the effective gate voltage of the FET including PZT. The gate voltage of the MoS_2 FET becomes the surface potential ψ_s due to the incorporation of PZT.

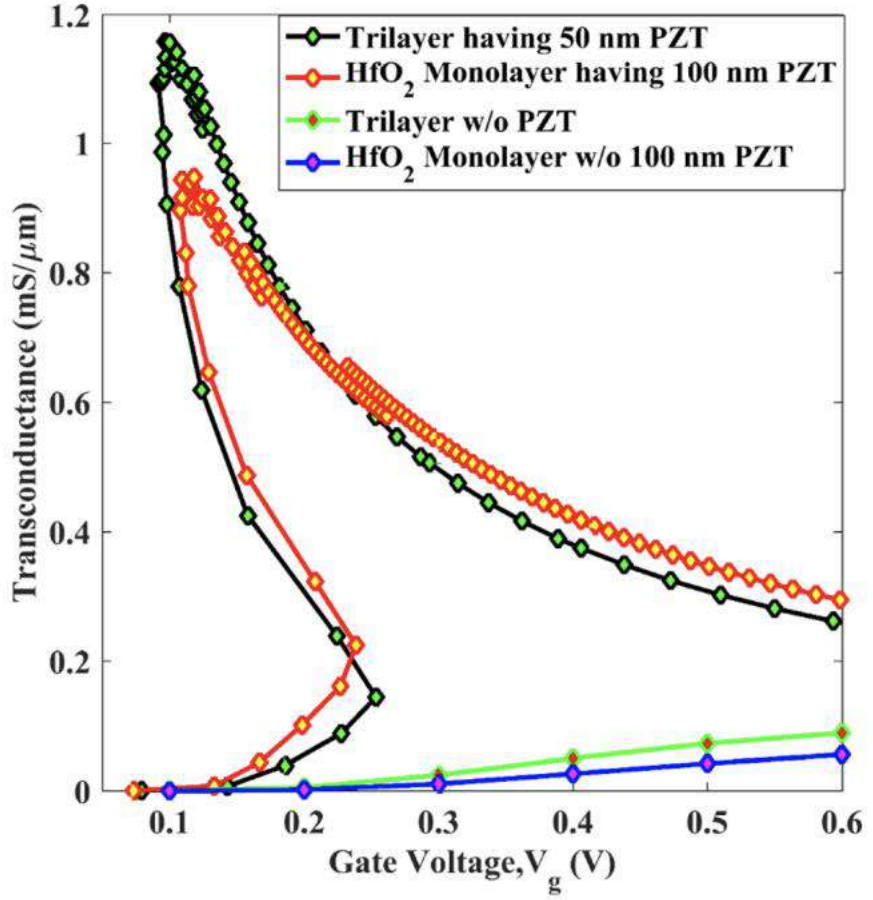

FIG. 9. Comparison of transconductance vs gate voltage of the 2D MoS_2 NCFET using the trilayer $HfO_2/TiO_2/HfO_2$ and single layer HfO_2.

Our results have shown tremendous improvement in the current on–off ratio as well as the transconductance value that suppresses all the results found from other works performed until now.

Using the TCAD Silvaco simulation

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Numerical Analysis of Gate-All-Around $HfO_2/TiO_2/HfO_2$ High-K Dielectric Based WSe_2 NCFET With Reduced Sub-Threshold Swing and High On/Off Ratio

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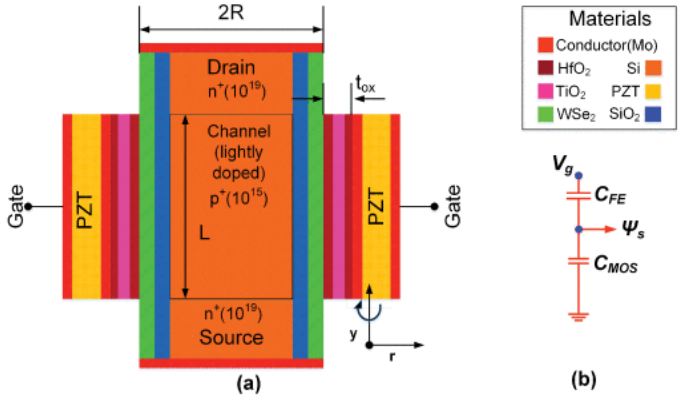

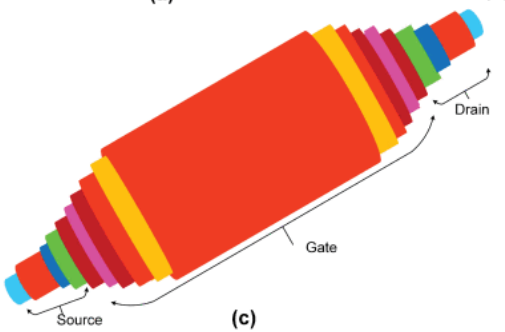

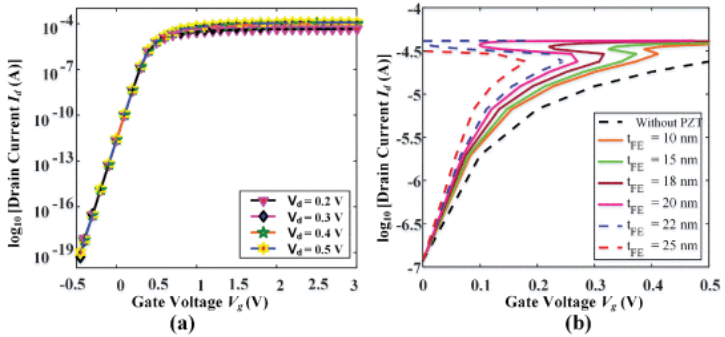

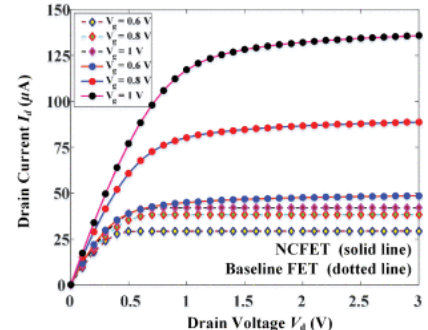

Using the TCAD Silvaco simulation

Subthreshold swing (SS): 18.9 mV/dec
I_{ON}/I_{OFF} ratio: 10^{12}
transconductance (*gm*) of 117 μS
cut-off frequency (f_T) of 335 GHz

Results in Physics 29 (2021) 104796

Contents lists available at ScienceDirect

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journal homepage: www.elsevier.com/locate/rinp

Dual source negative capacitance GaSb/InGaAsSb/InAs heterostructure based vertical TFET with steep subthreshold swing and high on-off current ratio

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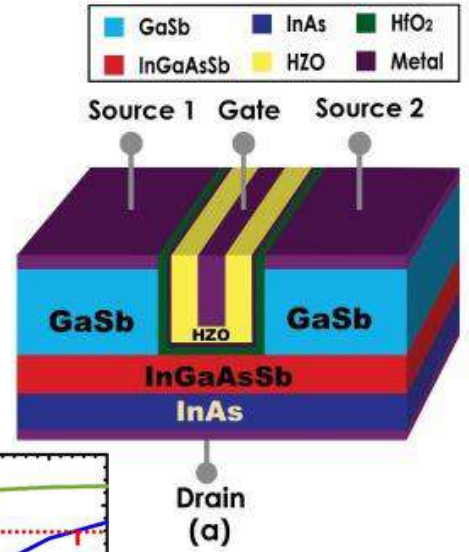
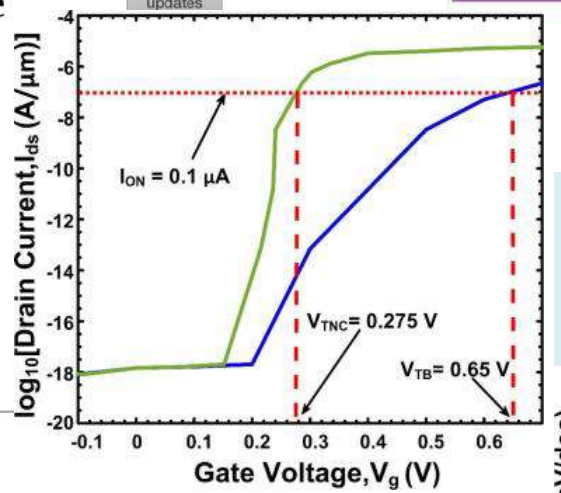
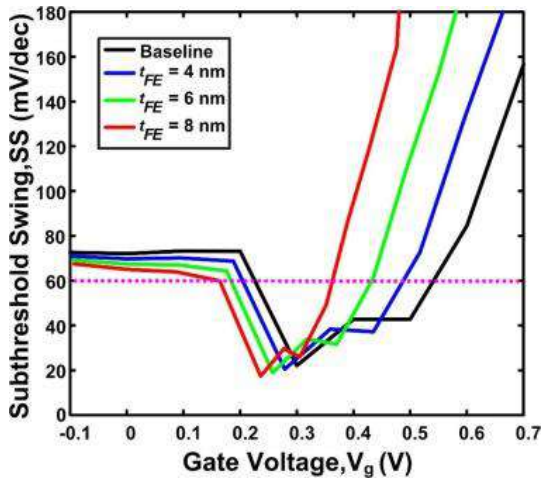




Subthreshold swing (SS): 17.37 mV/dec
I_{ON}/I_{OFF} ratio: 10^{12}



Using the TCAD Silvaco simulation

ARTICLE INFO

Keywords:
Vertical tunnel FET
Dual source
Ferroelectric material
Negative capacitance
Heterojunction

ABSTRACT

Continuous downscaling of CMOS technology at the nanometer scale with conventional MOSFETs leads to short channel effects (SCE), increased subthreshold slope (SS), and leakage current, degrading the performance of ICs. We proposed a dual-source vertical tunnel field-effect transistor (TFET) with a steeper subthreshold swing (SS) and superior electrostatic control thanks to quantum mechanical band-to-band tunneling. We show that the use of GaSb/InGaAsSb/InAs heterostructure boosts the band-to-band tunneling rate in TFETs, resulting in higher on-state current. Incorporating the negative capacitance effect using ferroelectric materials further enhances the performance of the proposed device greatly. The lowest SS of 21.94 mV/dec and an on–off current ratio of 4.3267×10^{11} were obtained for dual source GaSb/InGaAsSb/InAs heterostructure based vertical TFET. The lowest subthreshold swing was found as 17.37 mV/dec after integrating $Hf_{1-x}Zr_xO_2$ ferroelectric material into the gate stack. The negative capacitance effect also increases the on-state current tenfold, resulting in an incredible I_{ON}/I_{OFF} ratio of 10^{12}. The suggested device focuses on low power consumption applications by assuring a very low leakage current and a reduced subthreshold swing.

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Numerical Investigations of Nanowire Gate-All-Around Negative Capacitance GaAs/InN Tunnel FET

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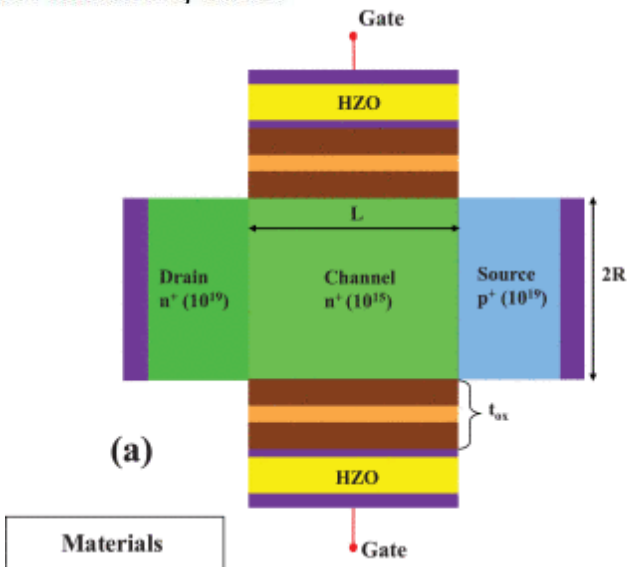
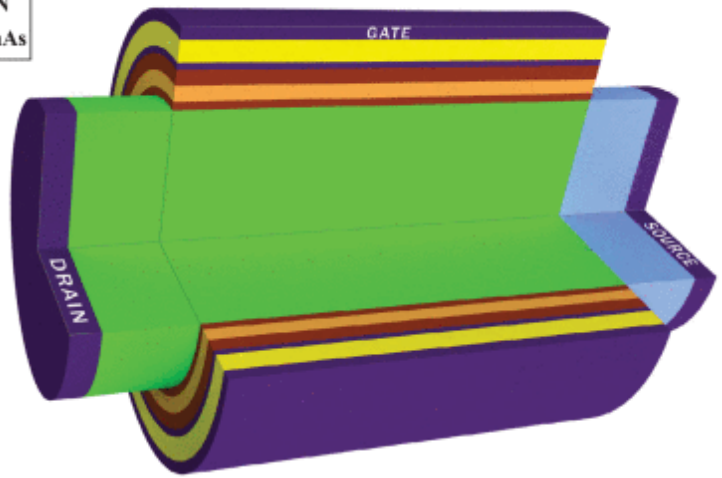
Corresponding author: Md. Sherajul Islam (sheraj_kuet@eee.kuet.ac.bd)



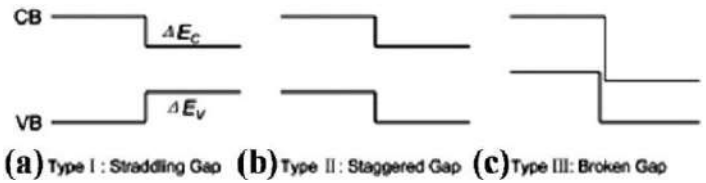


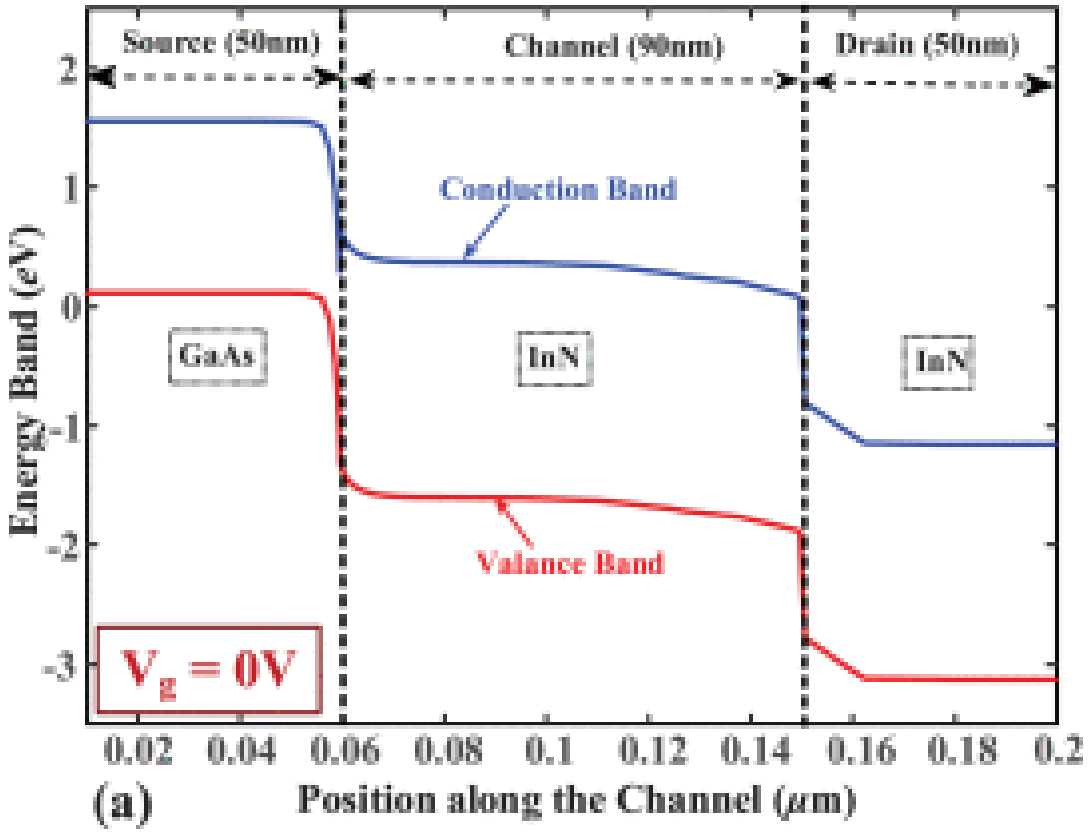
Subthreshold swing (SS): 20.56 mV/dec
I_{ON}/I_{OFF} ratio: 10^{11}

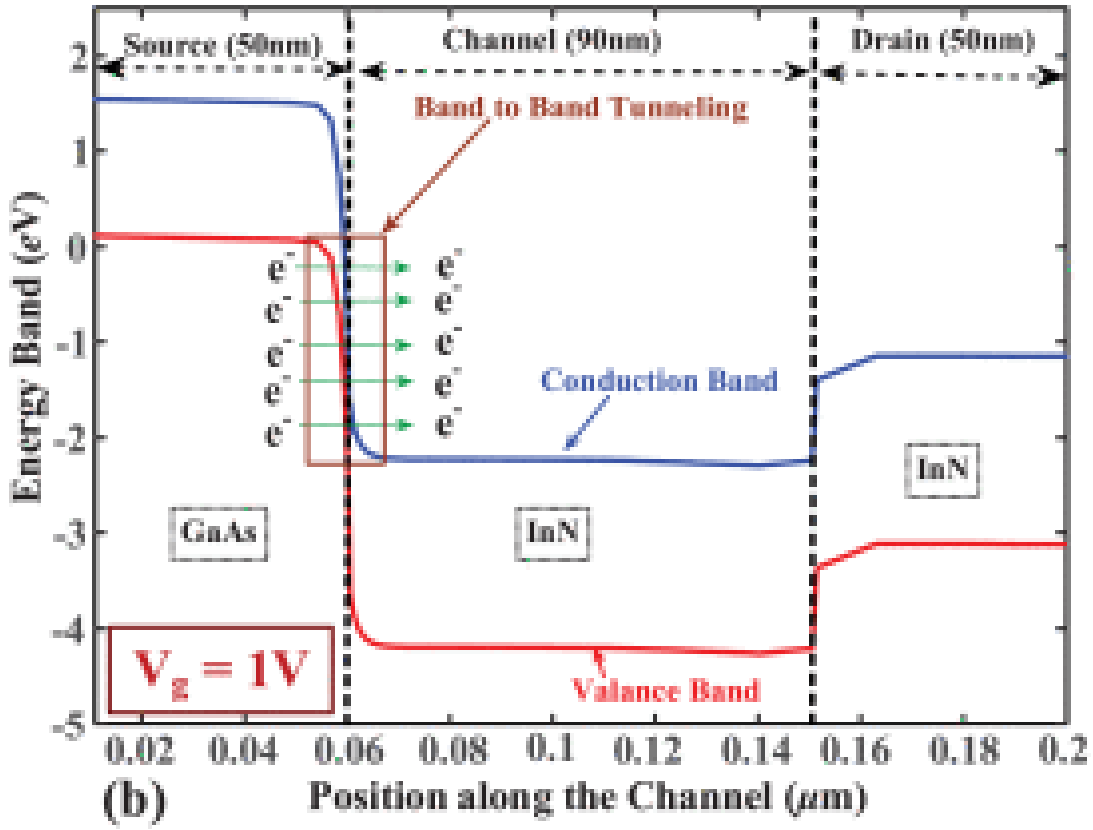
Performance Parameters	This Work	Previous Work
Sub-threshold Swing (SS)	18.9 mV/dec	14.4 mV/dec [24], 18.2 mV/dec [23]
On-state Current (I_{ON})	119 μA	210 μA [22], 239 μA [24]
On/Off ratio (I_{on}/I_{off})	10^{12}	$>10^6$ [22], 3×10^{14} [41]
Transconductance (g_m)	117 μS	12 μS [43], 1.1 mS [41]

Using the TCAD Silvaco simulation

Energy Band diagram of n-channel GAA nanowire Tunnel-FET along X-position



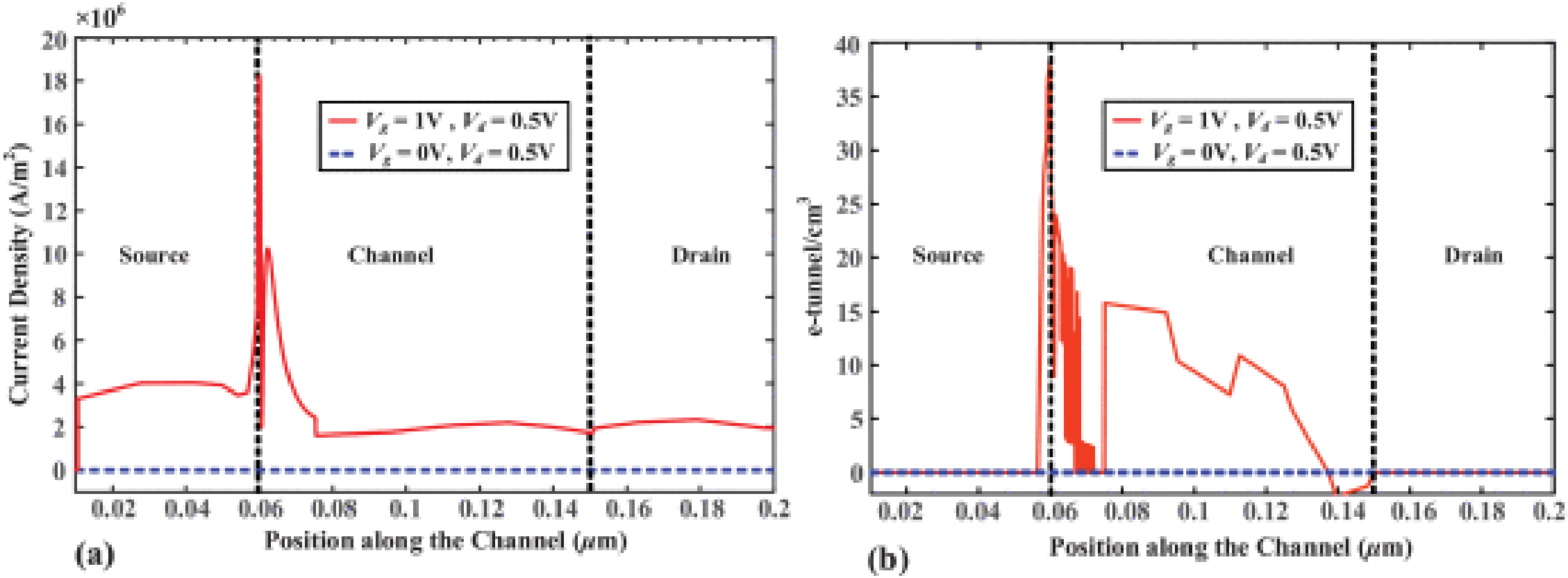




(a) band diagram for OFF-state (Vg=0V and Vd=0.5V), (b) band diagram for ON-state (Vg=1V and Vd=0.5V).

A. A. M. Mazumder, K. Hosen, M. S. Islam and J. Park, "Numerical Investigations of Nanowire Gate-All-Around Negative Capacitance GaAs/InN Tunnel FET," in *IEEE Access*, vol. 10, pp. 30323-30334, 2022, doi: 10.1109/ACCESS.2022.3159809.

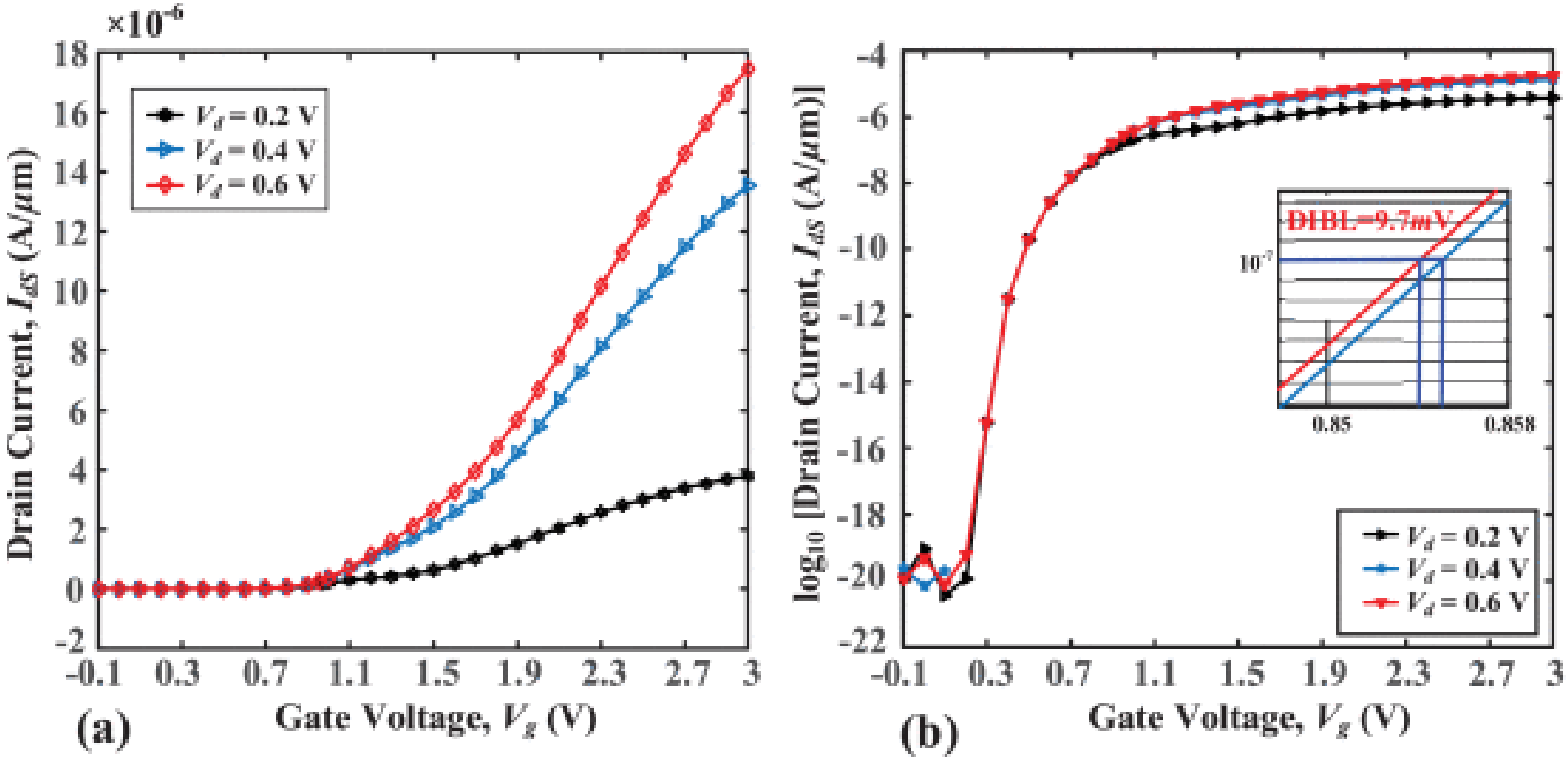
Distribution profile of the current density and e-tunneling



The distribution profile of the current density and e-tunneling along with the position of channel length in different gate voltages for the nanowire GAA n-channel Tunnel-FET; (a) current density vs position along the channel, showing a maximum value of 1.8×10^{7} A/m^2 (b) e-Tunneling in logarithmic scale vs position along the channel showing the highest value of $\approx10^{38}$/cm^3.

A. A. M. Mazumder, K. Hosen, M. S. Islam and J. Park, "Numerical Investigations of Nanowire Gate-All-Around Negative Capacitance GaAs/InN Tunnel FET," in *IEEE Access*, vol. 10, pp. 30323-30334, 2022, doi: 10.1109/ACCESS.2022.3159809.

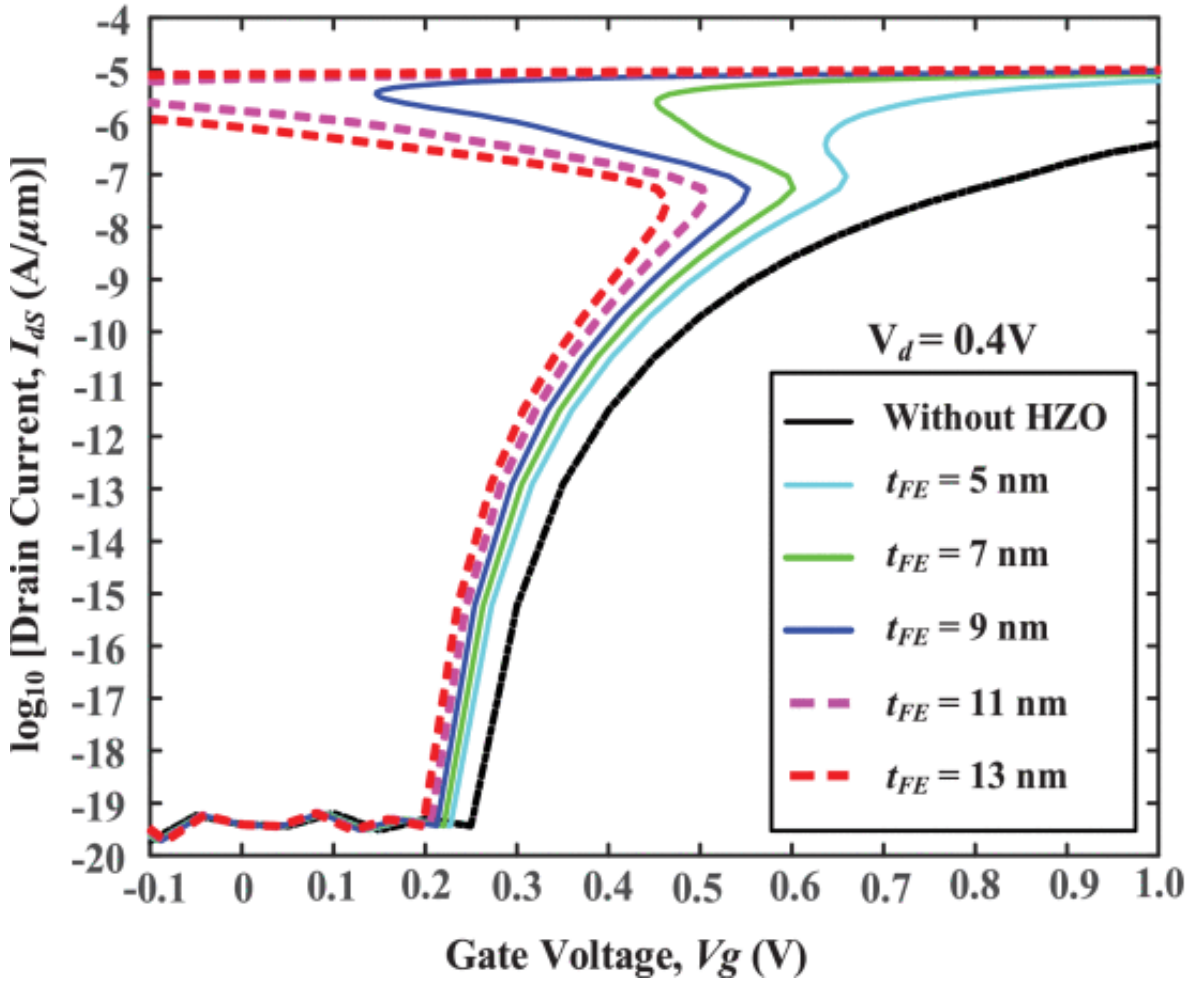
Transfer characteristics of the baseline NGAA Tunnel-FET



Transfer characteristics of the baseline NGAA Tunnel-FET (a) Ids vs Vg , showing a large saturation current of 17μA and a maximum I_{ON}/I_{OFF} ratio of ≈1.132×10^{9} at Vd=0.6V , and (b) log10 (Ids) vs Vg curve by differing Vd , showing a low DIBL of 9.7 mV.

A. A. M. Mazumder, K. Hosen, M. S. Islam and J. Park, "Numerical Investigations of Nanowire Gate-All-Around Negative Capacitance GaAs/InN Tunnel FET," in *IEEE Access*, vol. 10, pp. 30323-30334, 2022, doi: 10.1109/ACCESS.2022.3159809.

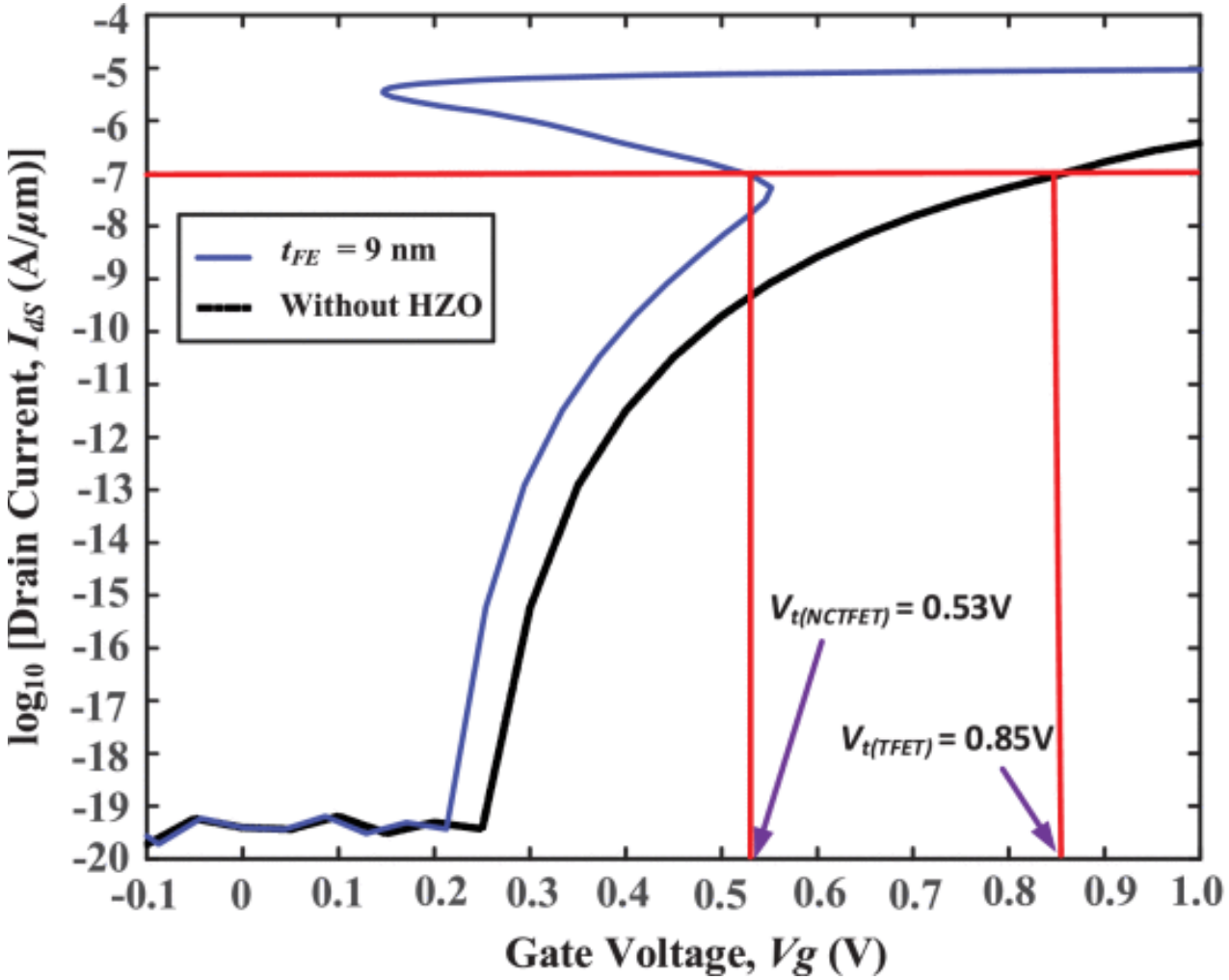
Transfer characteristics (I_{ds} vs V_g)



Transfer characteristics (Ids vs Vg) of nanowire gate all around NC Tunnel-FET for various HZO thicknesses. At tFE=9 nm, the value of drain current is 135μA .

A. A. M. Mazumder, K. Hosen, M. S. Islam and J. Park, "Numerical Investigations of Nanowire Gate-All-Around Negative Capacitance GaAs/InN Tunnel FET," in *IEEE Access*, vol. 10, pp. 30323-30334, 2022, doi: 10.1109/ACCESS.2022.3159809.

Threshold voltage of the baseline structure

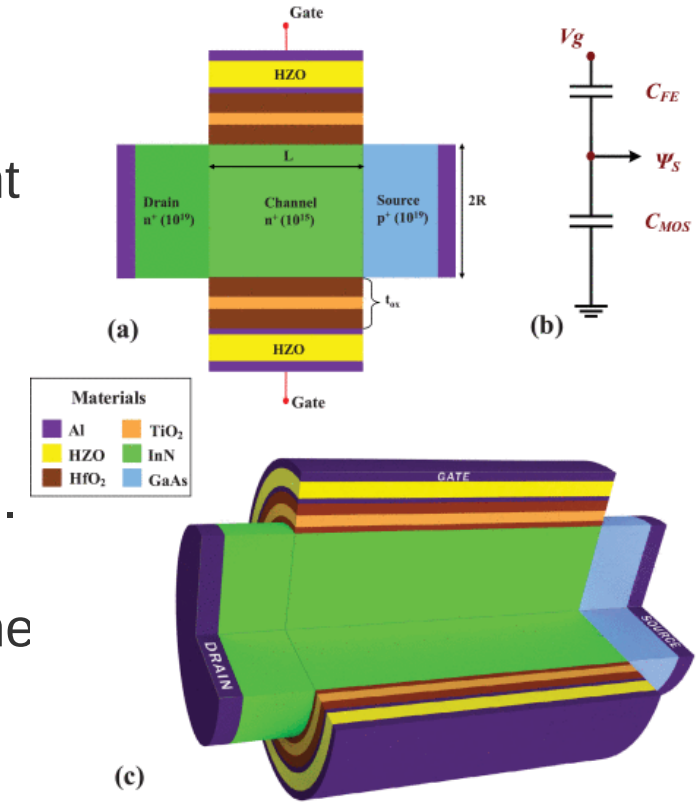


Performance evaluation of the proposed structure with and ferroelectric materials. The threshold voltage of the baseline structure is 0.85 V (Vt(TFET)), whereas it reduces to 0.53 V (Vt(NCTFET)) once the NC effect is introduced.

A. A. M. Mazumder, K. Hosen, M. S. Islam and J. Park, "Numerical Investigations of Nanowire Gate-All-Around Negative Capacitance GaAs/InN Tunnel FET," in *IEEE Access*, vol. 10, pp. 30323-30334, 2022, doi: 10.1109/ACCESS.2022.3159809.

Highlights

- A hybrid nanowire GAA NCTFET structure is demonstrated by combining the GaAs/InN baseline TFET and a ferroelectric layer (HZO) in the gate stack.
- The use of large lattice-mismatched materials enables the staggered and broken bandgap alignment, and the GAA structure maintains better current conduction and carrier control capabilities of the device.
- The GAA TFET channel architecture and ferroelectric gate insulator are adjusted to obtain the optimum band-to-band tunneling and potential amplification, therefore the highest ION/IOFF ratio of NCTFET is achieved.
- The proposed GaAs/InN nanowire gate all around NCTFET ameliorates the limitations of scaling down the transistor size and reduces power consumption.
- Therefore, GaAs/InN nanowire GAA NCTFET creates a unique route for the ongoing advancement of the applicability of electronic devices, seems to be a viable option for an Internet of Things (IoT) technological platform.



Challenges of NCFETs

- NCFET technology comes with an important side effect in which it increases the total capacitance of transistor, which can lead to **reliability problems** caused by IR-drop and voltage fluctuation during circuit's operation.

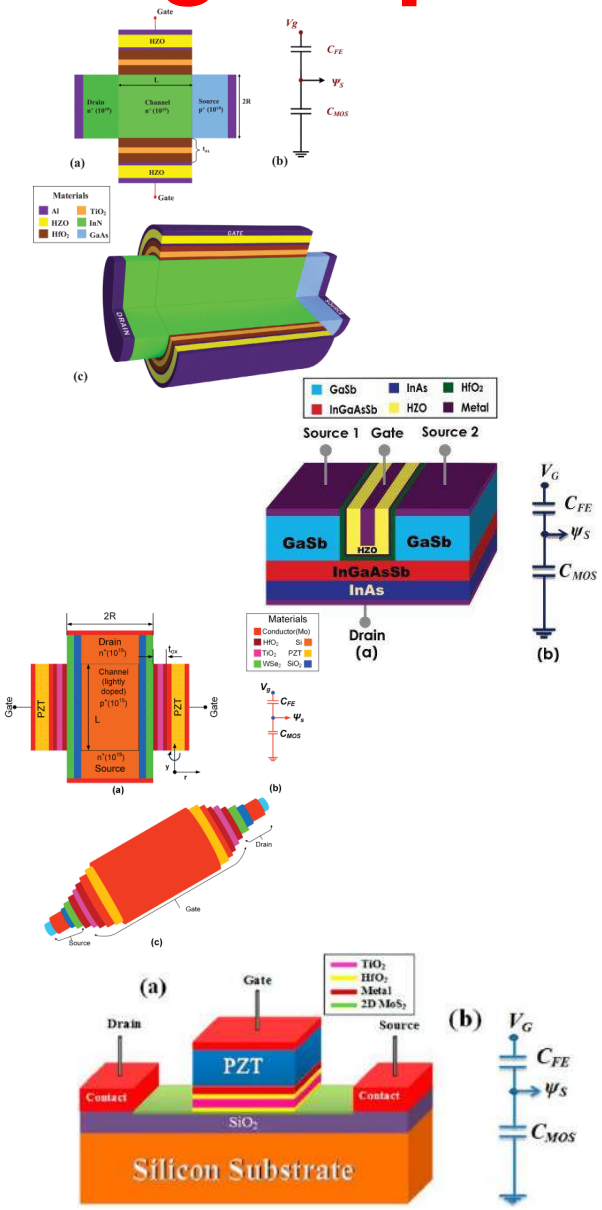
- At the same time, because NCFET technology enables circuits to operate at lower voltages, it is expected that other **reliability problems**, related to lifetime, to become much less because all the underlying aging mechanisms, such as negative bias temperature instability (BTI) and hot-carrier injection (HCI), strongly depend on the operating voltage.

Prospects of NCFETs

- Because of the high need for low-power FET technology, NCFETs have received much attention since Salahuddin and Datta's work.
- Although significant progress has been made in establishing the NC effects both theoretically and empirically, numerous obstacles remain before NCFETs can be used in genuine consumer devices.
- Although NCFETs will open a new era of transistors to satisfy the demands of a new low-power switch, NCFET optimization and device physics will necessitate a thorough grasp of a wide range of applications.

Recent Publications: NCFETs from our group

- Negative-Capacitance Field-Effect Transistors: Behind the Origin and Challenges, Md. Sherajul Islam, Abdullah Al Mamun Mazumder, Changjian Zhou, Catherine Stampfl, Jeongwon Park, Cary Y. Yang, **IEEE Journal of Electronic Device Society (2023)** DOI: 10.1109/JEDS.2023.3267081 (Impact Factor: 2.523)
- Numerical Investigations of Nanowire Gate-all-around Negative Capacitance GaAs/InN Tunnel FET, Abdullah Al Mamun Mazumder, Kamal Hosen, Md. Sherajul Islam, Jeongwon Park, **IEEE Access,** 10, 30323 (2022) (Impact Factor: 3.367)
- Dual Source Negative Capacitance GaSb/InGaAsSb/InAs Heterostructure Based Vertical TFET with Steep Subthreshold Swing and High On-Off Current Ratio, Sohag, Minhaz Uddin, Md Sherajul Islam, Kamal Hosen, Md Al Imran Fahim, Md Mosarof Hossain Sarkar, and Jeongwon Park, **Results in Physics**, 104796, (2021) (Impact Factor: 4.476)
- Numerical Analysis of Gate-all-around $HfO_2/TiO_2/HfO_2$ High-K Dielectric Based WSe_2 NCFET with Reduced Sub-threshold Swing and High On/Off Ratio, Kamal Hosen; Md. Sherajul Islam; Catherine Stampfl; Jeongwon Park, **IEEE Access,** 9, 116254 - 116264 (2021) (Impact Factor: 3.367)
- $HfO_2/TiO_2/HfO_2$ tri-layer high-K gate oxide based MoS_2 negative capacitance FET with steep subthreshold swing**,** Md. Sherajul Islam , Shahrukh Sadman, A. S. M. Jannatul Islam, and Jeongwon Park, **AIP Advances** 10, 035202 (2020) (Impact Factor: 1.548)

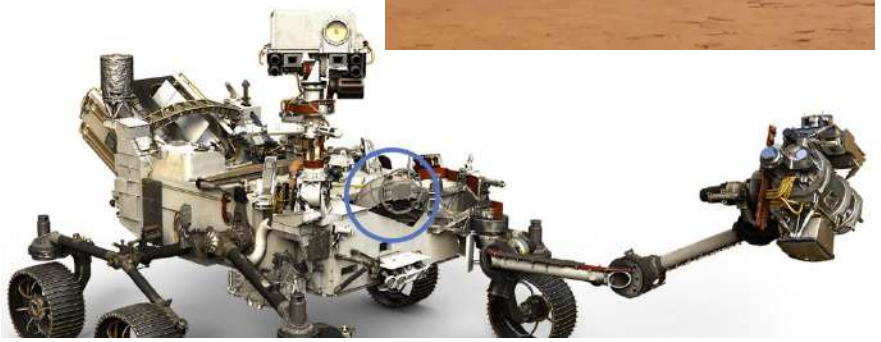


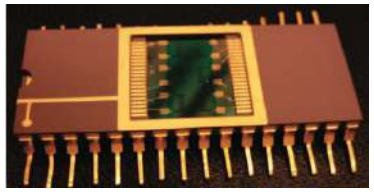
Agenda

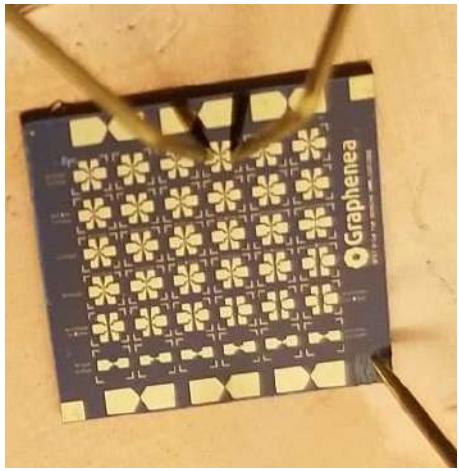
- Introduction
- Semiconductor R&D Trends
- Transistor Scaling
- 2D Materials and Devices
- Negative Capacitance FETs
- Brief Introduction of Other Research Areas in My Group
  - Wide-Bandgap Semiconductors
  - Wireless Power Transfer
  - Brain-Computer Interface
- Challenges and Prospects

Wireless Power Transfer

Multiscale







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DOI: 10.1002/mmce.22291

INTERNATIONAL JOURNAL OF RF AND MICROWAVE COMPUTER-AIDED ENGINEERING WILEY

RESEARCH ARTICLE

New small-signal extraction method applied to GaN HEMTs on different substrates

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Abstract

In this article, a new extraction technique is proposed to extract the small-signal parameters of gallium nitride (GaN) high electron mobility transistors (HEMTs) on three different substrates namely, Si, SiC, and Diamond. This extraction technique used a single small-signal circuit model to efficiently describe the physical and electrical properties of GaN on different substrates. This technique takes into account any asymmetry between the gate-source and gate-drain capacitances on the asymmetrical GaN HEMT structure, charge-trapping effects, passivation layer inclusion, as well as leakage currents associated with the nucleation layer between the GaN buffer layer and the different substrates. The extracted values were then optimized using the grey wolf optimizer. The proposed technique was demonstrated through a close agreement between simulated and measured *S*-parameters.

KEYWORDS

diamond substrate, GaN HEMT, grey wolf optimizer, parameter extraction, small signal modeling

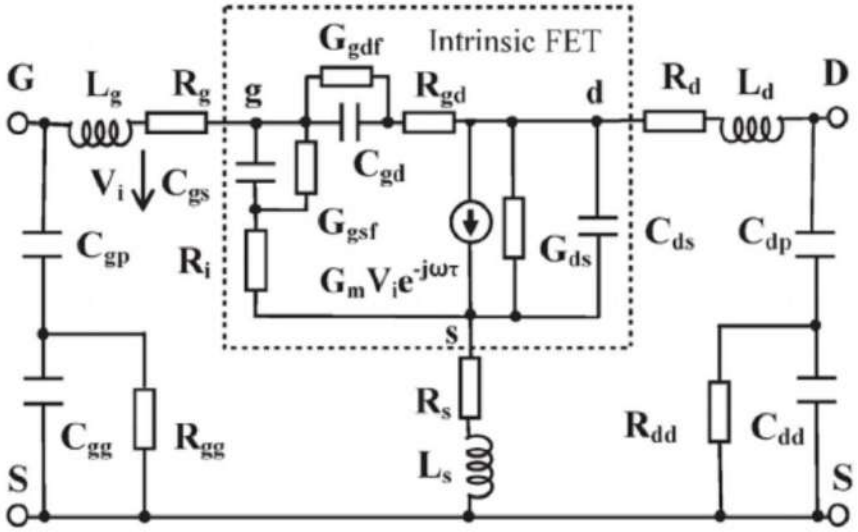

FIGURE 1 GaN HEMT equivalent circuit-small signal model (EC-SSM) including the substrate-buffer model[19]

scientific reports (2020) 10:22050

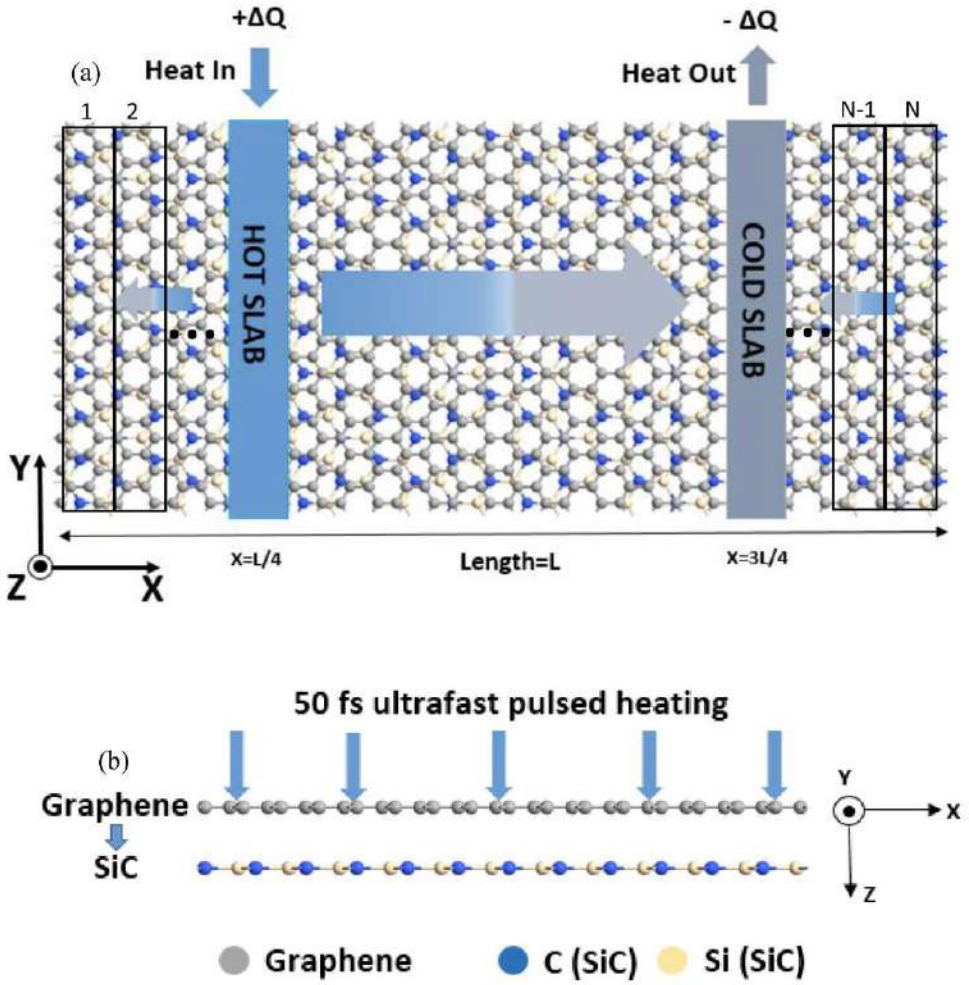

Figure 1. Atomic configuration of the graphene/2D-SiC van der Waals heterostructure (vdWH) used to calculate the (**a**) in-plane and (**b**) out-of-plane thermal conductivity. The $+\Delta Q$ amount of heat is applied to the hot slab (blue area) placed at the length of $X = L/4$ and $-\Delta Q$ amount of heat is extracted from the cold slab (gray area) placed at the length of $X = 3L/4$ in the x direction. Here, the blue to gray gradient arrow reflects the heat flow around the sheet length. A 50 fs ultra-fast heat impulse is applied to the graphene in the out-of-plane (z) direction to compute the interface thermal resistance.

Exceptional in-plane and interfacial thermal transport in graphene/2D-SiC van der Waals heterostructures

Md. Sherajul Islam[1]✉, Imon Mia[1], Shihab Ahammed[1], Catherine Stampfl[2] & Jeongwon Park[3,4]

Graphene based van der Waals heterostructures (vdWHs) have gained substantial interest recently due to their unique electrical and optical characteristics as well as unprecedented opportunities to explore new physics and revolutionary design of nanodevices. However, the heat conduction performance of these vdWHs holds a crucial role in deciding their functional efficiency. In-plane and out-of-plane thermal conduction phenomena in graphene/2D-SiC vdWHs were studied using reverse non-equilibrium molecular dynamics simulations and the transient pump-probe technique, respectively. At room temperature, we determined an in-plane thermal conductivity of ~ 1452 W/m-K for an infinite length graphene/2D-SiC vdWH, which is superior to any graphene based vdWHs reported yet. The out-of-plane thermal resistance of graphene → 2D-SiC and 2D-SiC → graphene was estimated to be 2.71×10^{-7} km^2/W and 2.65×10^{-7} km^2/W, respectively, implying the absence of the thermal rectification effect in the heterobilayer. The phonon-mediated both in-plane and out-of-plane heat transfer is clarified for this prospective heterobilayer. This study furthermore explored the impact of various interatomic potentials on the thermal conductivity of the heterobilayer. These findings are useful in explaining the heat conduction at the interfaces in graphene/2D-SiC vdWH and may provide a guideline for efficient design and regulation of their thermal characteristics.

SiC related works from our group (2020-2022)

1. Two-dimensioTwo-dimensional SiC/AlN based type-II van der Waals heterobilayer: A promising photocatalyst for overall water disassociation, Naim Ferdous, Md. Sherajul Islam, Jeshurun Biney, Catherine Stampfl & Jeongwon Park **(Nature) Scientific Reports,** 12, 20106 (2022) (Impact Factor: 4.996)
2. Temperature and interlayer coupling induced thermal transport across graphene/2D-SiC van der Waals heterostructure, Md. Sherajul Islam, Imon Mia, A. S. M. Jannatul Islam, Catherine Stampfl, and Jeongwon Park **(Nature) Scientific Reports, 12**, 761 (2022) https://www.nature.com/articles/s41598-021-04740-4 (Impact Factor: 4.996)
3. Superior tunable photocatalytic properties for water splitting in two- dimensional GeC/SiC van der Waals hetero-bilayers, Islam, Md, Abu Farzan Mitul, Md Mojumder, Rayid Hasan, A. S. M. Islam, Catherine Stampfl, and Jeongwon Park, **(Nature) Scientific Reports,** 11.1, 1-14 (2021) https://www.nature.com/articles/s41598-021-97251-1 (Impact Factor: 4.996)
4. Exceptional In-Plane and Interfacial Thermal Conductivity in Graphene/2D-SiC van der Waals Heterostructure, Md. Sherajul Islam, Imon Mia, Shihab Ahammed, Catherine Stampfl and Jeongwon Park, **(Nature) Scientific Reports**, 10, 22050 (2020) https://www.nature.com/articles/s41598-020-78472-2 (Impact Factor: 4.996)
5. Germanene/2D-SiC van der Waals heterobilayer: structural features and tunable electronic properties, Md Sherajul Islam, Md. Rayid Hasan Mojumder; Naim Ferdous; Jeongwon Park, **Materials Today Communications,** 101718 (2020) https://doi.org/10.1016/j.mtcomm.2020.101718 (Impact Factor: 2.678)
6. Lateral and flexural thermal transport in stanene/2D-SiC van der Waals heterostructure, Shihab Ahammed, Md. Sherajul Islam, Imon Mia, Jeongwon Park, **Nanotechnology,** 31, 505702 (2020) https://doi.org/10.1088/1361-6528/abb491 (Impact Factor 3.399)

Scanning microwave imaging of optically patterned $Ge_2Sb_2Te_5$

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View Online Export Citation

Scott R. Johnston,[1] Edwin Ng,[1] Scott W. Fong,[2] Walter Y. Mok,[3] Jeongwon Park,[3,4] Peter Zalden,[3,5] Anne Sakdinawat,[3] H.-S. Philip Wong,[2] Hideo Mabuchi,[1] and Zhi-Xun Shen[1,6,a)]

AFFILIATIONS

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[5]European XFEL, Holzkoppel 4, 22869 Schenefeld, Germany
[6]Department of Physics, Stanford University, Stanford, California 94305, USA

[a)]Electronic mail: zxshen@stanford.edu

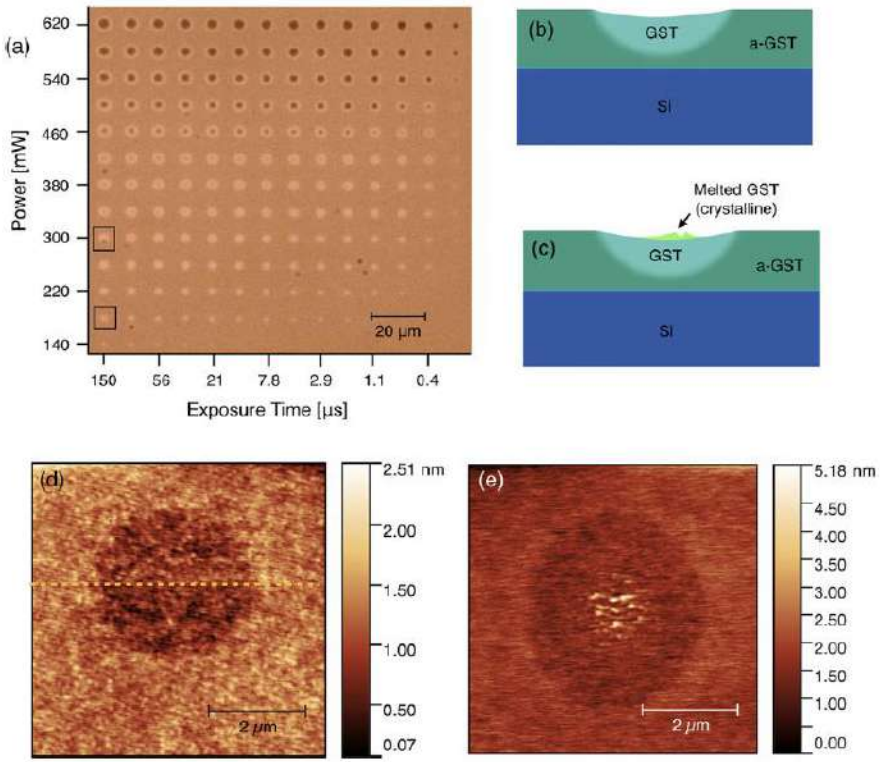
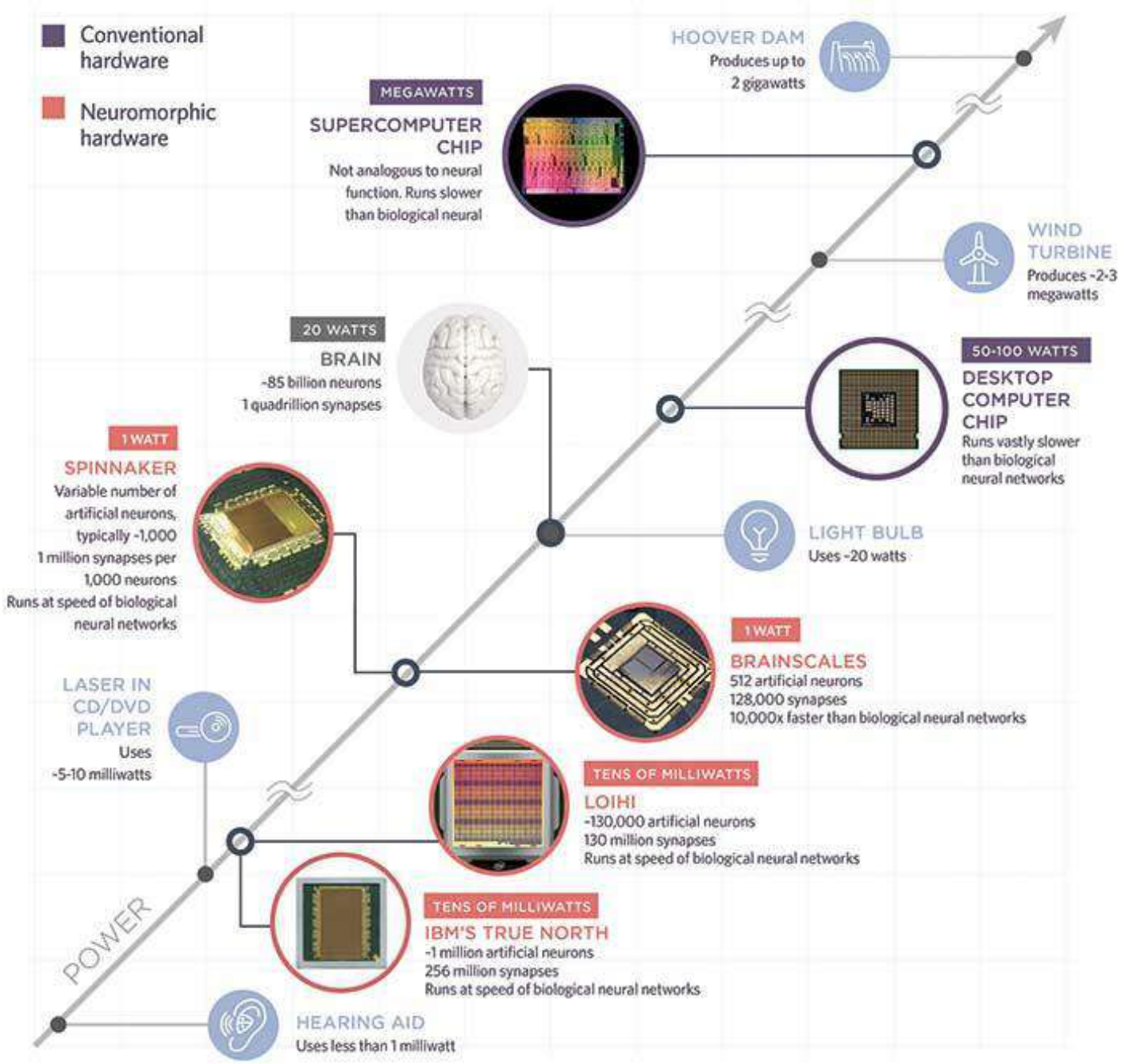


FIG. 1. (a) Optical microscopy image of the optically patterned 40 nm a-GST film. (b) Illustration of the crystallized region created by low-power patterning. (c) Illustration of melting at higher power. (d) and (e) AFM topography measurements at 180 mW, 300 mW, and 150 μs, as marked in (a).

ABSTRACT

The measurement of inhomogeneous conductivity in optically crystallized, amorphous $Ge_2Sb_2Te_5$ (GST) films is demonstrated via scanning microwave impedance microscopy (MIM). Qualitative consistency with expectations is demonstrated in spots crystallized by focused coherent light at various intensities, exposure times, and film thicknesses. The characterization of process imperfections is demonstrated when a mask is used to optically pattern the nanoscale features of crystalline GST in the amorphous film. These measurements show the ability of MIM to resolve partial crystallization, patterning faults, and other details in optically patterned GST.

Power dissipation of neuromorphic and conventional hardware with respect to the human brain

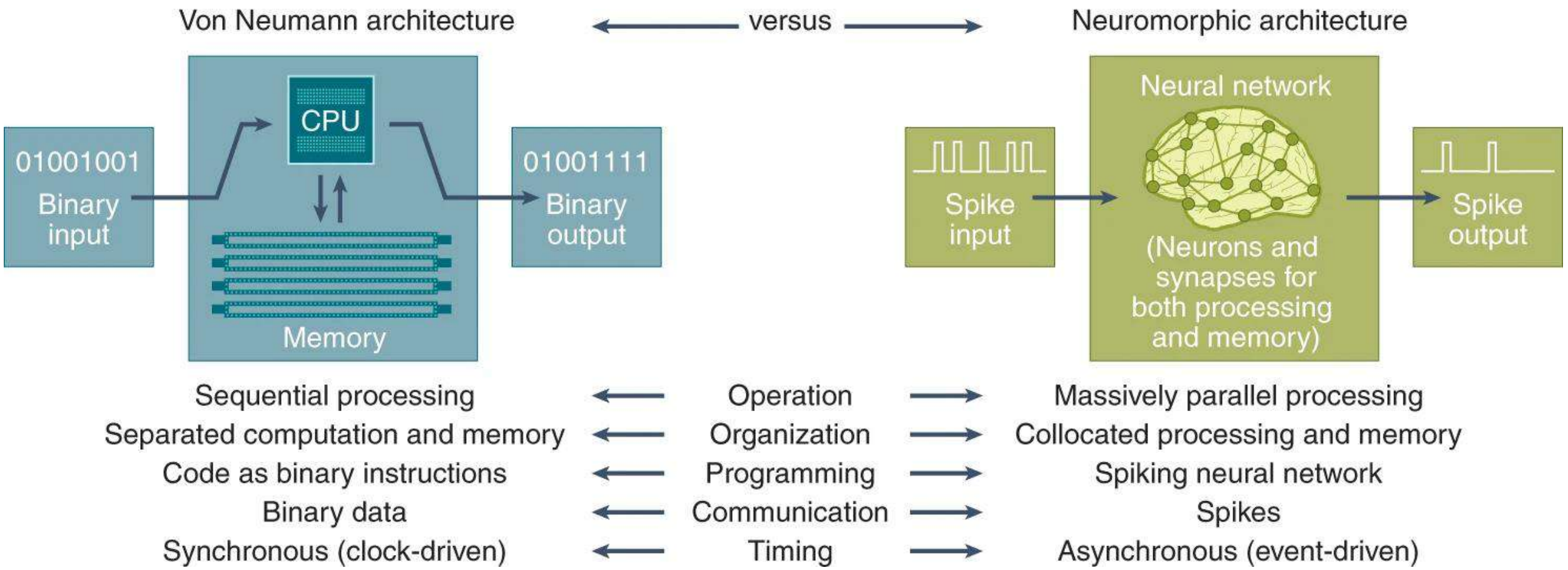


Note the power consumed by state-of-the-art supercomputing chips is orders of magnitude higher than neuromorphic computing chips

(Source: S. Ravindran, "Infographic: Brain-like computers provide more computer power.").

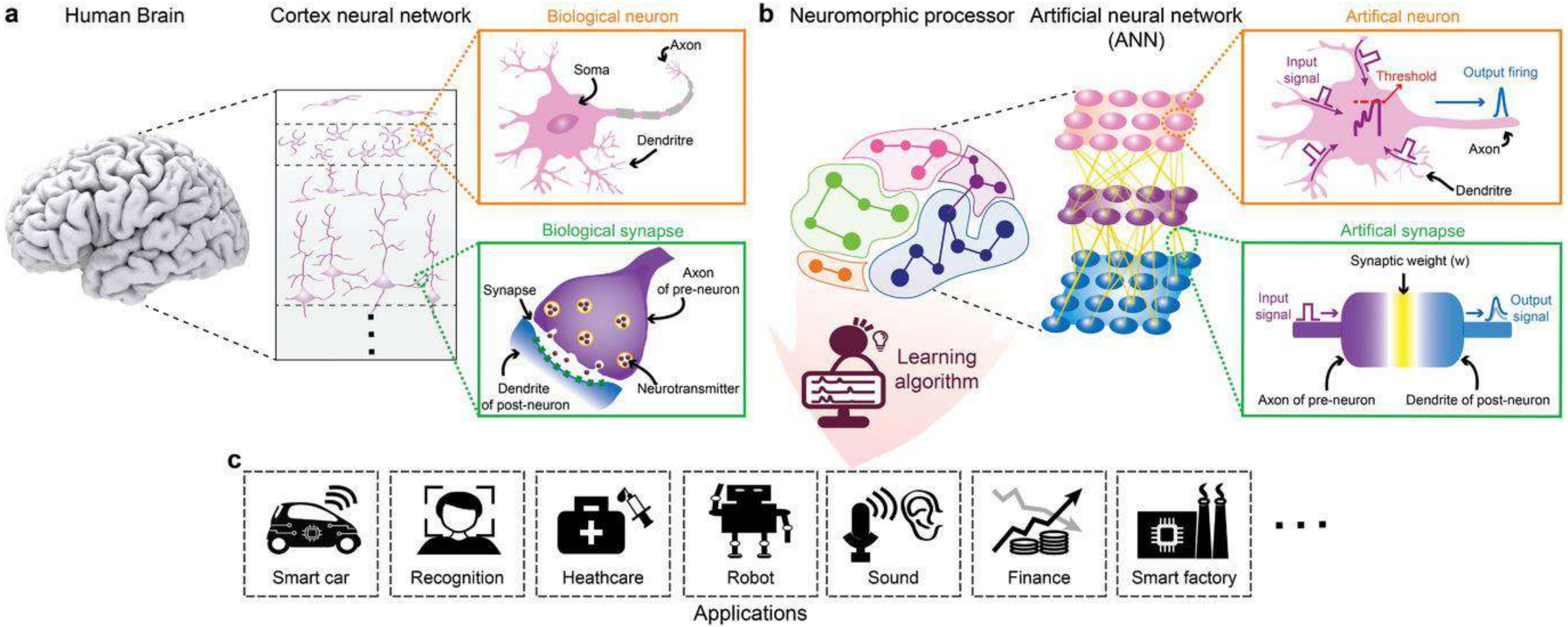
https://raksha-anirveda.com/a-perspective-on-neuromorphic-computing/

What Is Neuromorphic Computing?



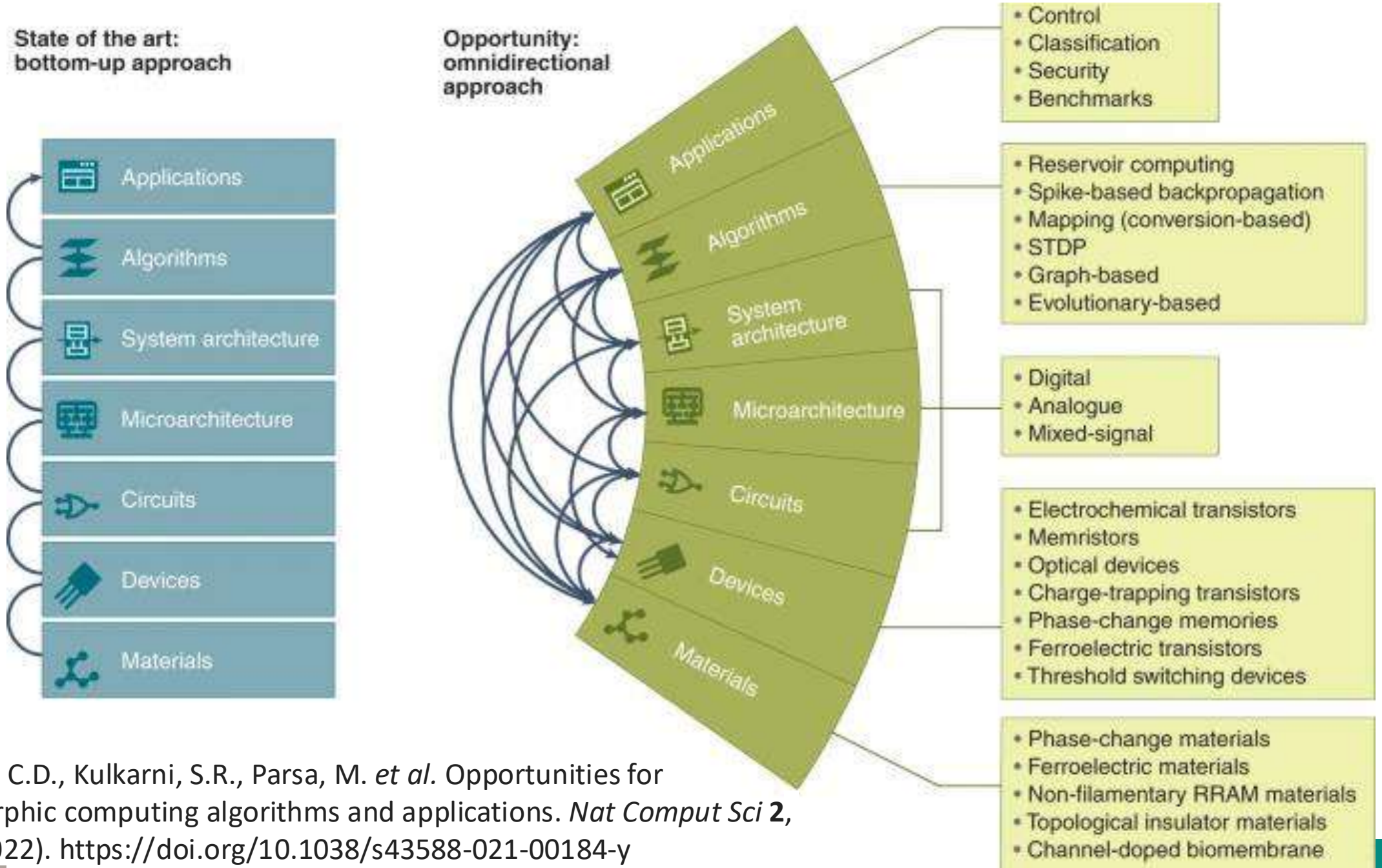
Schuman, C.D., Kulkarni, S.R., Parsa, M. *et al.* Opportunities for neuromorphic computing algorithms and applications. *Nat Comput Sci* **2**, 10–19 (2022). https://doi.org/10.1038/s43588-021-00184-y

Emerging Memristive Artificial Synapses and Neurons for Energy-Efficient Neuromorphic Computing



Advanced Materials, Volume: 32, Issue: 51, First published: 01 October 2020, DOI: (10.1002/adma.202004659)

Opportunity for full compute stack co-design in neuromorphic computers



Schuman, C.D., Kulkarni, S.R., Parsa, M. *et al.* Opportunities for neuromorphic computing algorithms and applications. *Nat Comput Sci* **2**, 10–19 (2022). https://doi.org/10.1038/s43588-021-00184-y

Challenges of Neuromorphic Computing

While neuromorphic computing has the potential to revolutionize applications of artificial intelligence, data analysis and even our understanding of human cognition, its development faces several challenges.

- Has no standard benchmarks for performance assessment
- Limited hardware and software availability
- Difficult to learn and apply
- Reduced precision and accuracy in comparison to similar neural networks

No Benchmarks or Standardization

- Because neuromorphic computing is still a relatively new technology, there are no standard benchmarks for it, making it difficult to assess its performance and prove its efficacy outside of a research lab.
- The lack of standardized architectures and software interfaces for neuromorphic computing can also make it difficult to share applications and results.
- However, there is a “big push” among academic and industry leaders to change this.

Biomedical Engineering Letters (2022) 12:303–316
https://doi.org/10.1007/s13534-022-00226-y

REVIEW ARTICLE

Deep brain stimulation for Parkinson's Disease: A Review and Future Outlook

Anahita Malvea[1] · Farbod Babaei[2] · Chadwick Boulay[3,4] · Adam Sachs[3,4,5] · Jeongwon Park[2,6]

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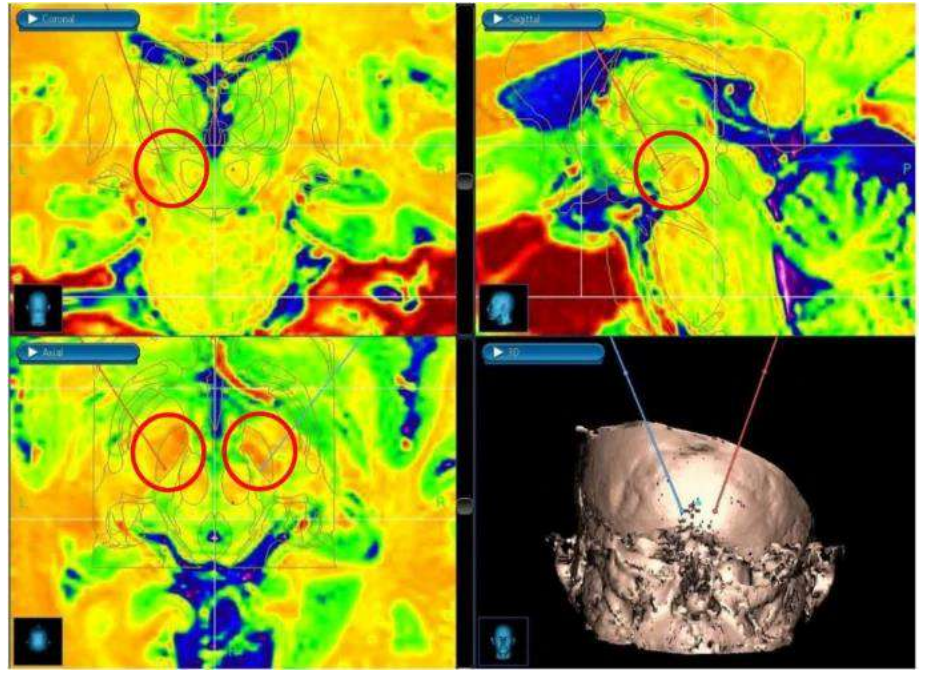
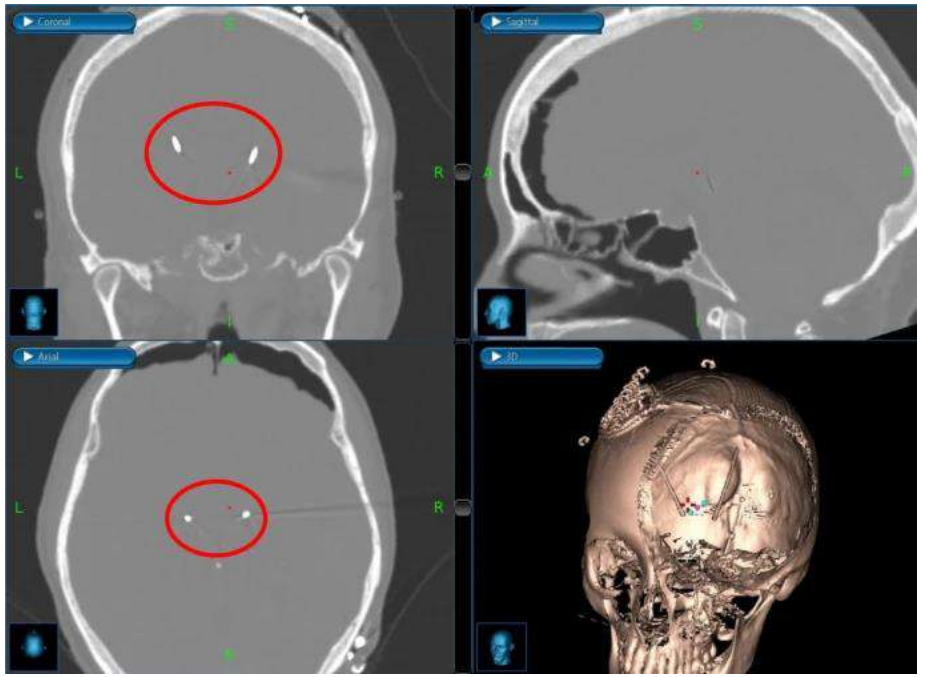
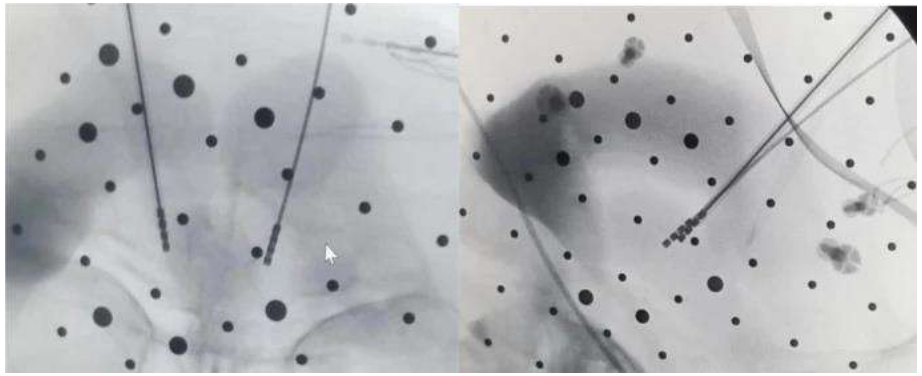
Abstract

Parkinson's Disease (PD) is a neurodegenerative disorder that manifests as an impairment of motor and non-motor abilities due to a loss of dopamine input to deep brain structures. While there is presently no cure for PD, a variety of pharmacological and surgical therapeutic interventions have been developed to manage PD symptoms. This review explores the past, present and future outlooks of PD treatment, with particular attention paid to deep brain stimulation (DBS), the surgical procedure to deliver DBS, and its limitations. Finally, our group's efforts with respect to brain mapping for DBS targeting will be discussed.

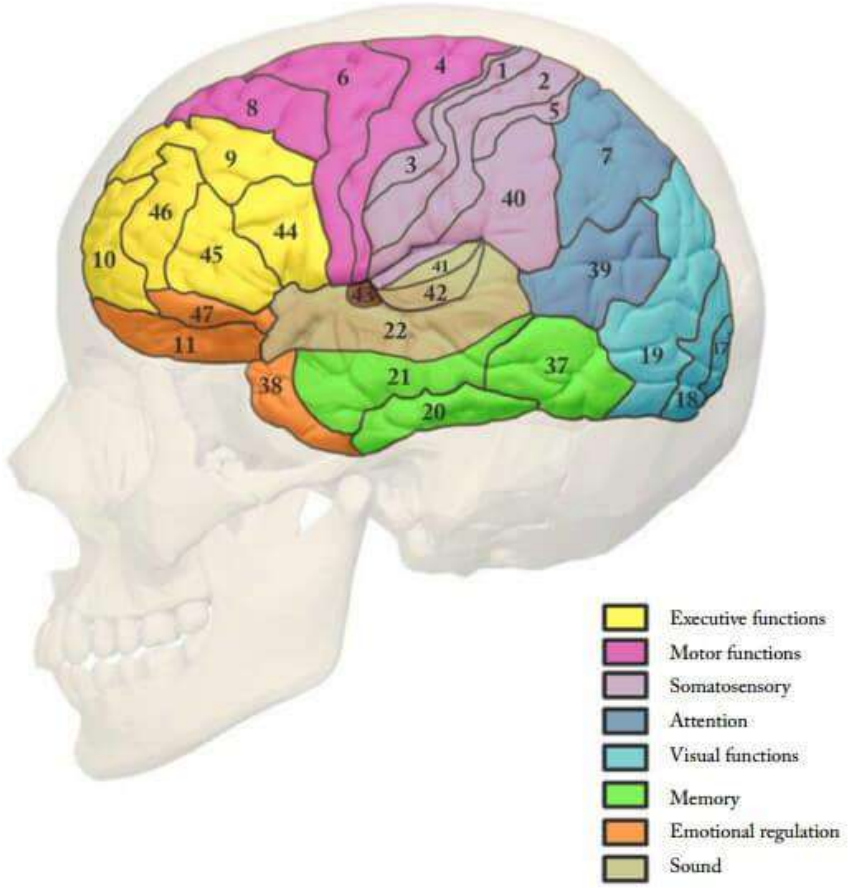


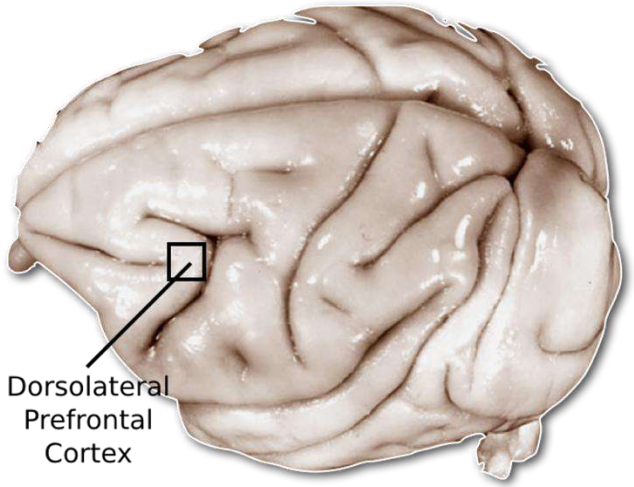


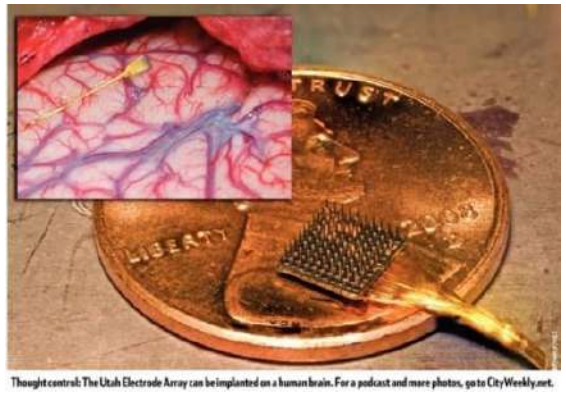


Recurrent Neural Networks to Model Neural Dynamics and Decode Intended Saccades in Prefrontal Cortex

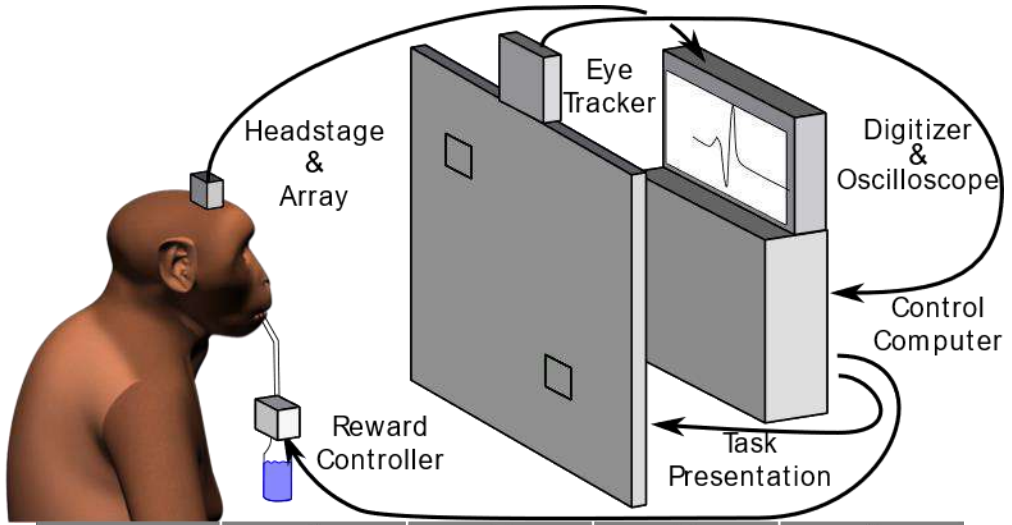
- The Recorded Area in Brain

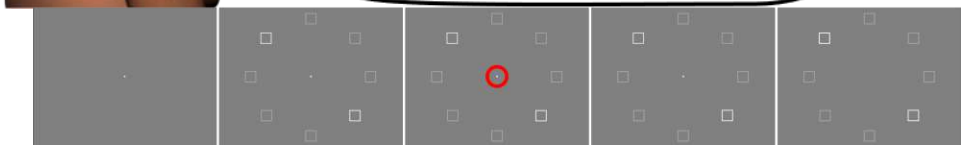




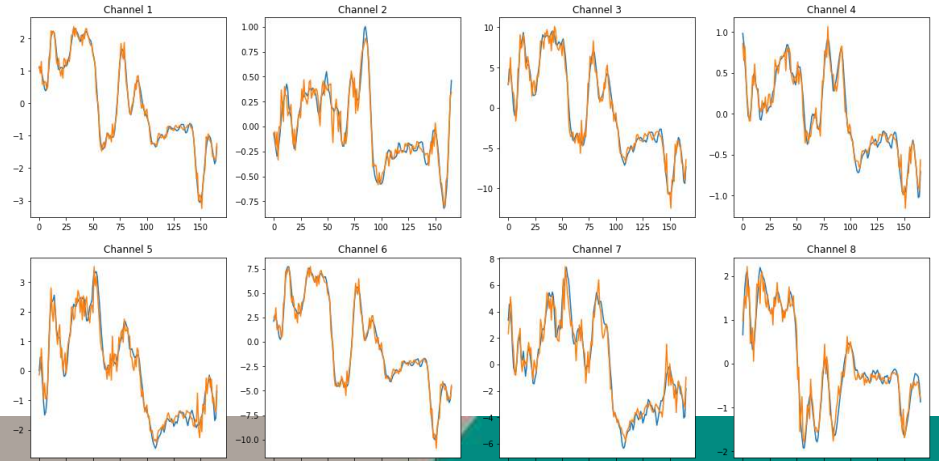

Thought control: The Utah Electrode Array can be implanted on a human brain. For a podcast and more photos, go to CityWeekly.net.

- The Behavioural Task






First 8 Channels of Reconstructed Neural Activity and RNN Activations in Original Space

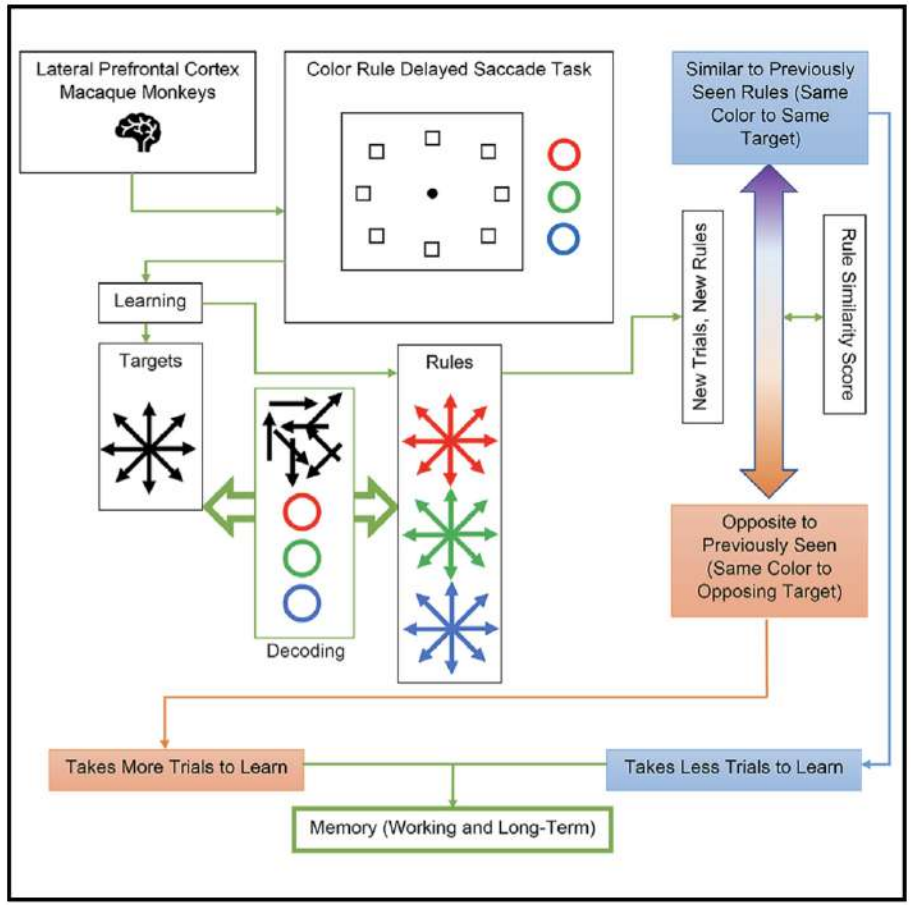


Article

Cell Reports

Ensembles code for associative learning in the primate lateral prefrontal cortex

Graphical abstract



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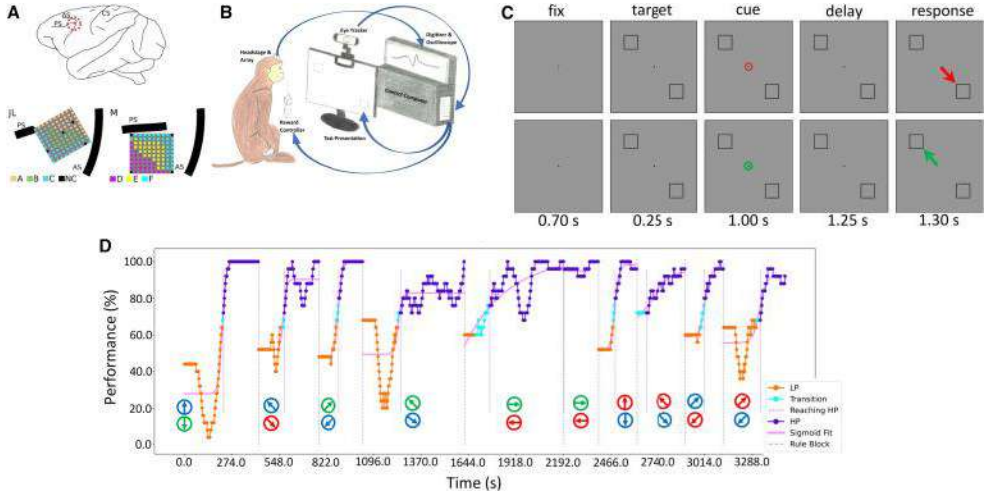
In brief

The study investigated how stimulus-response associations are encoded in lateral prefrontal cortex of the brain in a learning task using working and long-term memory. The recorded neuronal activities change after learning the associations, and in a low-dimensional space, similar associations occupy closer subspaces.

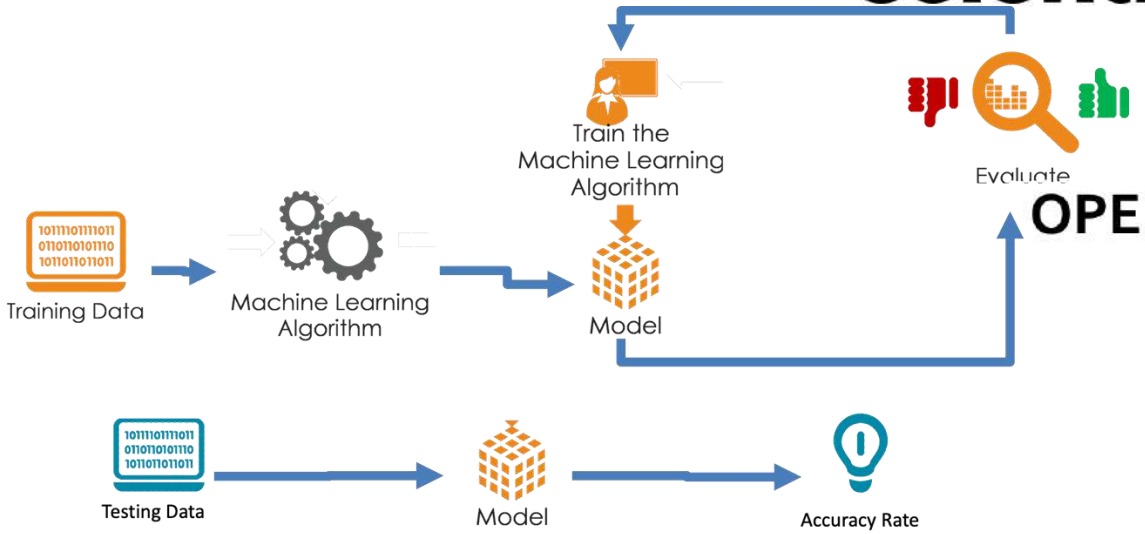


Rouzitalab et al., 2023, Cell Reports 42, 112449
May 30, 2023
https://doi.org/10.1016/j.celrep.2023.112449

scientific reports

Siraj Ahmed et al., Scientific Reports, 12, 21469 (2022)

OPEN



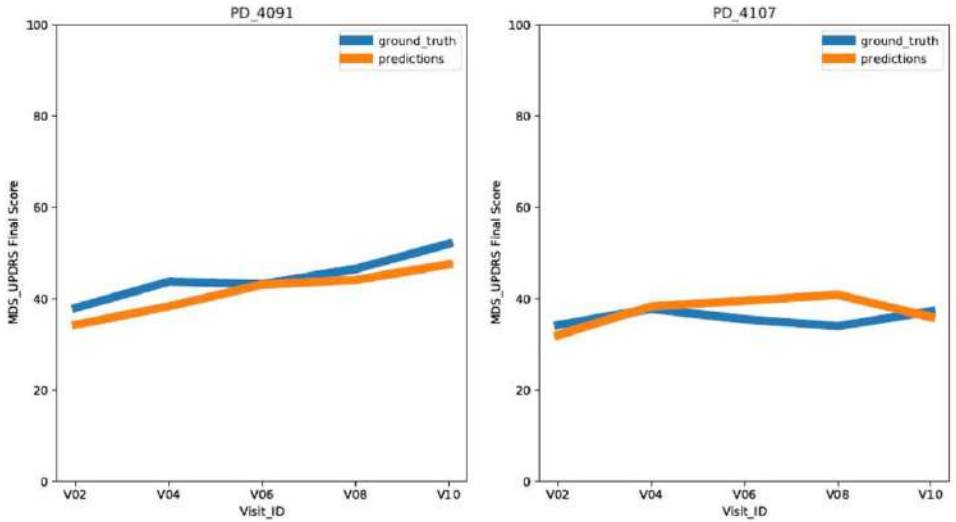


Figure 6. Predicted and Ground Truth disease progression curves for Test Patients. Each subplot belongs to one test patient. The curve in blue is the ground truth curve and the curve in orange is the one predicted by our Predictive Model. The x-axis has discrete visit points of 6 months(V02), 12 months (V04), 24 months (V06), 36 months (V08), 48 months (V10) and the y-axis has the MDS-UPDRS score for the patient.

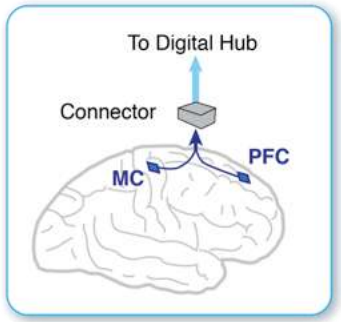
Predictive modelling of Parkinson's disease progression based on RNA-Sequence with densely connected deep recurrent neural networks

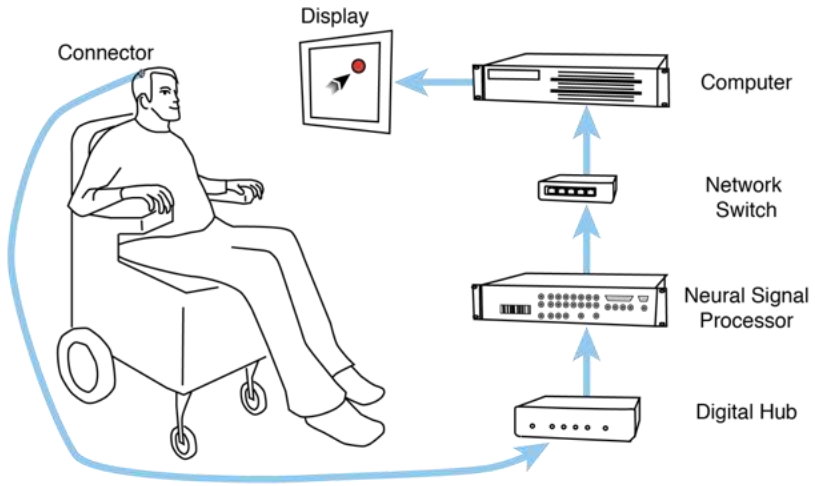
Siraj Ahmed[1], Majid Komeili[2]✉ & Jeongwon Park[1,3]✉

The advent of recent high throughput sequencing technologies resulted in unexplored big data of genomics and transcriptomics that might help to answer various research questions in Parkinson's disease (PD) progression. While the literature has revealed various predictive models that use longitudinal clinical data for disease progression, there is no predictive model based on RNA-Sequence data of PD patients. This study investigates how to predict the PD Progression for a patient's next medical visit by capturing longitudinal temporal patterns in the RNA-Seq data. Data provided by Parkinson Progression Marker Initiative (PPMI) includes 423 PD patients without revealing any race, sex, or age information with a variable number of visits and 34,682 predictor variables for 4 years. We propose a predictive model based on deep Recurrent Neural Network (RNN) with the addition of dense connections and batch normalization into RNN layers. The results show that the proposed architecture can predict PD progression from high dimensional RNA-seq data with a Root Mean Square Error (RMSE) of 6.0 and a rank-order correlation of ($r = 0.83$, $p < 0.0001$) between the predicted and actual disease status of PD.

Future Research

- Integrating PFC in BCI Studies
- Advancing the PD Treatment





- Neuro Cognitive Communicator
- Synergistic utilization of multiple cortical areas

- Triggered Deep Brain Stimulation (DBS)
- Effects of Modulations On Symptoms
- Therapeutic Closed Loop BCI for PD

A. Rouzitalab, C. B. Boulay, J. Park, J. C. Martinez-Trujillo, and A. J. Sachs, “Ensembles code for associative learning in the primate lateral prefrontal cortex”, **Cell Reports**, vol. 42, no. 5, May 2023, doi: 10.1016/j.celrep.2023.112449.

UNR Davidson Foundation Cleanroom

Workspace: 3,000 ft^2

Mask aligner

CVD: 2D Materials

E-beam evaporator

Image Source: University of Nevada, Reno

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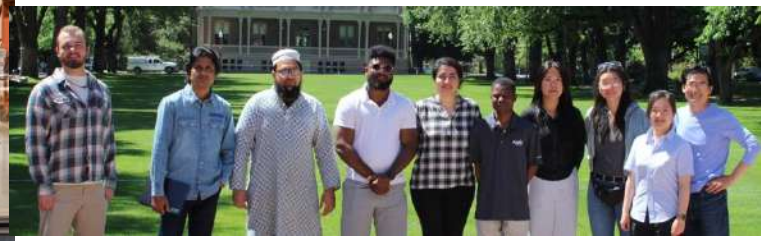

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