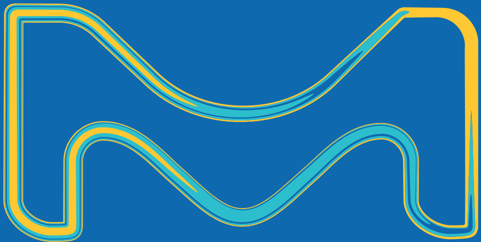
The Electronics business of Merck KGaA, Darmstadt, Germany operates as EMD Electronics in the U.S. and Canada.

Thermal Atomic Layer Etch

A Critical Tool for Logic and Memory Downscaling

Martin E. McBriarty, PhD (he/him)

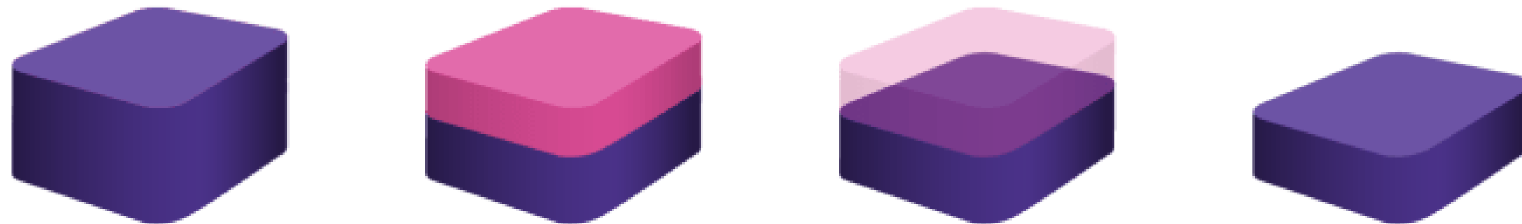
martin.mcbriarty@emdgroup.com
April 11, 2024



EMD ELECTRONICS

Thermal Atomic Layer Etch
Agenda

1. **Background**
   - *Growing Complexity of 3D Devices*
   - *Semiconductor Etches*
   - *How ALE Works*
2. **ALE of Metals: Cu, Co, Mo, W, Ni**
3. **ALE of Metal Oxides: ZrO_2, HfO_2**
4. **Outlook**

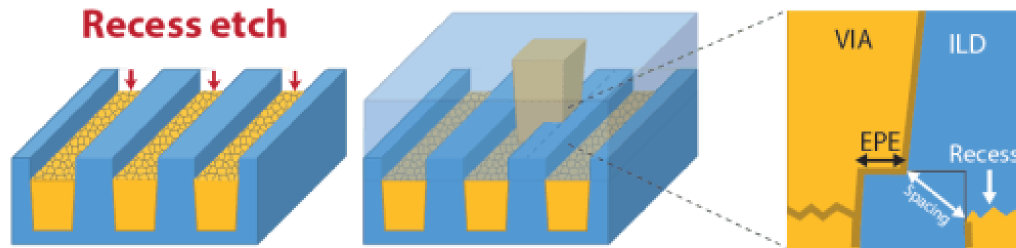


Background: 3D Devices & Etches

01

Logic (BEOL)

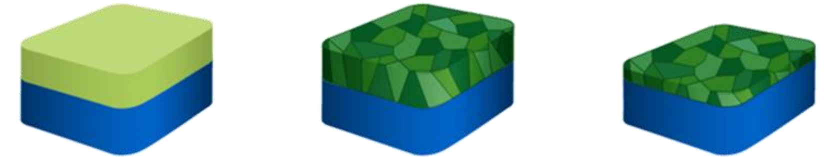
Fully Self-Aligned Via (FSAV)



A. Mackus, AtomicLimits (2019)

DRAM

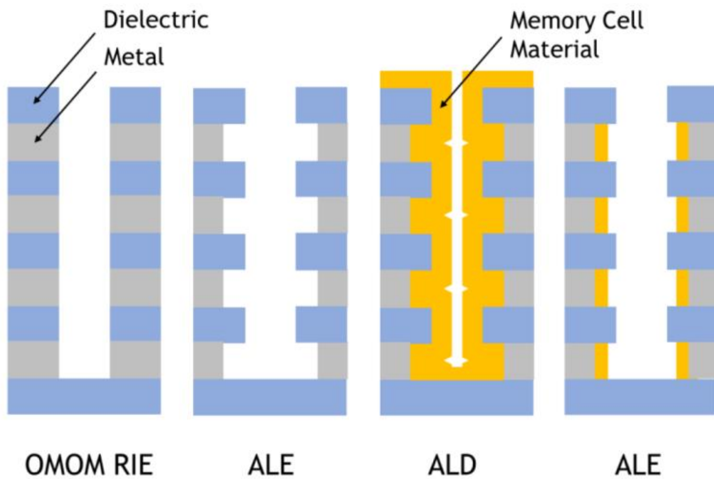
High-*k* Dielectric Thinning



M. McBriarty, AtomicLimits (2022)

3D Memory

Excess Material Removal and Recess

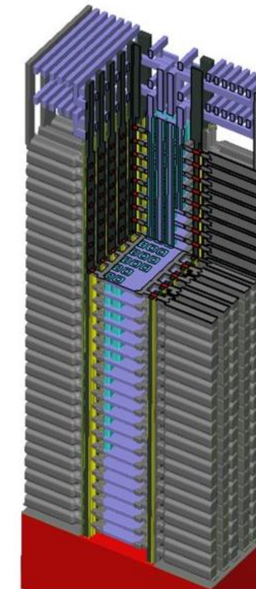


A. Fischer et al., JVSTA 39 (2021) 030801

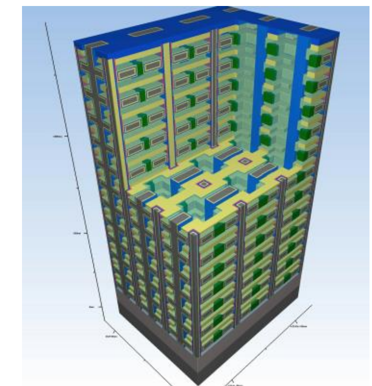
Shaping devices in complex 3D nano-architectures requires **selective, isotropic (conformal) etches**

3D DRAM

Complex Stacked Structures, Novel Materials



B. Vincent, Lam Research (2023)



A. Furnemont, imec (2022)

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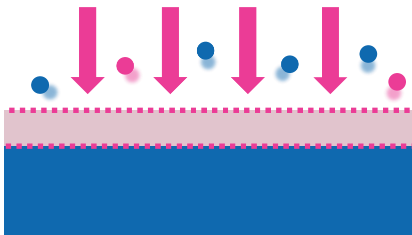
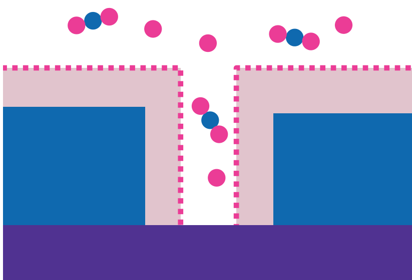
Etches & Cleans in Semiconductor Fabrication

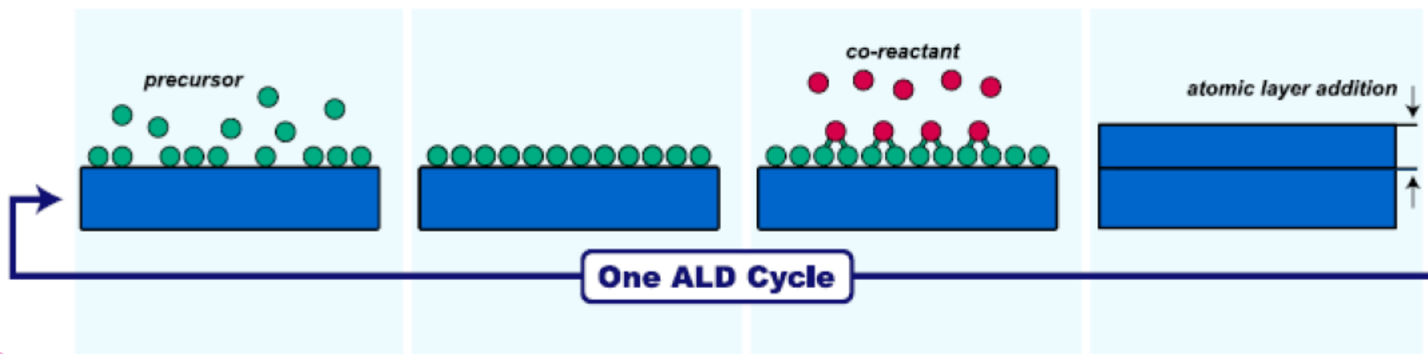


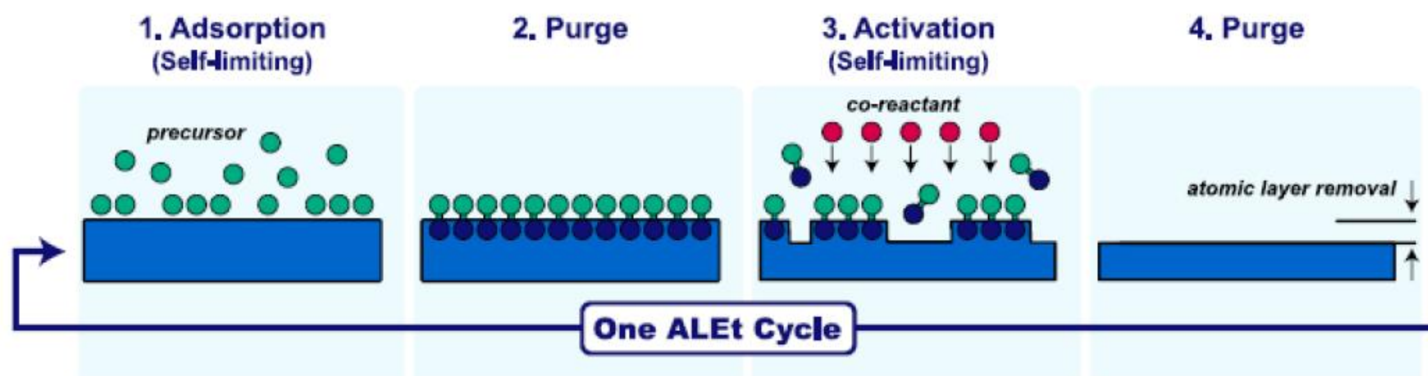


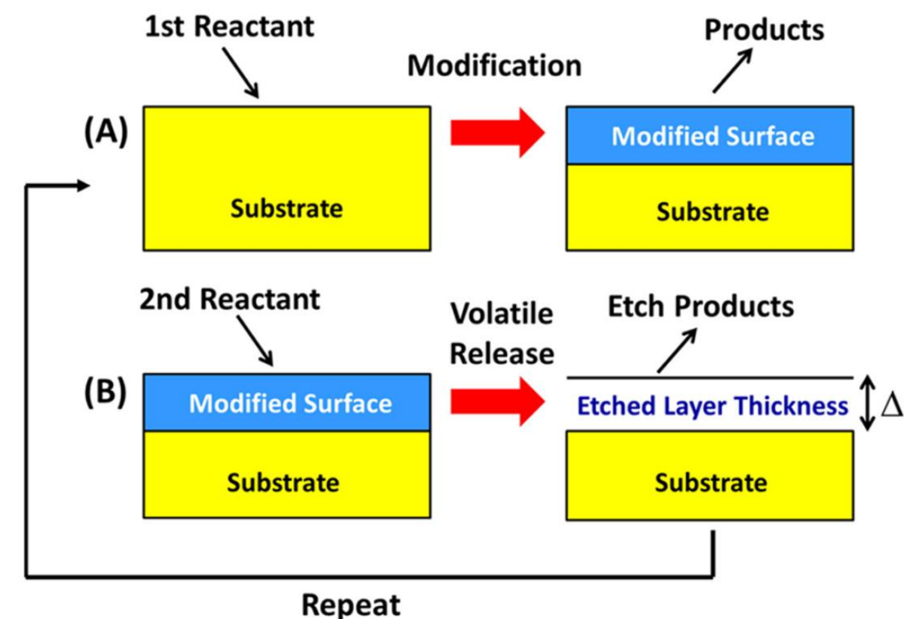
Method	Etch Rate	Selectivity	Conformality
Wet Etches & Cleans	~1 – 10^3 nm/min	Good	Limited at high AR / low CD
Plasma Etching & Reactive Ion Etching (RIE)	~10 – 10^4 nm/min	Moderate damage to non-etched surfaces	Poor
Atomic Layer Etch (ALE)	~0.1 - 1 nm/min	Good	Good (thermal ALE)

ALE is the best method for *precise, selective etch* in complex 3D nanostructures

ALE is the “reverse” of Atomic Layer Deposition (ALD)







S.M. George, Acc. Chem. Res 53 (2020) 1151

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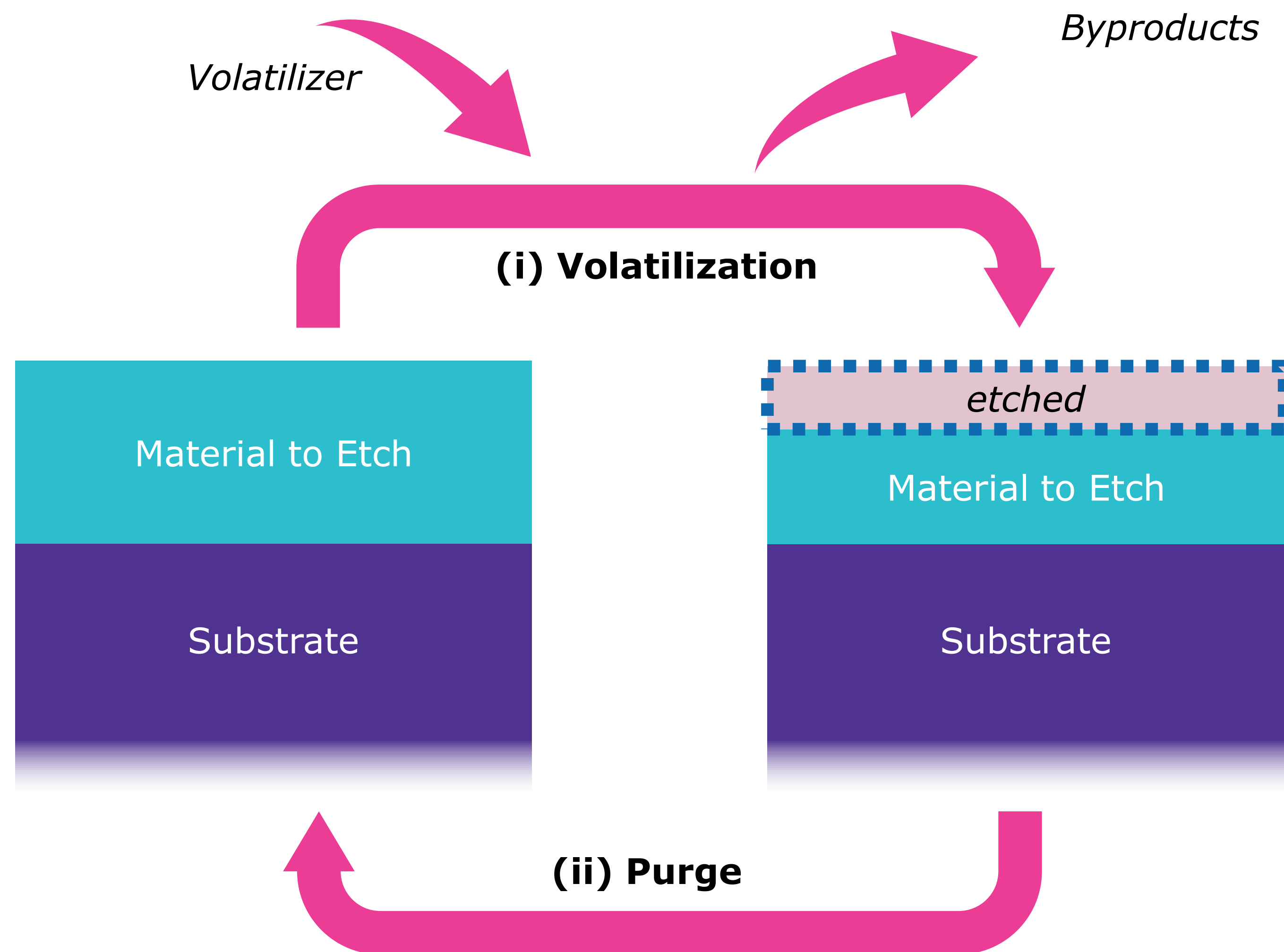
Vapor-Phase Etch by Thermal Volatilization
Making Volatile Metal Complexes at the Surface

Volatilizers are vapor-phase chemical etchants

The volatilizer selectively removes one material without affecting other materials

Vapor-phase selective etch for surface cleans and native oxide removal is sometimes called "atomic layer cleaning" (ALC)

Can be continuous etch or cycled



Thermal Atomic Layer Etch
Controlling Selective Etch Using Surface Modification

Surface modifiers convert a thin surface layer of a material (<1nm) into a different compound:

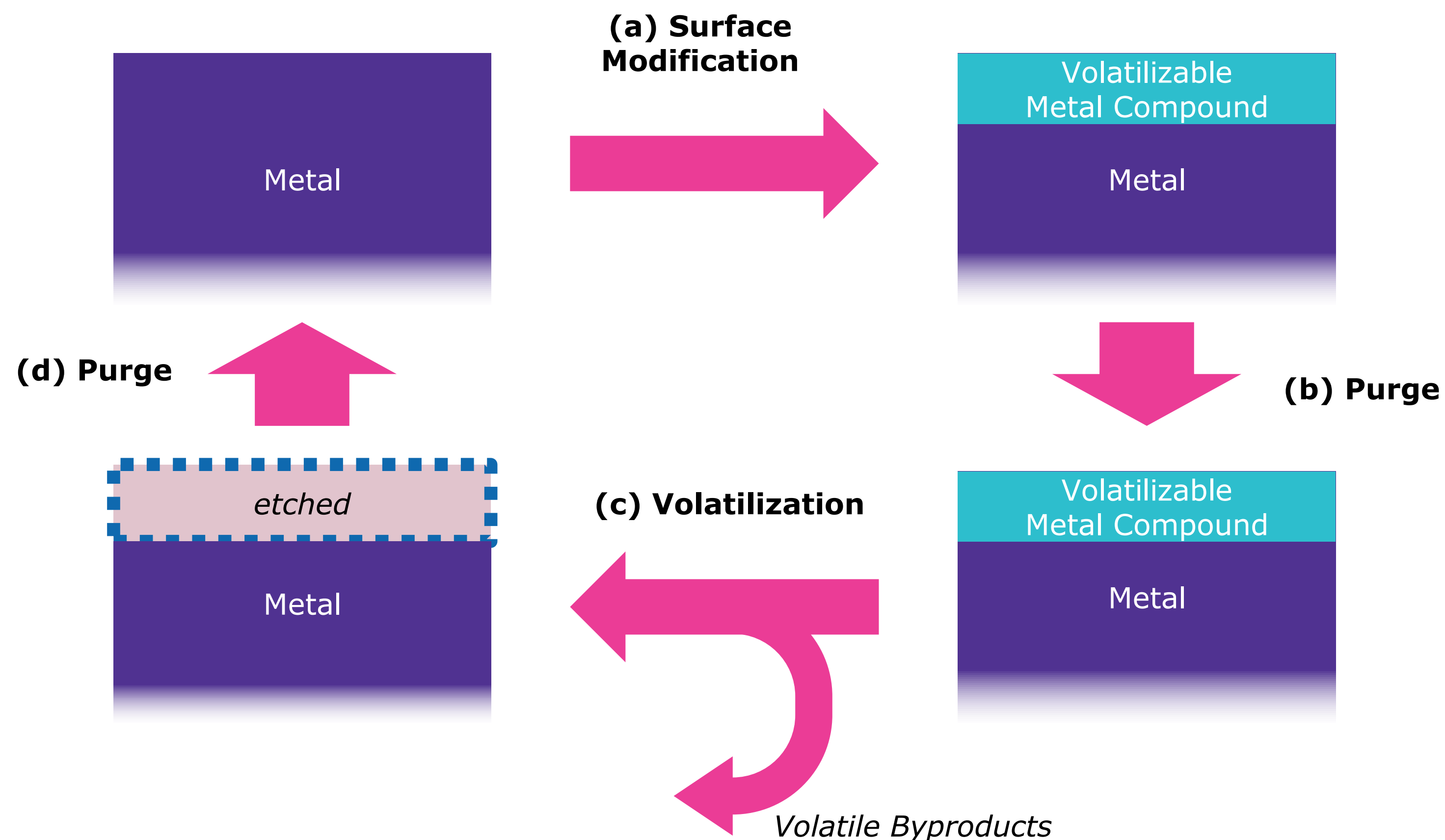
- Metals → metal oxides or halides
- Metal oxides → metal halides

After a purge, the **volatilizer** selectively etches the modified surface material

This ALE sequence is cycled to remove the desired thickness of material (a few nm)

Plasmas may be used for surface modification and/or volatilization, if geometry allows

Example Thermal ALE Process for a Metal:



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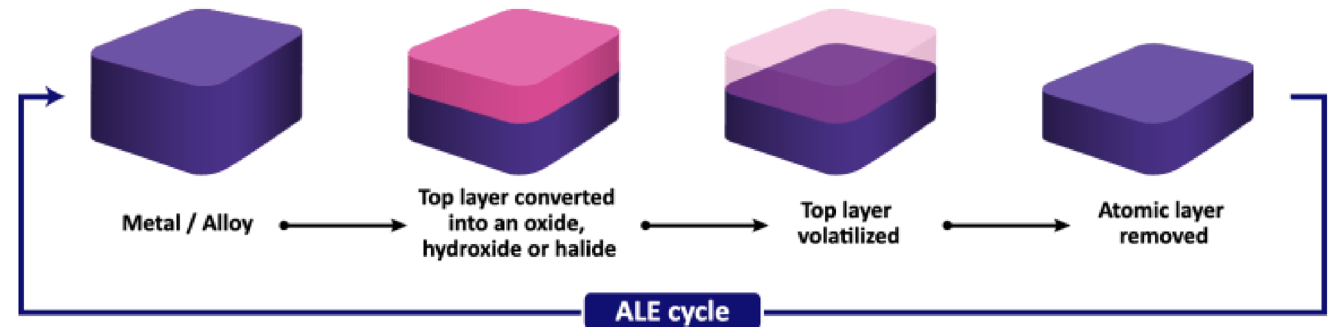

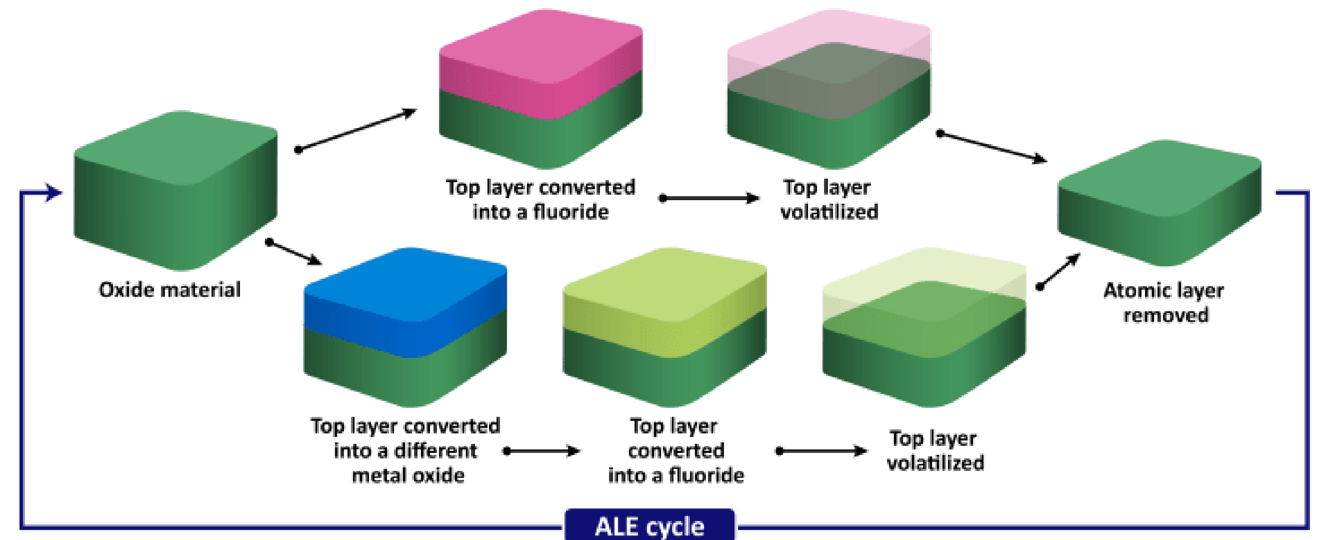

M. McBriarty, AtomicLimits.com (2022)

https://www.atomiclimits.com/2022/02/03/atomic-layer-etch-carves-the-path-to-more-efficient-computing/

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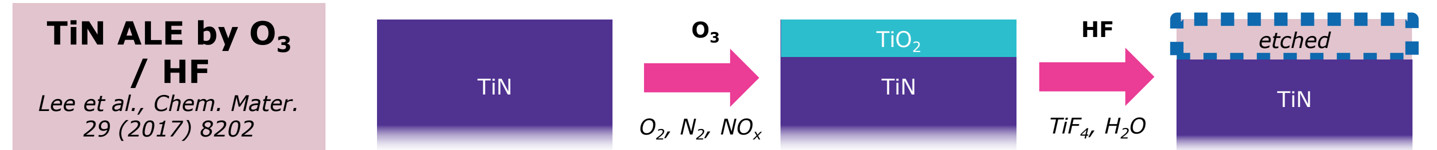
Classification: Public

Thermal Atomic Layer Etch: Examples

Controlling Selective Etch Using Surface Modification



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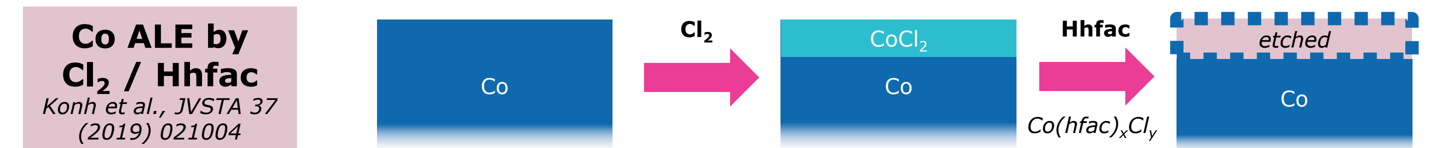

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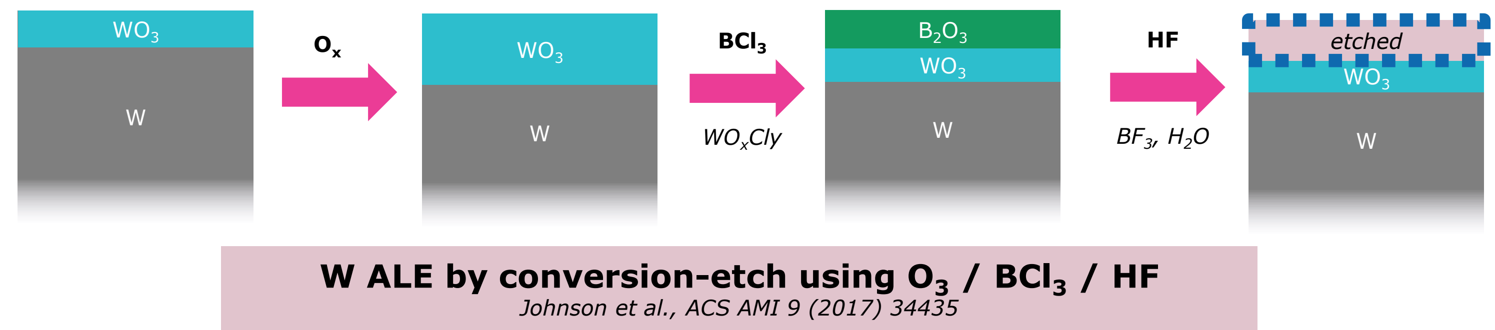

Thermal Atomic Layer Etch
Isotropic Etch by Kinetic Control

When conformal etch is needed, the surface modification reaction **must be self-limiting**

Thermal ALE enables **atomically precise etch** in 3D nano-architectures:

- Trenches
- Vias
- Lateral openings

Trench structure

Poor kinetic control of the ALE process

Etch per cycle

Dose time

Good kinetic control of the ALE process

Etch per cycle

Dose time

M.E. McBriarty. Atomic Layer Etch Carves the Path to More Efficient Computing. ***2022****. AtomicLimits.*

EMD Electronics covers nearly all aspects of semiconductor manufacturing

How do ALE & related techniques fit in?

Deposition

Patterning

Planarization

Chip Design

Prototyping and Testing

Packaging

Module Assembly

End Use

Doping

Etching

Cleaning

EMD Electronics covers nearly all aspects of semiconductor manufacturing

How do ALE & related techniques fit in?

Chip Design → Prototyping and Testing → [Patterning, Deposition, Planarization, Etching, Cleaning, Doping] → Packaging → Module Assembly → End Use

Deposition: *Cleanup of nuclei on non-growth surface*

Patterning: *Hard mask shaping & smoothing*

Packaging: *Contact recess for hybrid bonding*

Etching: *High aspect ratio / low critical dimension etches*

Cleaning: *Removal of residues and native oxides*

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Intermolecular: EMD's Silicon Valley Science Hub

Capabilities at-a-glance

Deposition Systems

- AP30 cluster platform
- ALD: 300mm
- PVD: 200 & 300mm

Integration (Wet cleans & Anneals)

- Wet: Clean etch, deposition
- Single Wafer Clean: 300mm
- Wet-bench: 300mm
- Anneal: Coupons → 300mm

Lithography & Etch

- Contact lithography (up to 8”), coat, exposure, develop & etch
- Oxide and metal etch
- Electron beam lithography

Informatics

- Substrate management
- Automated data collection & materials database
- Automated analysis

Physical, Optical, & X-ray Characterization

- XRF, XRR, XRD, XPS
- Ellipsometry, UV-Vis, FTIR
- Optical microscopy
- Spectrophotometry
- SEM, AFM, contact angle
- Particles (SP1)
- Nanoindentation
- TEM, Auger, SIMS, TXRF, ICPMS*

Electrical Characterization & E-Test

- Variable temperature chucks
- C-V, I-V, P-V & parameter extraction
- Leakage, line resistance, contact resistance, capacitance
- Radiant ferroelectric tester
- V_{bd} TDDB
- Pulse switching: I_{on}, I_{off}, data retention (e.g. Non-volatile memory)
- Internal Photoemission Spectroscopy & KPFM

ALE of Metals

02

Metal ALE for Logic: Fully Self-Aligned Via (FSAV)
Controlled Selective Etch for <10nm Interconnects

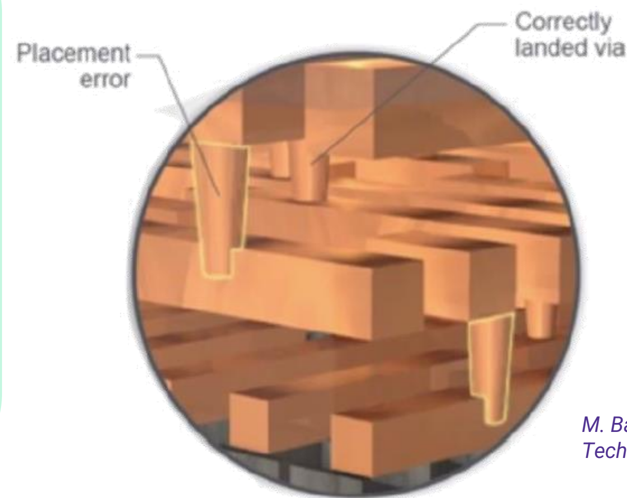
Smaller transistors need **smaller metal lines** to connect them

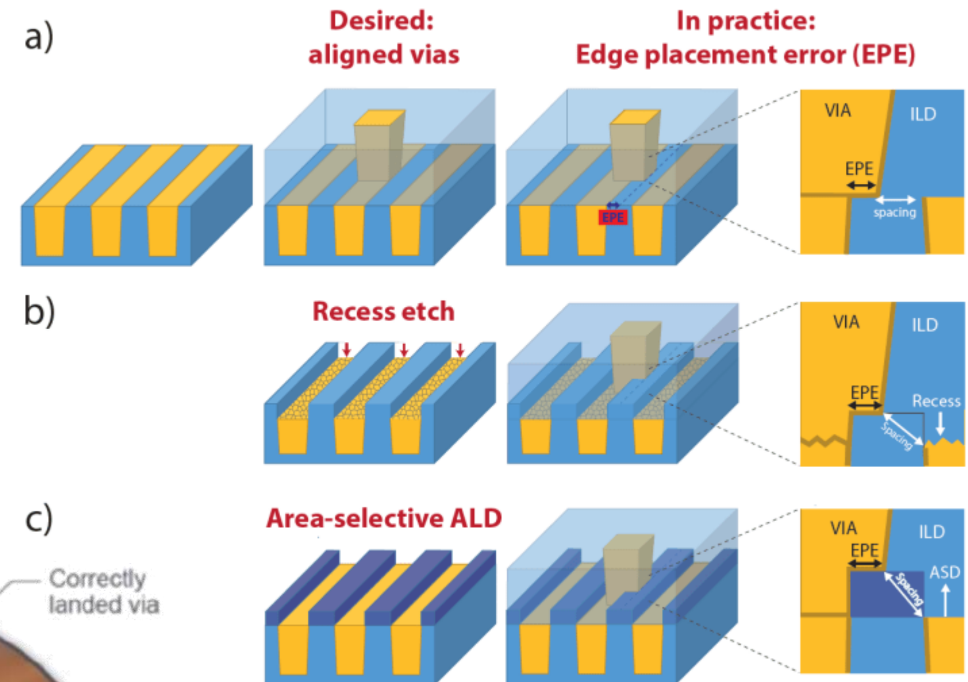
Every Å of pattern error can have **orders of magnitude impact** on device reliability

Fully self-aligned via (FSAV): **larger *horizontal* margin of error** by *vertically* displacing the contact

Requirements for metal ALE:

- *Low temperature*
- *No residues*
- *Free of certain halogens*
- *No roughening*
- *No damage to neighboring materials*





A.J.M. Mackus, M.J.M. Merkx. Fully Self-Aligned Vias: The Killer Application for Area-Selective ALD? – A Discussion of the Requirements for Implementation in High Volume Manufacturing. ***2019****, 7. AtomicLimits.*

M. Balseanu, Selective ALD in a Continuous World, New Techniques and Advancements. SMC Korea ***2021****.*

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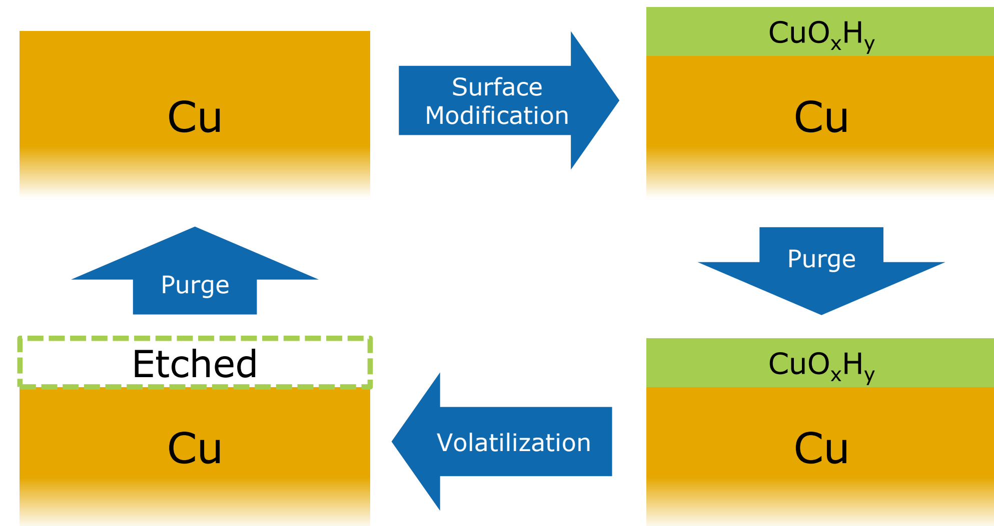
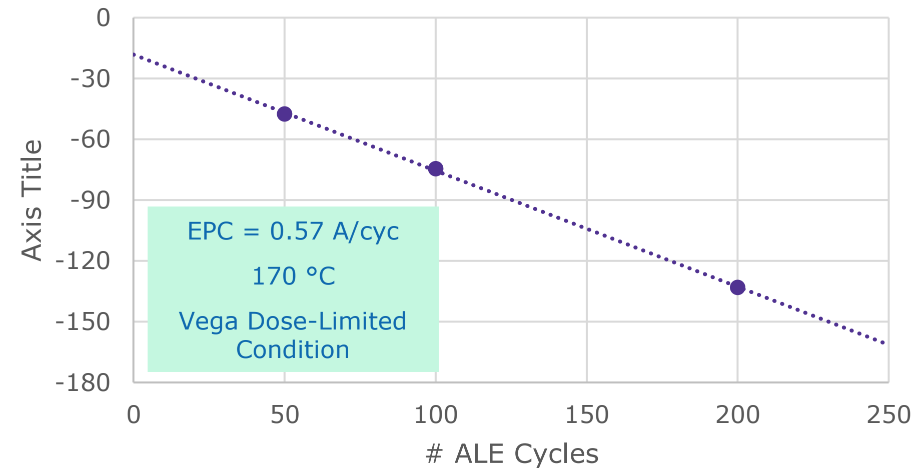
Thermal ALE of Cu

Halogen-Free Cu Removal on a Limited Thermal Budget



2-chemical ALE process:

- Controlled oxidation + hydroxylation of Cu surface by O_2+H_2O
- Purge byproducts with argon
- Volatilization of oxidized surface by halogen-free etchant: **Adhil** or **Vega**
- Purge byproducts with argon



Thermal ALE of Cu
Process Tuning Using the Adhil Halogen-Free Volatilizer

Control oxidant & volatilizer doses to tune etch per cycle:

● Low oxidant dose ● High oxidant dose

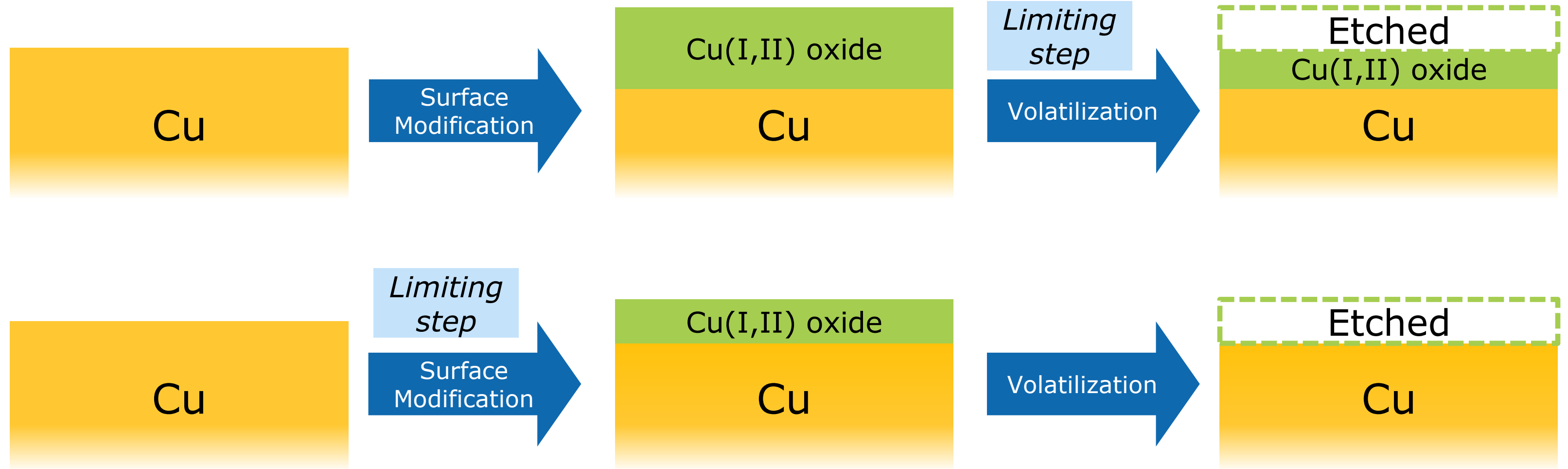
Cu Etch per Cycle (A)

1.6
1.2
0.8
0.4
0

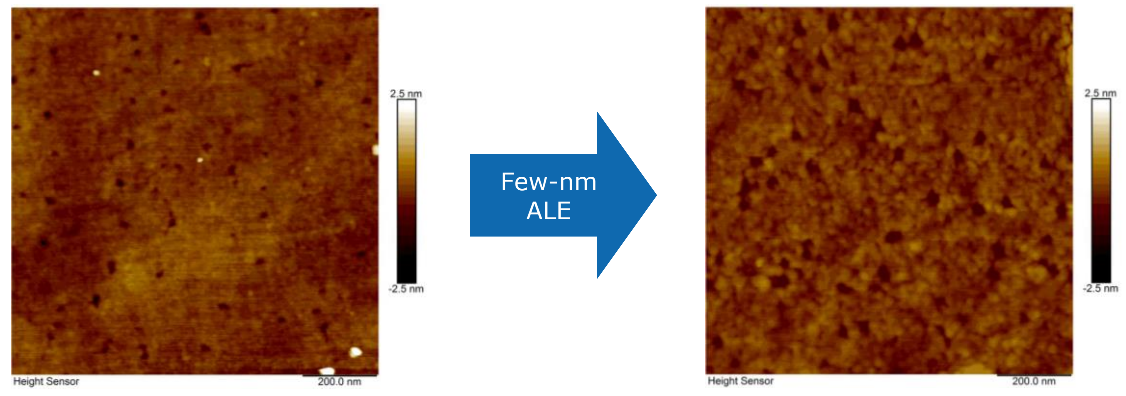
140 °C

0 10 20 30 40

Adhil Dose Time (s)



Limited roughening of the Cu surface:



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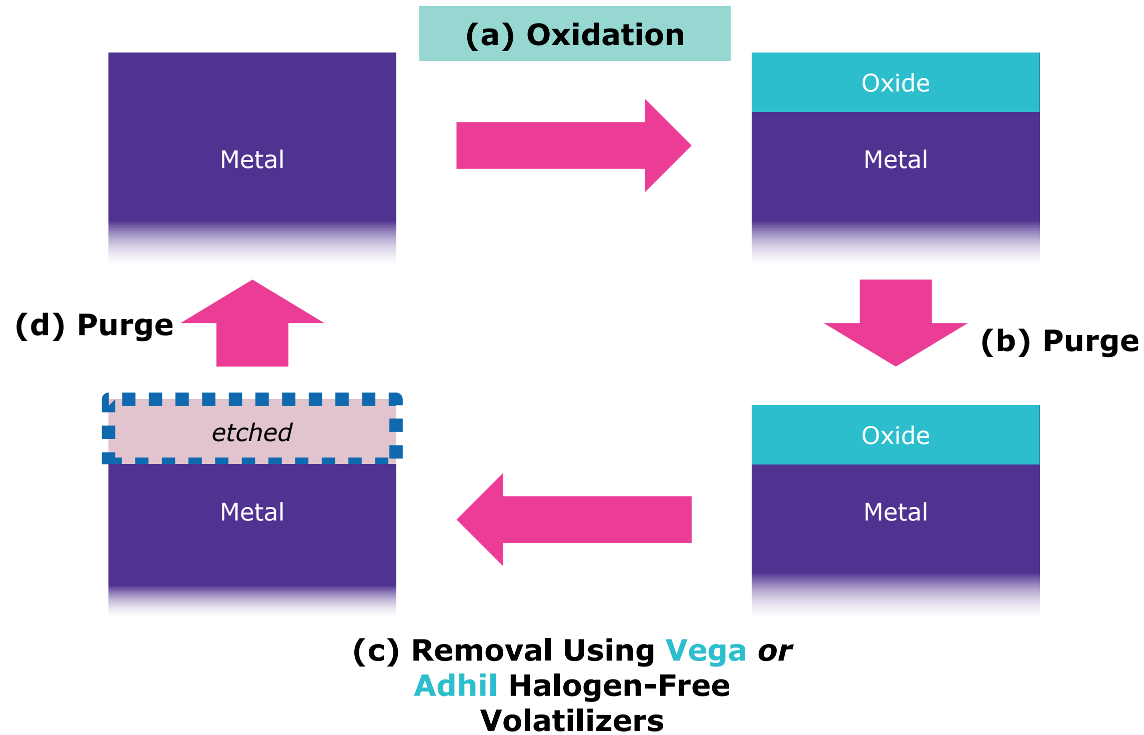
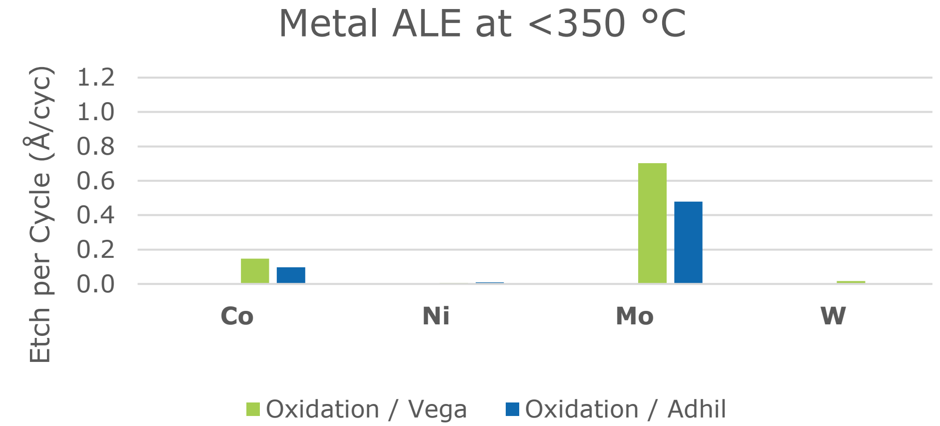
Thermal ALE of Co, Ni, Mo, and W
Choosing the Right Surface Modifier



(c) Removal Using Vega *or* Adhil Halogen-Free Volatilizers

Oxides of **Co**, **Ni**, or **W** are *not* removed by Adhil or Vega…



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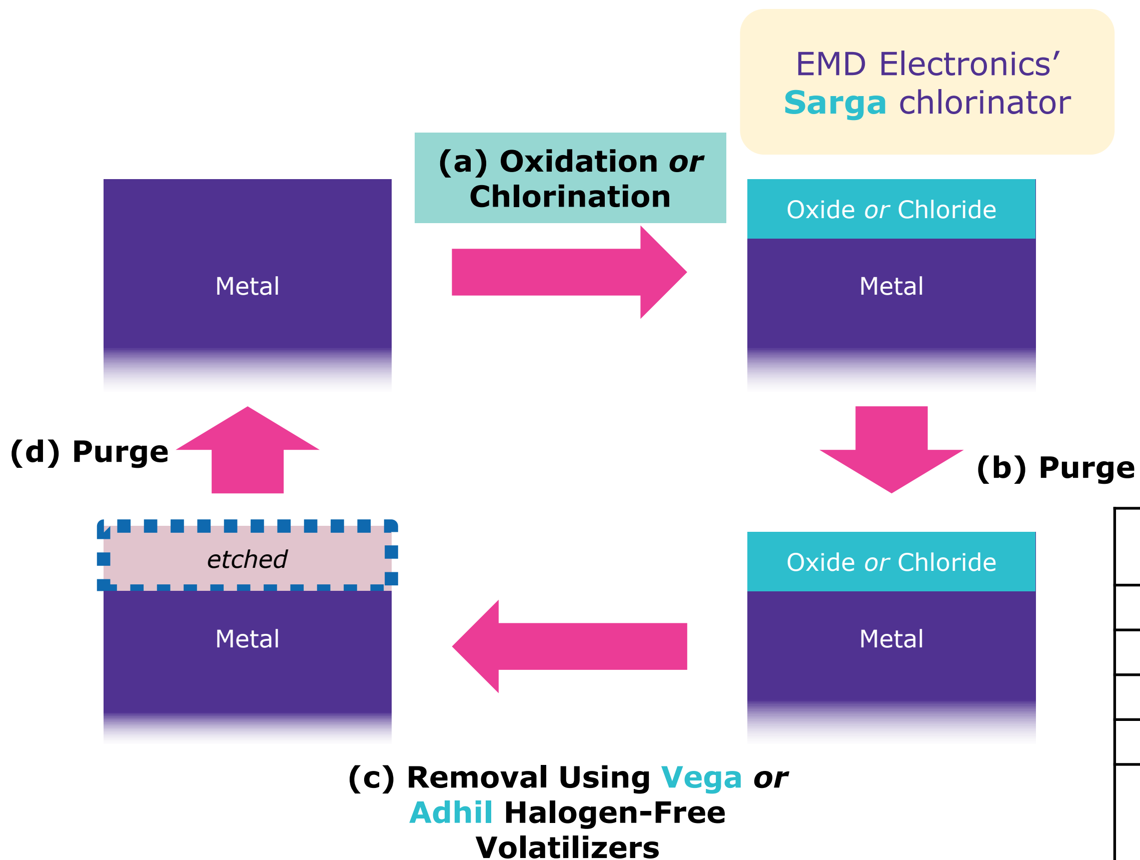

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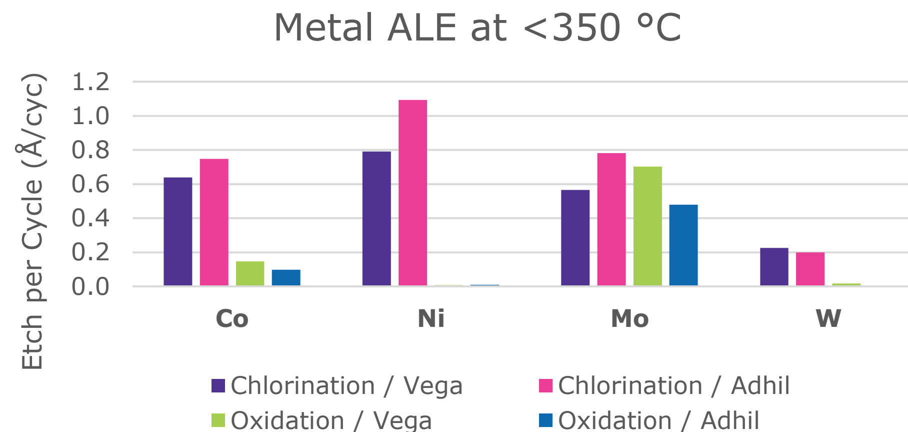

…but chlorides of **Mo, Co, Ni,** or **W** are volatilized.

Mo ALE	*No Process*	Oxidation / Vega	Chlorination / Vega
Mo Removed (Å)	--	28	30
RMS roughness (nm)	*0.3*	0.9	0.4
Resistivity Increase (uohm-cm)	--	>50% increase	No change
Etch Selectivity vs. Si and SiO_2	--	>20:1	>20:1
AFM Image (2um x 2um, 6nm vertical range)			

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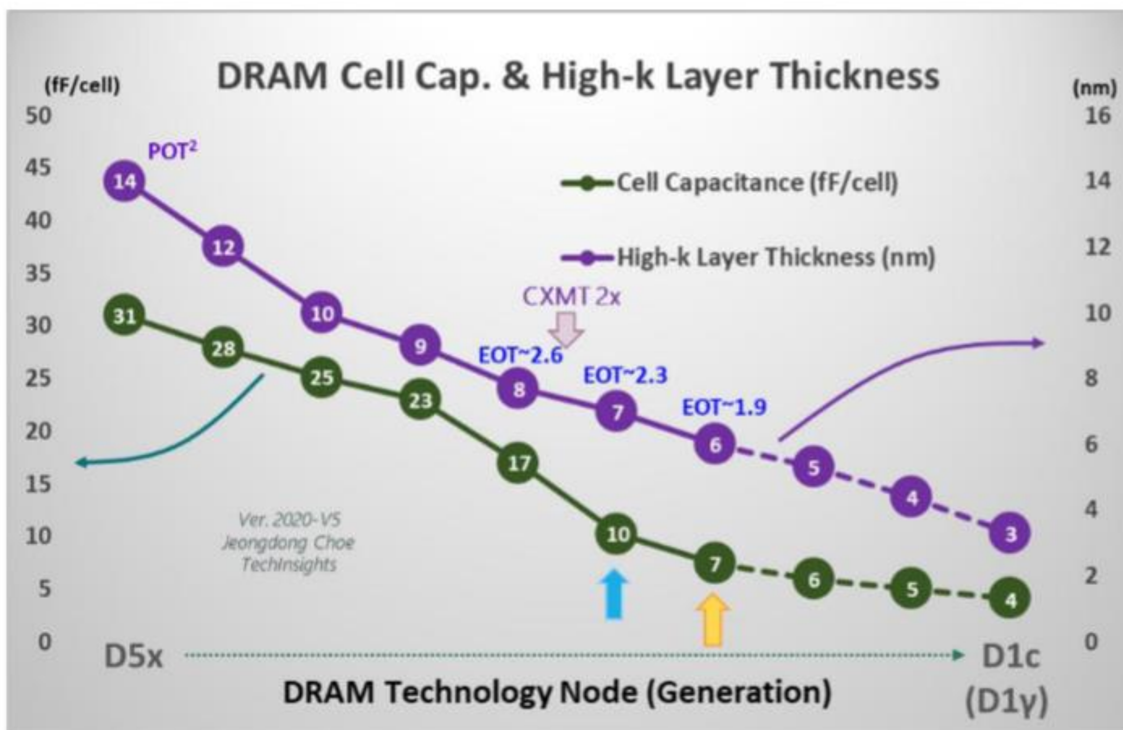
03

ALE of Metal oxides

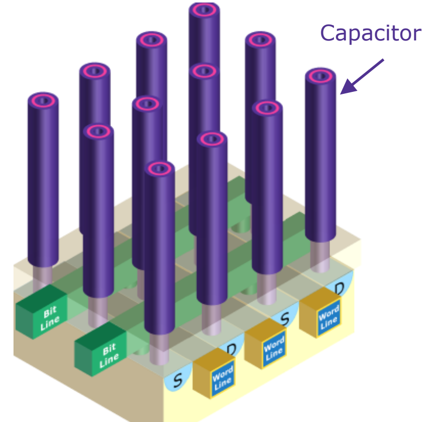
How Can ALE Enable DRAM Downscaling?

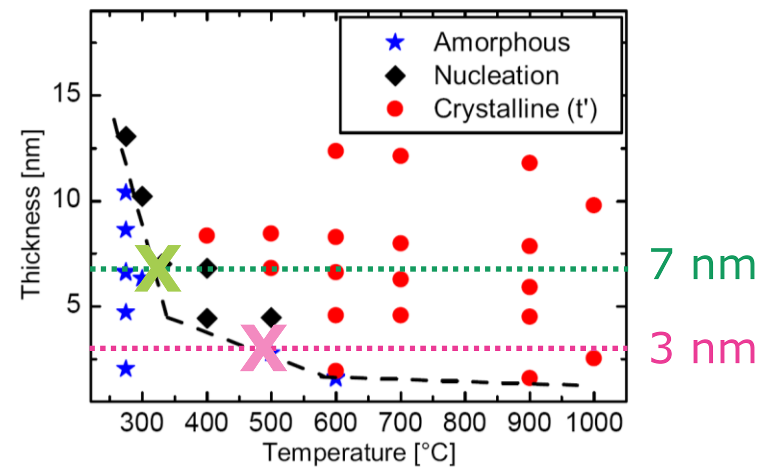


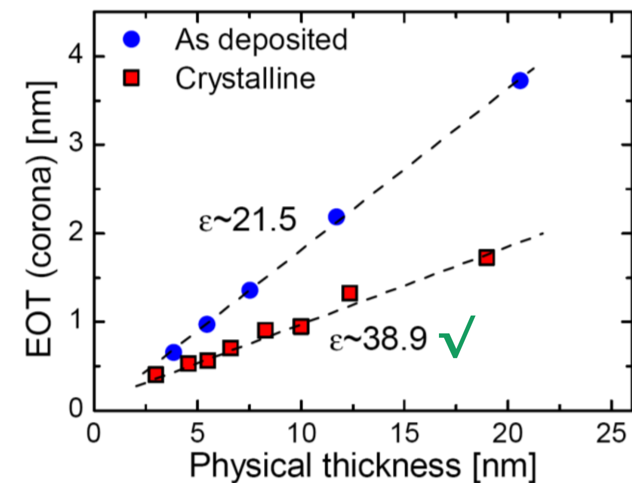
1 Average of three major players; Samsung, Micron and SK Hynix
2 POT: Physical Oxide Thickness, EOT: Equivalent Oxide Thickness

TechInsights Memory Roadmap Analysis

DRAM Device Structure



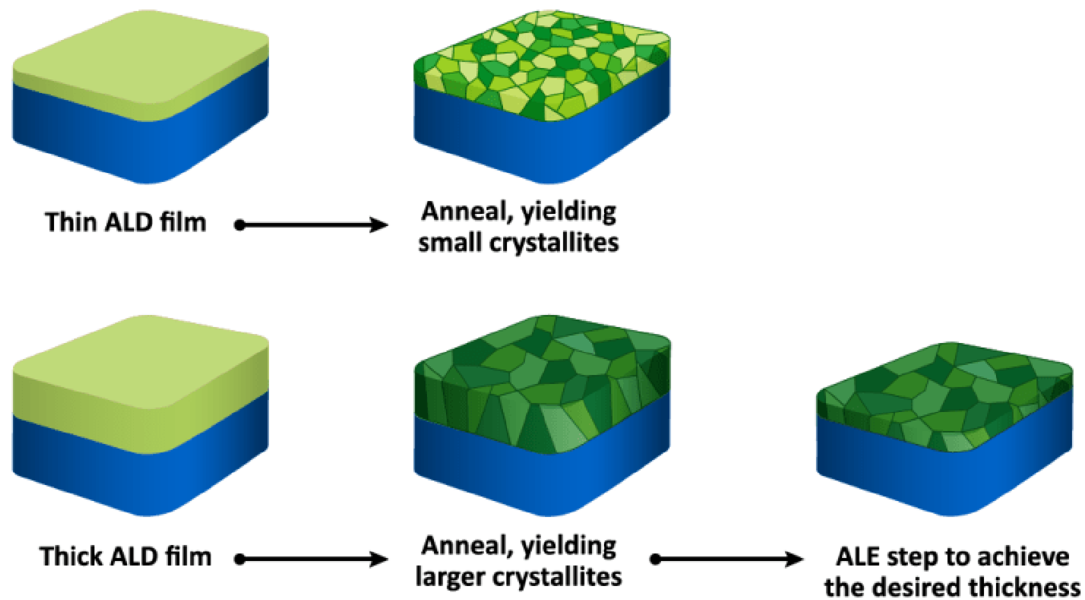


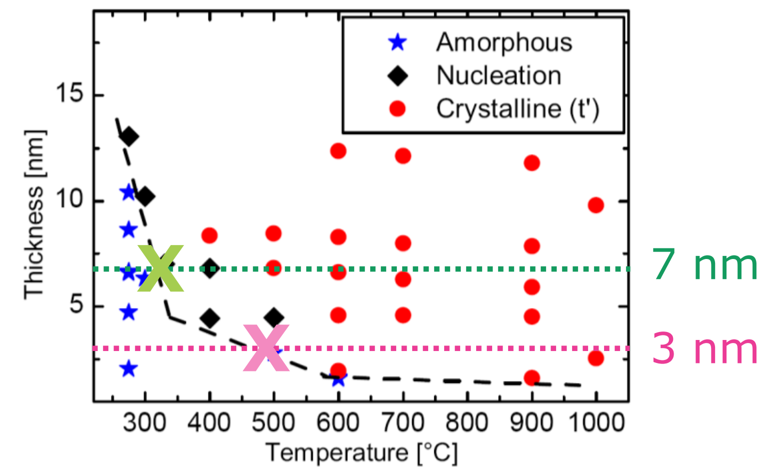


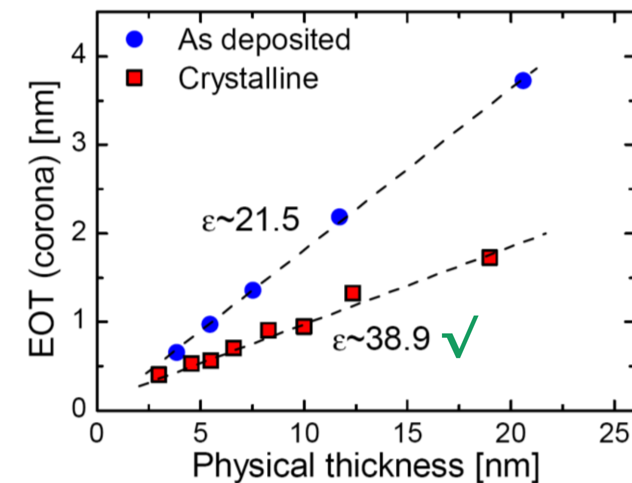
T.S. Böscke, PhD Dissertation, TU Hamburg (2010)

How Can ALE Enable DRAM Downscaling?

How to form a <5nm high-*k* ZrO_2 film:







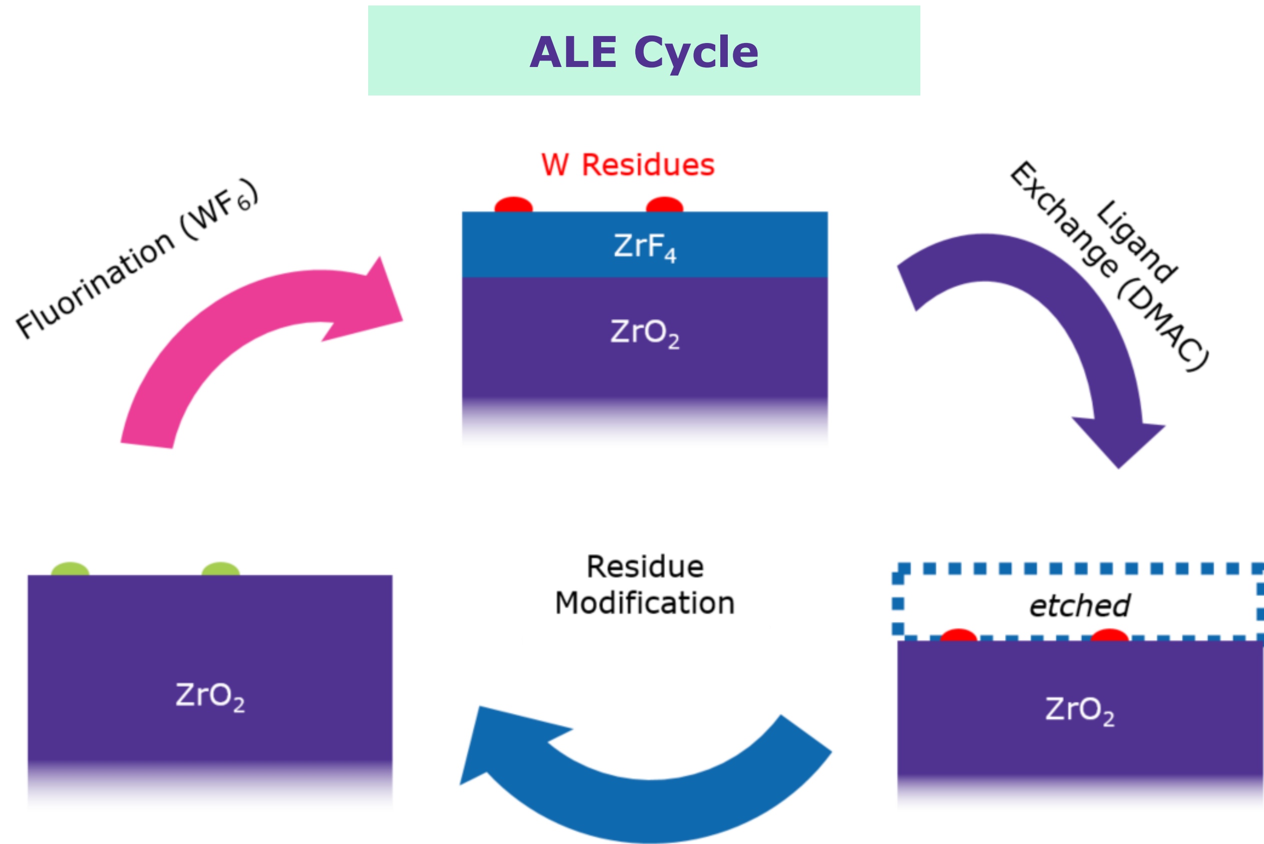
M.E. McBriarty, "Atomic Layer Etch Carves the Path to More Efficient Computing", AtomicLimits (2022)

*J.A. Murdzek & S.M. George, J. Vac. Sci. Technol. A **38** (2020) 022608*

T.S. Böscke, PhD Dissertation, TU Hamburg (2010)

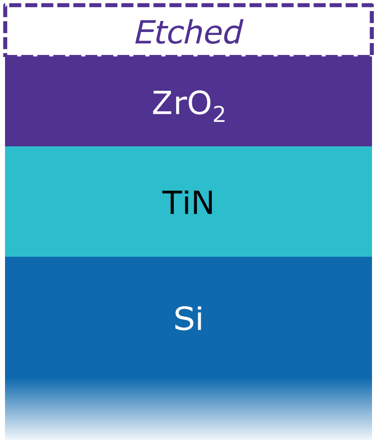
EMD’s High-*k* ALE Process 1

ZrO_2 Thermal ALE



Process Flow for ALE Experiments

- **ALE** (350 °C)
- Ar anneal (500 °C)
- ALD ZrO_2
- ALD TiN
- SiO_2 (3000 Å)
- Si substrate



EMD's High-*k* ALE Process 1

ZrO_2 Thermal ALE

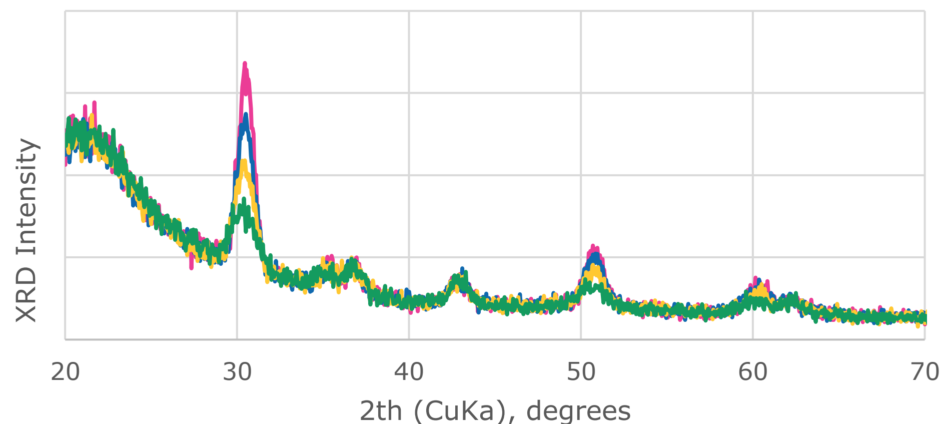
Process Flow

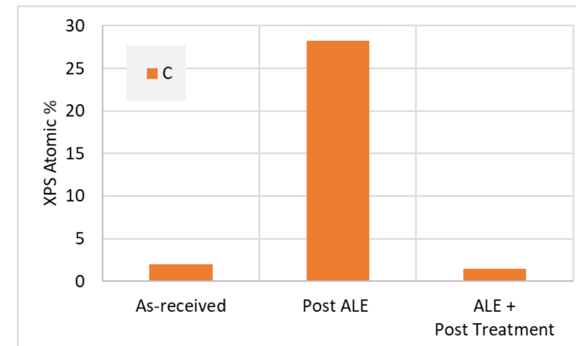
- **ALE**, 350 °C
- Ar anneal, 500 °C
- ALD ZrO_2 (70 Å)
- ALD TiN (~80 Å)
- SiO_2 (3000 Å)
- Si substrate

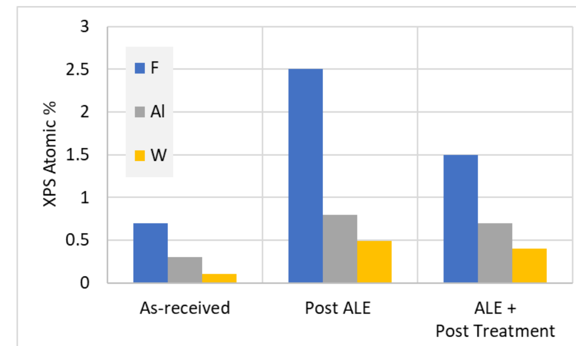
ALE Etch per Cycle (EPC) is tuned by choice of residue modifier & process parameters

EPC = 0.6 – 1.5 Å/cyc

Film & Surface Characterization:







After ALE:

Crystallinity is maintained

C, F, Al, W surface contamination

C and F mitigated by post-treatment

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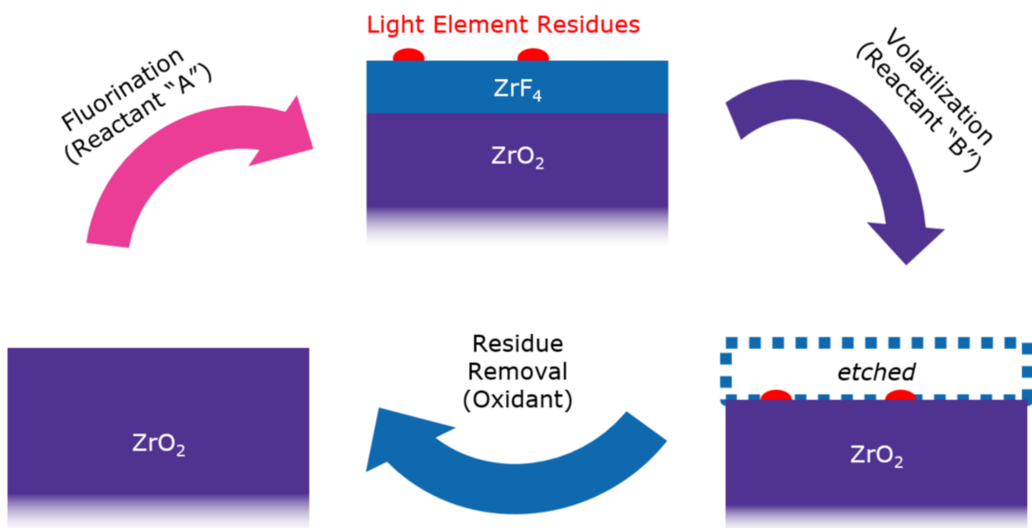
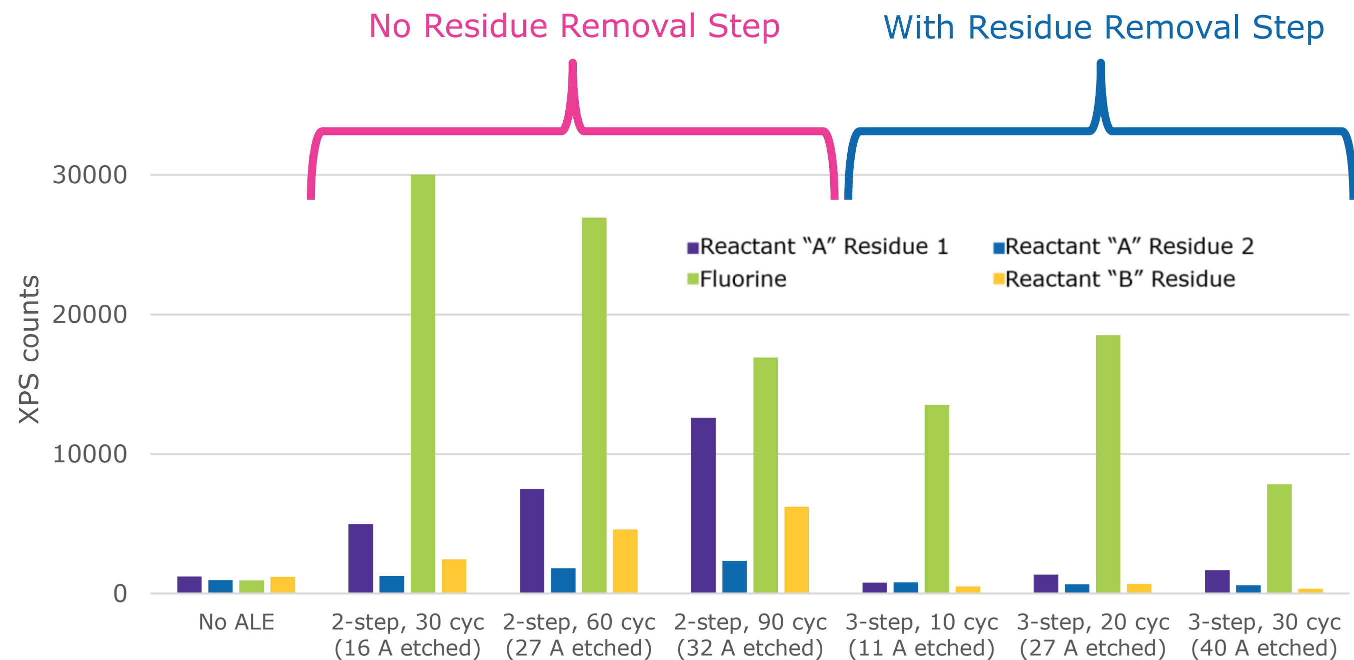
EMD's High-*k* ALE Process 2

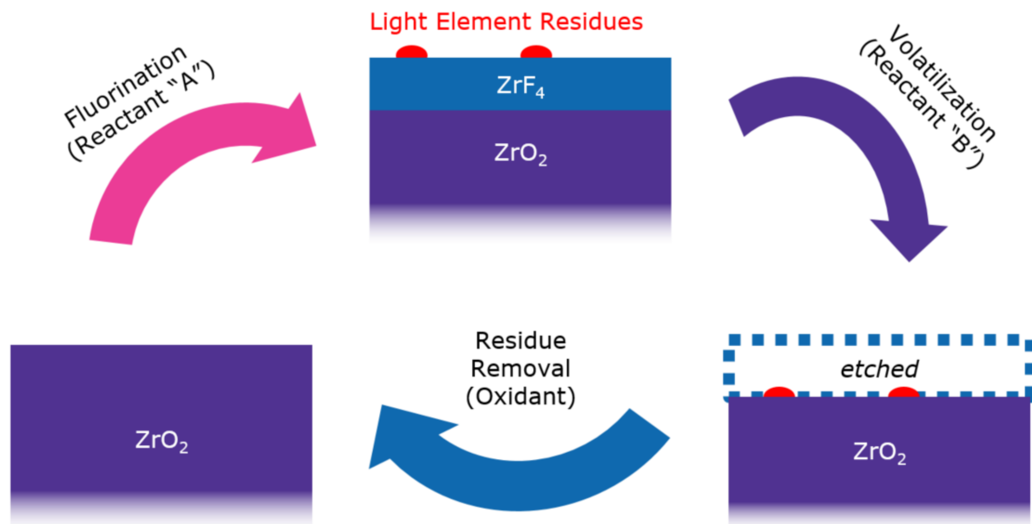
ZrO_2 Thermal ALE Using Metal-Free Reactants

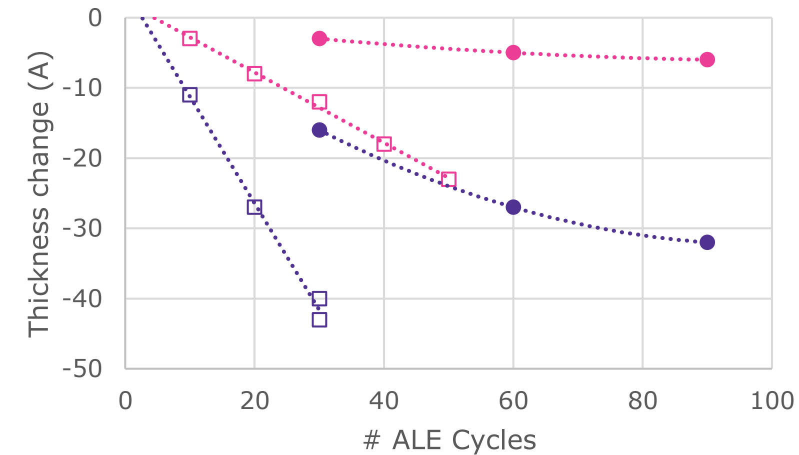




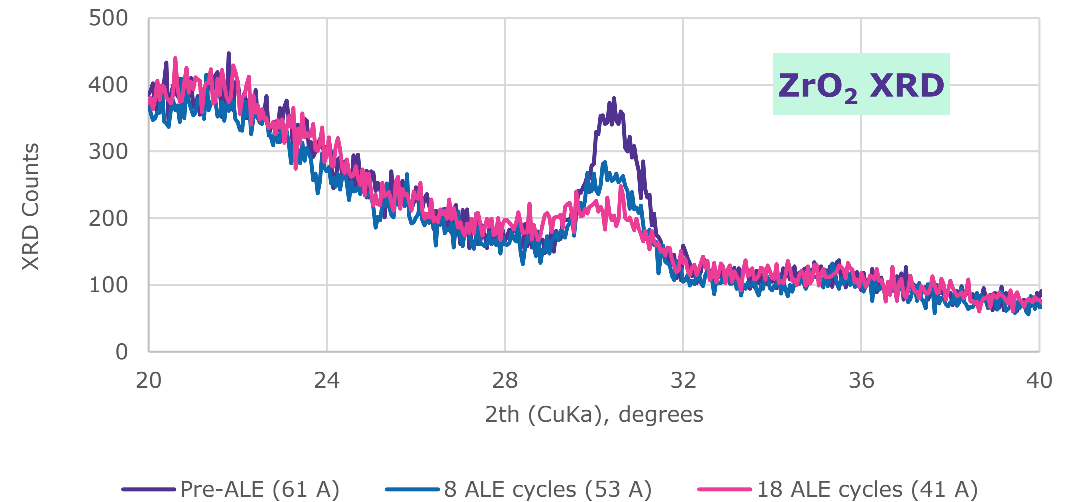
EMD's High-k ALE Process 2

ZrO_2 & HfO_2 Thermal ALE





ZrO_2 & HfO_2 Etch Performance



After ALE:

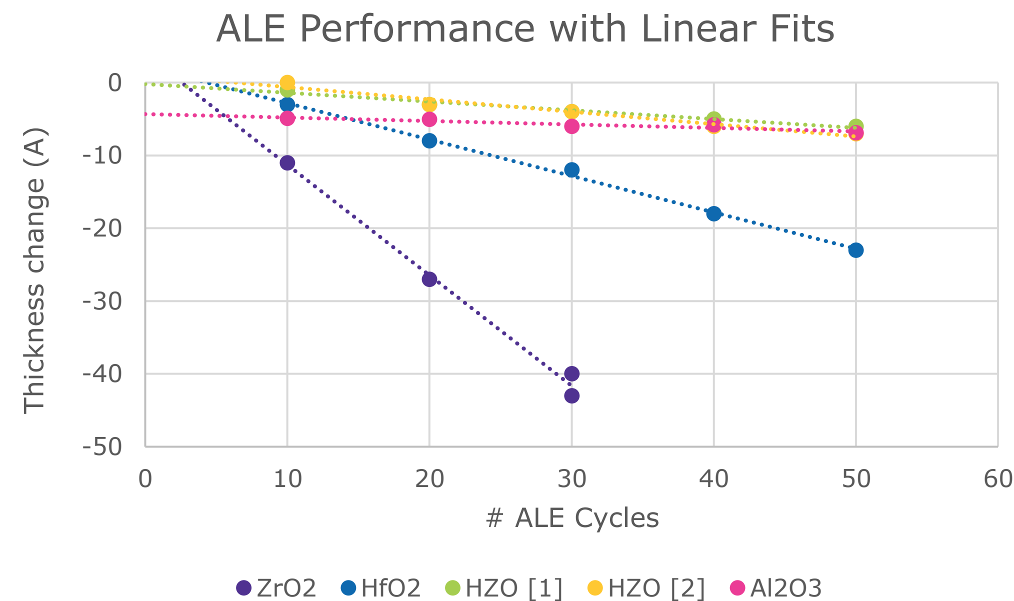
Crystallinity is maintained

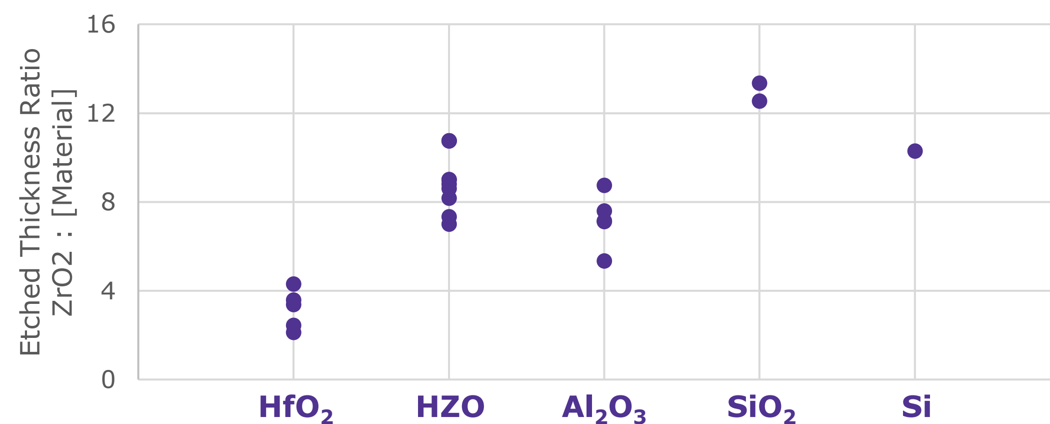
F surface contamination

EMD's High-*k* ALE Process 2

ALE Performance and Selectivity (350 °C)

Material	*Etch per cycle (Å/cyc)*	*Offset (Å)*
ZrO_2	1.52	3.9
HfO_2	0.50	2.2
HZO [ALD process 1]	0.12	-0.2
HZO [ALD process 2]	0.17	1.1
Al_2O_3	0.05	-4.3





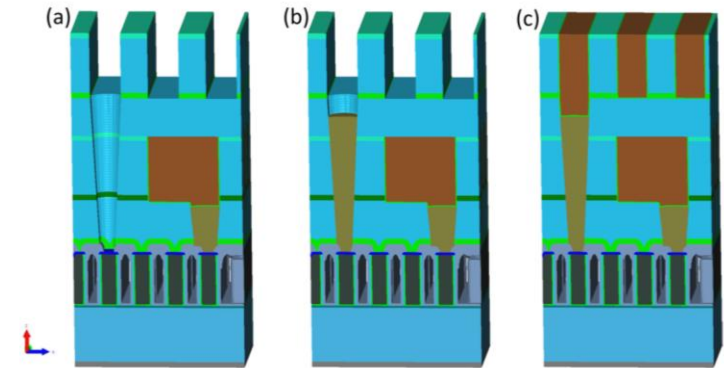
INTERMOLECULAR®

Outlook for ALE

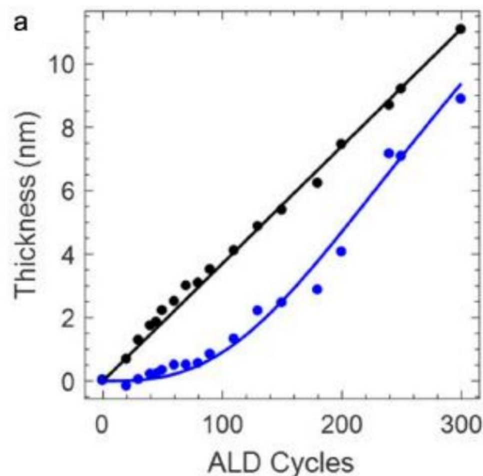
04

ALE Beyond Etchback
Boosting Area-Selective Deposition (ASD) by Selective Etch

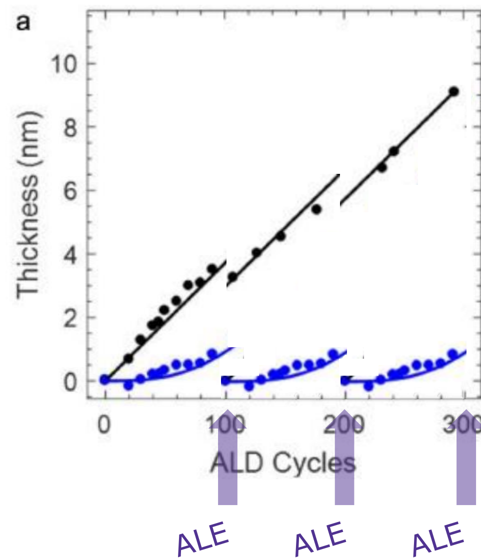
- In ASD, **unwanted nuclei** grow on the "non-growth" surface
- ALE can remove unwanted nuclei with **minimal removal** of desired film



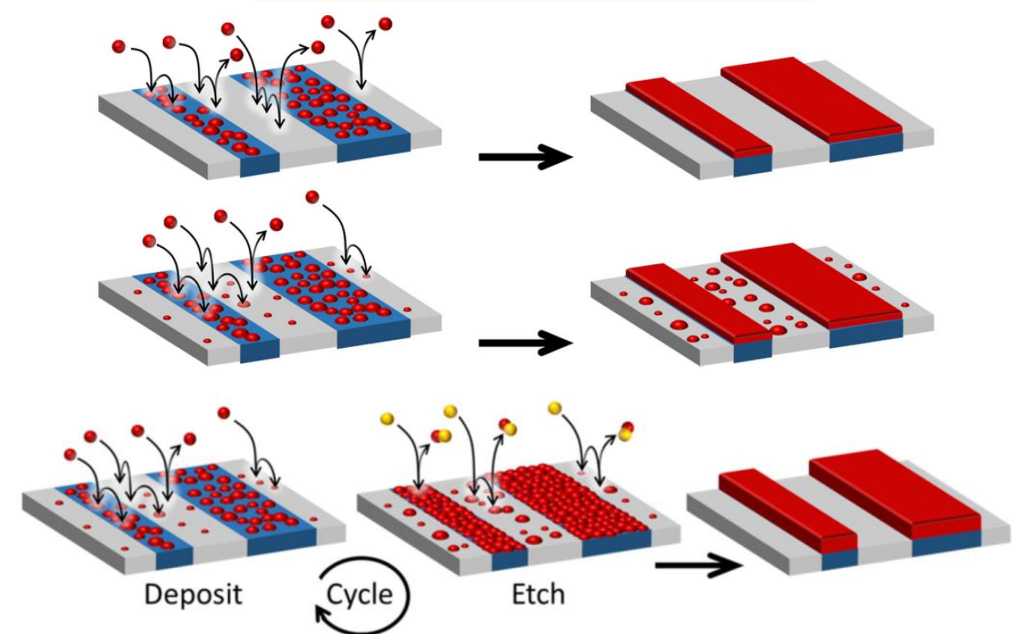
Metal-on-metal ASD for supervia bottom-up fill
Stray metal nuclei → current leaks!



Deposition on **growth surface** vs. **non-growth surface**



ASD + ALE Concept:



G.N. Parsons and R.D. Clark, *Chem. Mater.* **32** (2020) 4920

Making Thermal ALE Viable for Semiconductor Manufacturing

Process

- Etch per Cycle
- Selectivity
- Conformality
- Surface Quality
- Film Properties & Performance

Manufacturing

- Reproducibility
- Throughput
- Chemical Consumption
- Corrosion
- Byproduct Re-Deposition

Safety & Sustainability

- Abatement
- Global Warming Potential (GWP)
- Chemical Life Cycle

EMD Electronics covers nearly all aspects of semiconductor manufacturing

How do ALE & related techniques fit in?

Deposition

Cleanup of nuclei on non-growth surface

Patterning

Hard mask shaping & smoothing

Planarization

Contact recess for hybrid bonding

Chip Design → Prototyping and Testing → Packaging → Module Assembly → End Use

Doping

Cleaning

Removal of residues and native oxides

Etching

High aspect ratio / low critical dimension etches

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