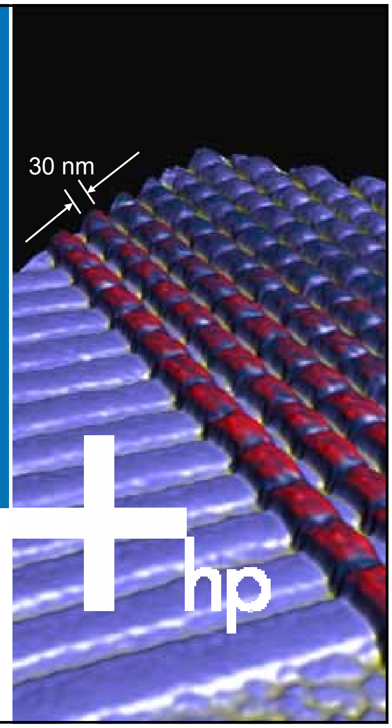
Finding the Missing Memristor



Stan Williams
HP

People who did the work:

Over 60 current and former members of the QSR Research group and 40 members of other HP orgs

esp. Greg Snider, Duncan Stewart, Dimitri Strukov, Matthew Pickett, Julien Borghetti, and Jianhua Yang

Our partners at UCLA & Caltech,

Our partners at LBNL and NIST

Supported in part by DARPA & IARPA

The nanotechnology dilemma

We say that nanotech is different, but then we try to build familiar objects with nano dimensions. . .

We say that nanotech is inter-disciplinary, but do we just work with the usual suspects?

We say that nano is new – but have we forgotten old lessons?

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Overview of Presentation

- What is a Memristor?
- How do you make them?
- What are they good for?
  - Configurable rectifiers and switches
  - Crosspoint Memories
  - Sequential Implication Logic
  - Synaptic computation

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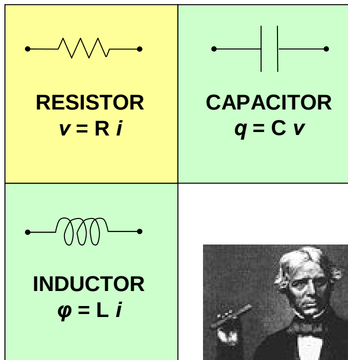
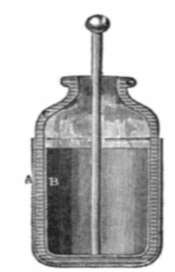
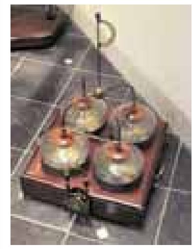
3 fundamental passive linear circuit elements

Resistor – 1827
Georg Ohm







Capacitor - 1745
Volta / von Kleist & van Musschenbroek
Benjamin Franklin

Inductor – 1831
Michael Faraday
Joseph Henry

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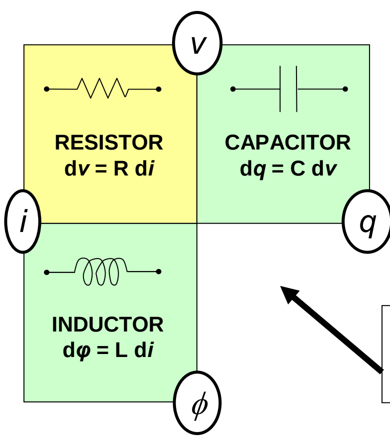
1960's – Leon Chua generalizes circuit theory to nonlinear systems of equations



And sees that there is a hole where an obvious relation seems to be missing

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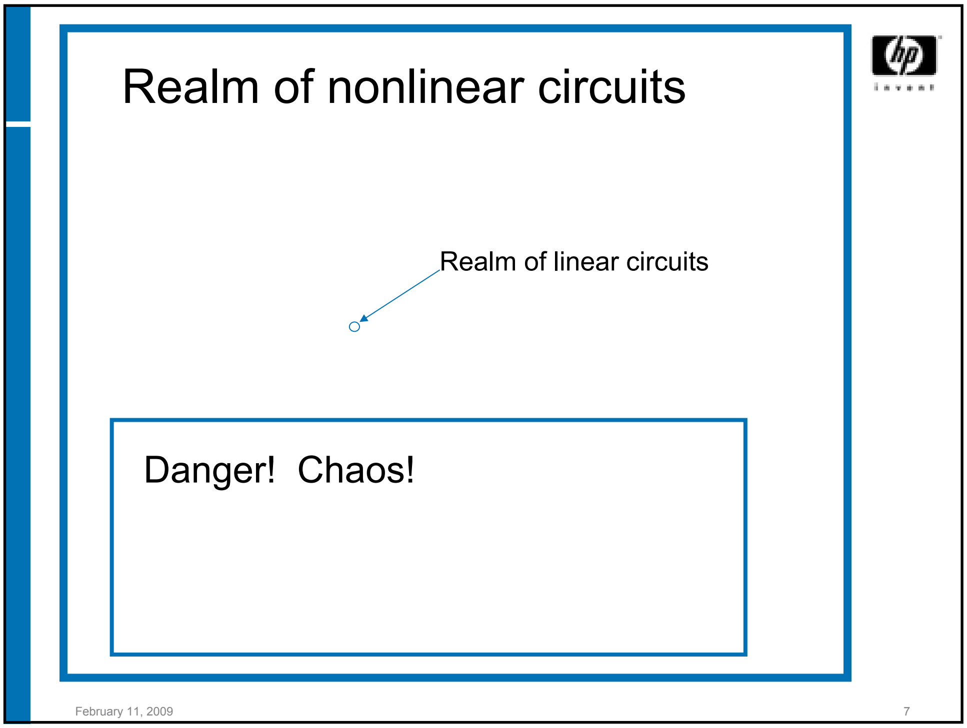
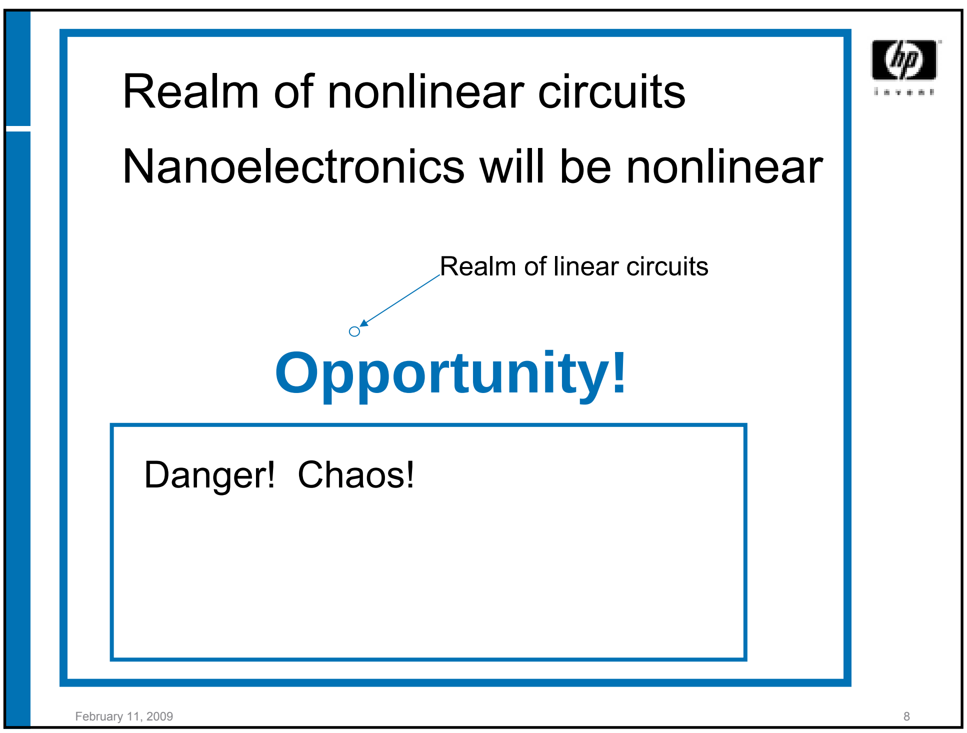

Realm of nonlinear circuits
Realm of linear circuits
Danger! Chaos!
February 11, 2009
7


Realm of nonlinear circuits
Nanoelectronics will be nonlinear
Realm of linear circuits
Opportunity!
Danger! Chaos!
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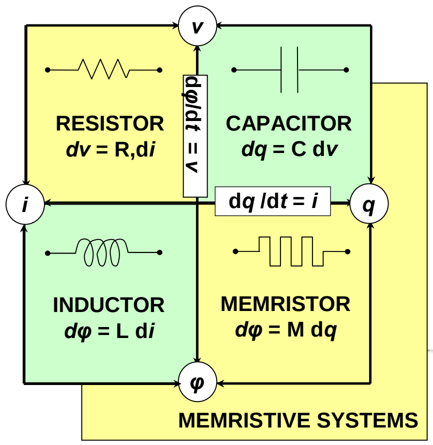
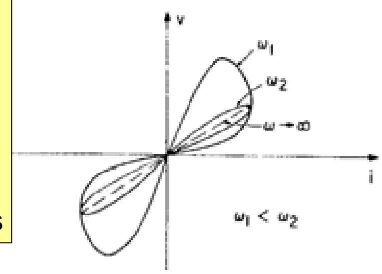
8

In1971, Chua postulates the memristor, but states that there is no known example



$$v = R(w)i$$

$$\frac{dw}{dt} = f(i)$$



L. O. Chua, "Memristor - the missing circuit element," IEEE Trans. Circuit Theory 18, 507–519 (1971).
L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE,* 64 (2), 209-23 (1976).

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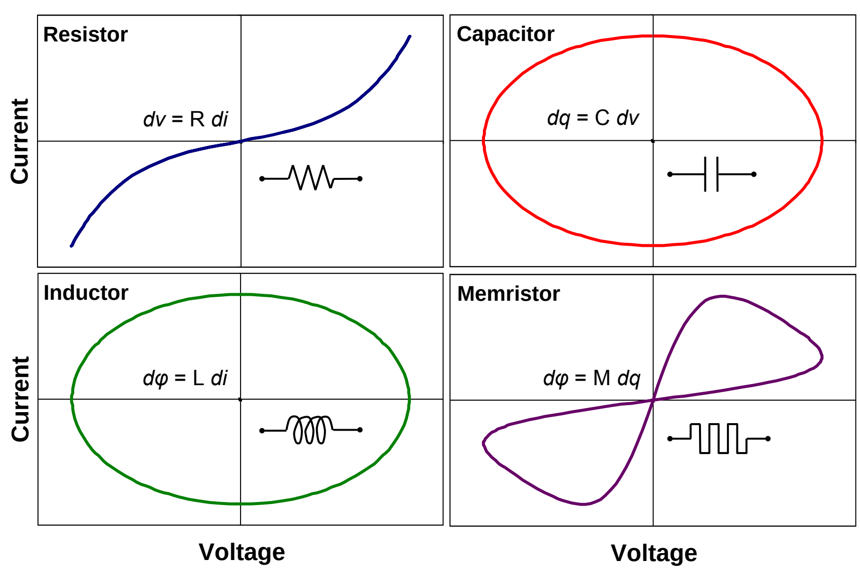
Four Fundamental Nonlinear Passive Circuit Elements



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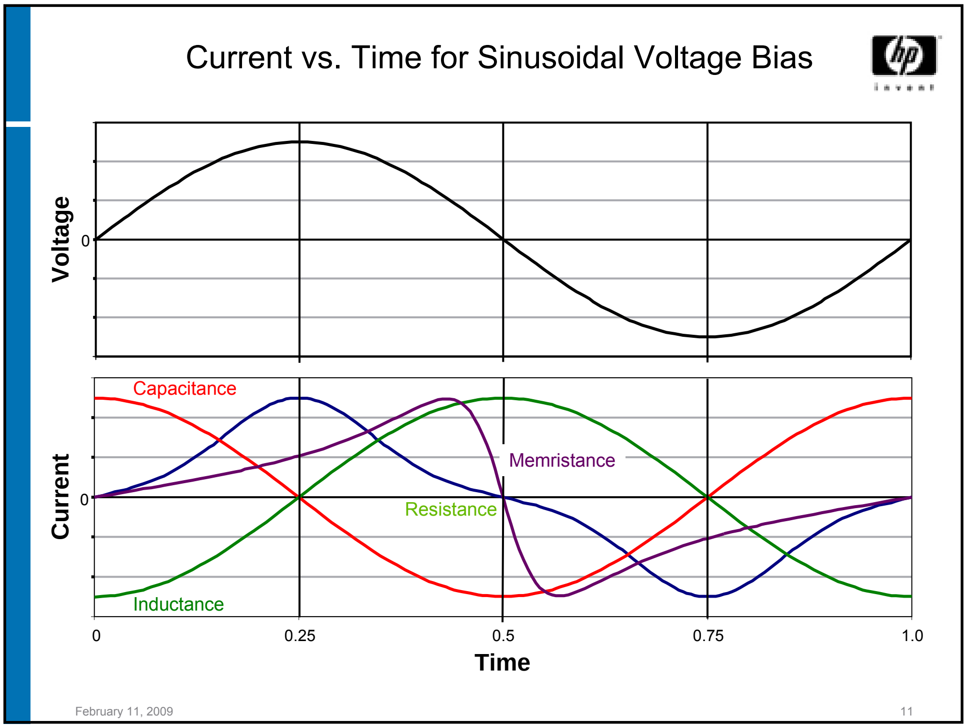
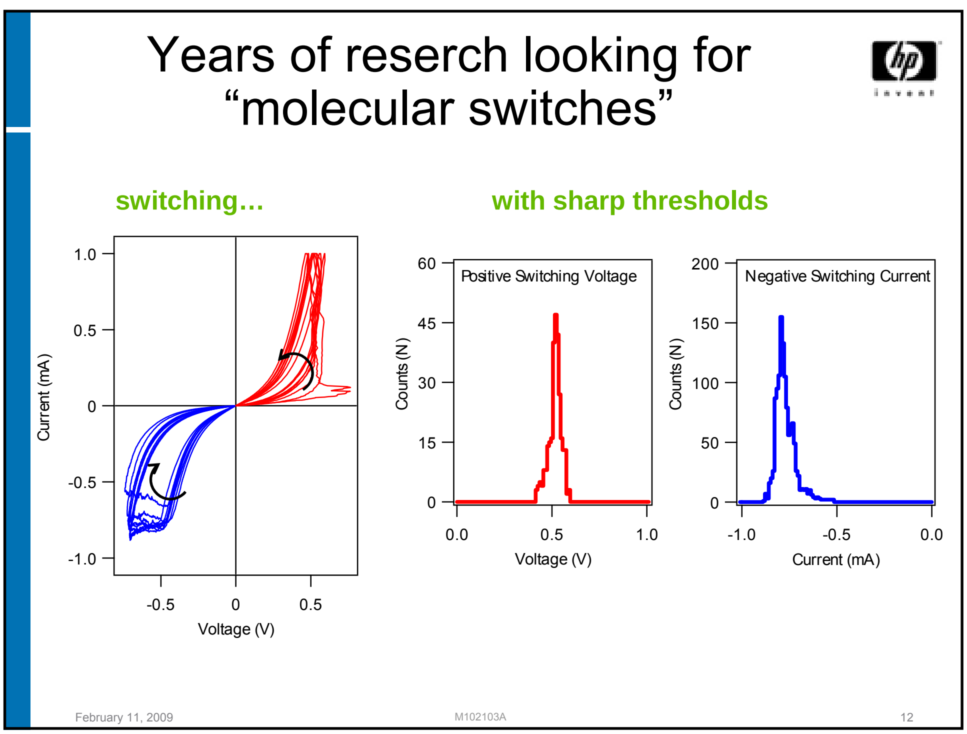
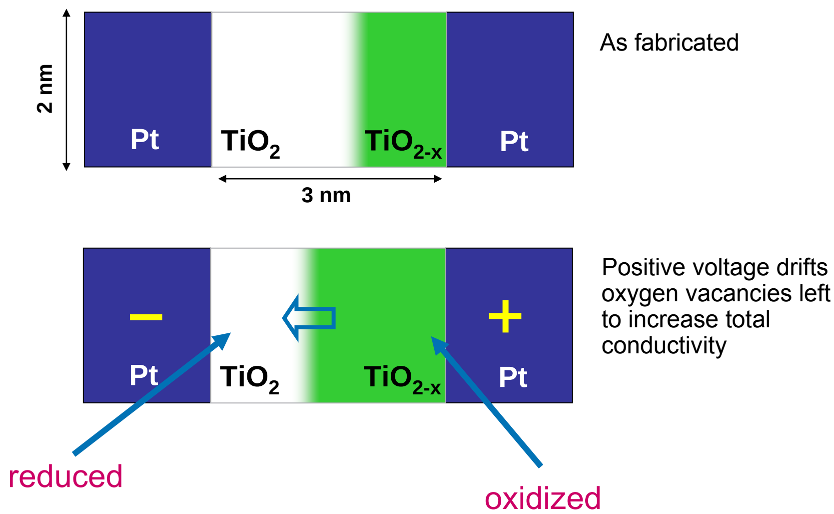

Current vs. Time for Sinusoidal Voltage Bias
Voltage
0
Current
0
Capacitance
Memristance
Resistance
Inductance
0
0.25
0.5
0.75
1.0
Time
February 11, 2009
11


Years of reserch looking for
“molecular switches”
switching…
with sharp thresholds
1.0
0.5
0
-0.5
-1.0
Current (mA)
-0.5
0
0.5
Voltage (V)
Positive Switching Voltage
60
45
30
15
0
Counts (N)
0.0
0.5
1.0
Voltage (V)
Negative Switching Current
200
150
100
50
0
Counts (N)
-1.0
-0.5
0.0
Current (mA)
February 11, 2009
M102103A
12

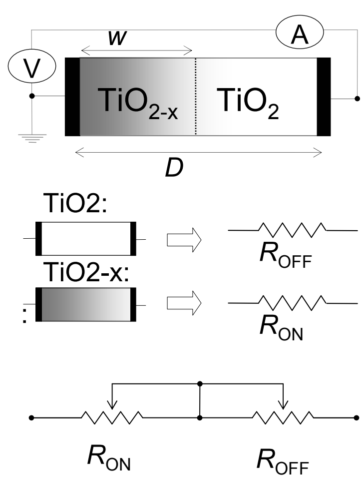
O vacancy drift model for TiO_{2-x} switch



As fabricated

Positive voltage drifts oxygen vacancies left to increase total conductivity

Simplified Theory of Memristance



$$\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i(t)$$

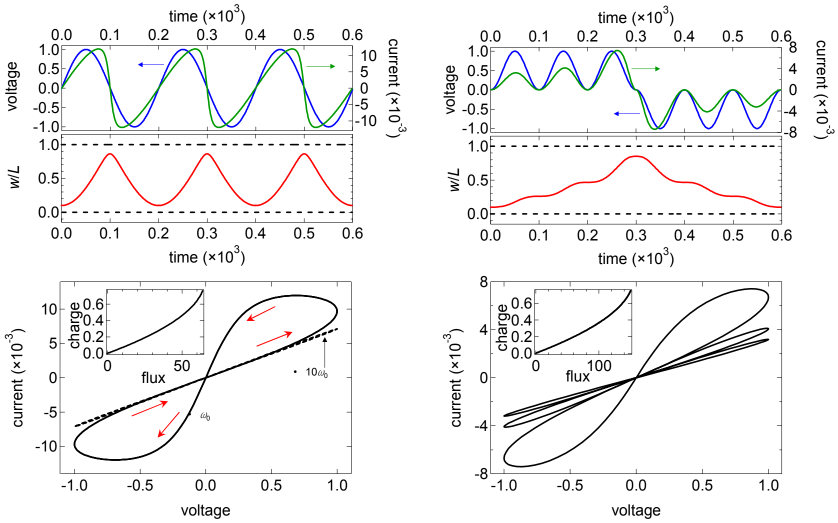
$$v(t) = \left[R_{ON} \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right] i(t)$$

$$M(q) = R_{OFF} \left(1 - \frac{\mu_V R_{ON}}{D^2} q(t) \right)$$

Two coupled equations of motion –
One for the charged vacancies
One for the electronic transport
(both versions of Ohm's law)

Nature **453** (2008) 80-83.

Look at current-voltage plots of the model



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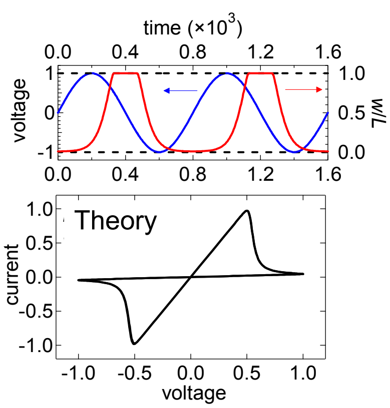
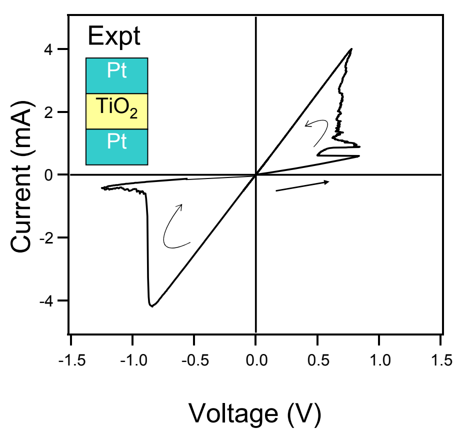
Comparison between Theory and Experiment: Pt : TiO_2 : Pt Memristor!





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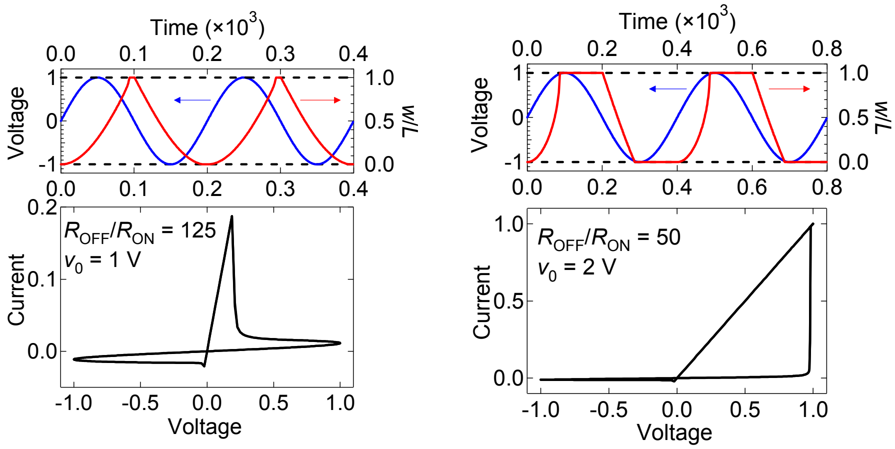
Ionic Memristive Device (Hard Boundary Conditions)



no window function but w is not changing beyond [0, D]

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Metal Oxide Resistive Switches

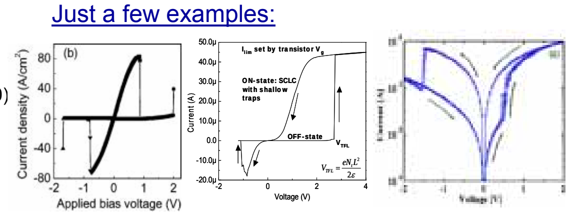
“Memory effects” in oxides have been known for a while:

G. Dearnaley *et al.*, *Rev. Prog. Phys.* (1970) a review with 150+ references

Just a few recent references:

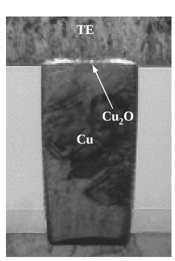
	metal:
S. Seo *et al.*, *APL* (2003)	Ni
B. J. Choi *et al.*, *JAP* (2005)	Ti
H. Sim *et al.*, *Microel. Eng.* (2005)	Nb
D. Lee *et al.*, EDL (2005)	Zr
A. Chen *et al.*, *IEDM'05*	Cu
M. Kund *et al.*, *IEDM'05*	Ag
D. C. Kim *et al.*, *APL* (2006)	Nb
N. Banno *et al.*, *IEICE TE* (2006)	Cu(S)
T.-N. Fang *et al.*, *ICMTD'07*	Cu
L. Courtade *et al.*, *ICMTD'07*	Ni
W. Guan *et al.*, *APL* (2007)	Zr
S.-W. Kim & Y. Nishi, *NVMTS'07*	Cu(S)
D. Stewart, *NVMTS'07*	Ti
K.-C. Liu *et al.*, *NVMTS'07*	Hf
D. Lee *et al.*, *APL* (2007)	Mo

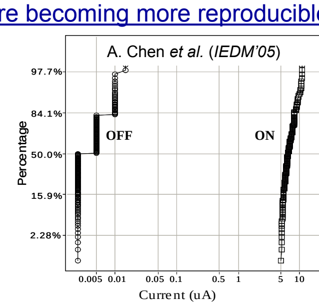
Just a few examples:



B. J. Choi *et al.* (2005) A. Chen *et al.* (2005) D. Lee *et al.* (2007)

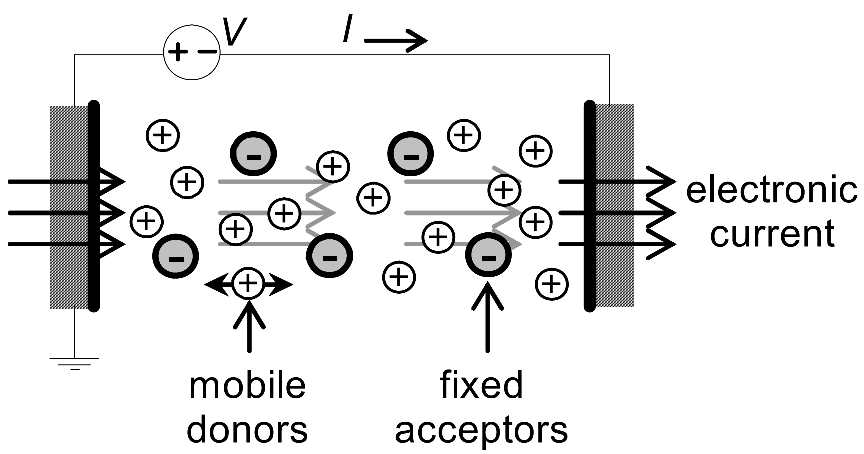
With time, data are becoming more reproducible:





February 11, 2009 slide courtesy K. Likharev

Semiconductor memristance is coupled ion-electron motion



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Slightly More Advanced Theory - Ions

$$J_{\text{ION}} = J_{\text{ION}}^{\text{drift}} + J_{\text{ION}}^{\text{solute diffusion}}$$

$$J_{\text{ION}}^{\text{drift}} = q\mu_0 E_0 \sinh\left(E / E_0\right)$$

$$J_{\text{ION}}^{\text{solute diffusion}} = qD\frac{\partial N}{\partial x}$$

$$D \approx fa^2 \exp[-U_A /(k_B T)]/(1 - Na^3)$$

$$N/ t = - J_{\text{ION}}/ x$$

$$J_{\text{ION}}(x=0) = J_{\text{ION}}(x=L) = 0$$

$$N' = N\left(1 - \left(1 + \frac{1}{g}\exp\left(\frac{E_D - E_F - e\varphi}{k_B T}\right)\right)^{-1}\right)$$

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Slightly More Advanced Theory – e⁻s

$$J_{\mathrm{ELECTRON}} = e\mu_{\mathrm{EL}} n_{\mathrm{EL}} \frac{\partial E_F(x)}{\partial x}$$

$$n_{EL} = N_C F_{1/2}\left(\frac{E_F - E_C + e\varphi}{k_B T}\right) \overset{E_F - E_C + e\varphi >> k_B T}{\approx} N_C \exp\left(\frac{E_F - E_C + e\varphi}{k_B T}\right)$$

$$-\varepsilon\varepsilon_0 \nabla^2 \varphi = ezN' - en_{EL}$$

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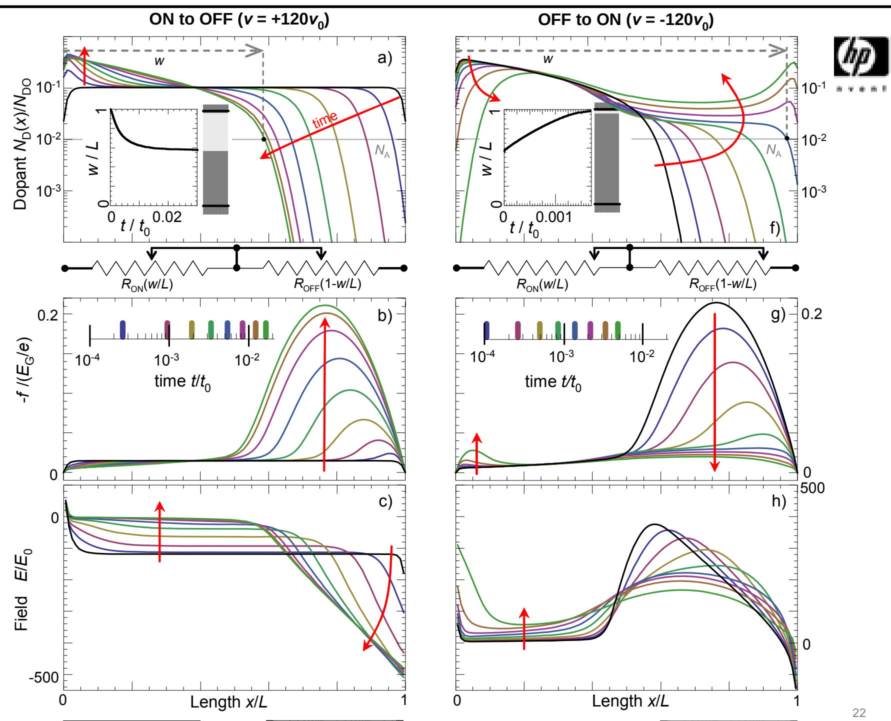

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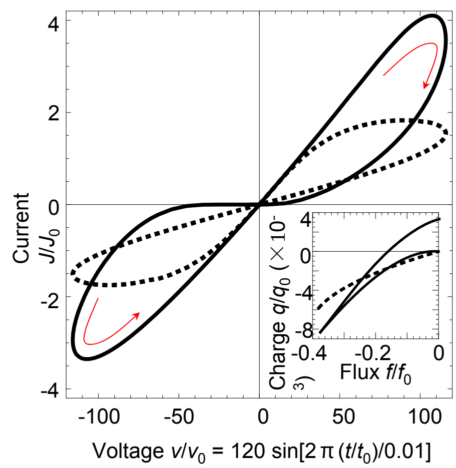
Drift-Diffusion Model: Memristance



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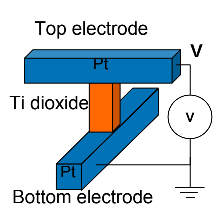
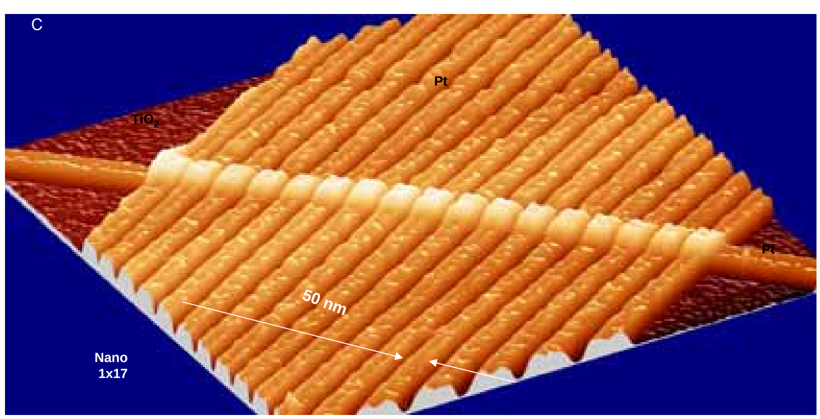
The Workhorse System:

50 nm Pt electrodes by NIL

~3-30 nm TiO_2





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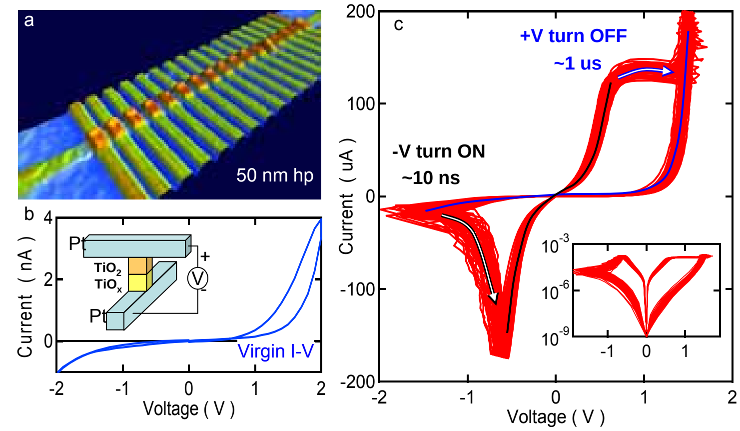
50 nanometer Pt/TiOx/Pt devices



Switch ON ~10 ns, state is stable for (10^6?) years

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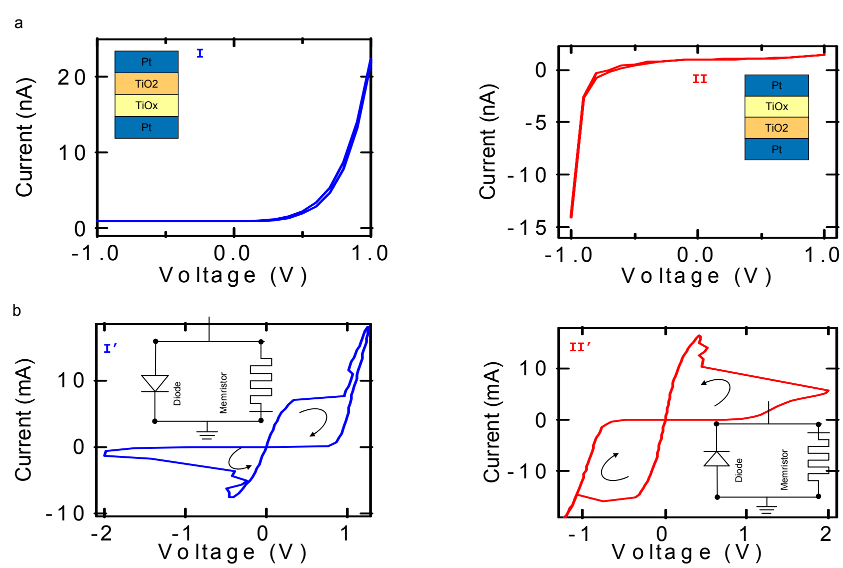
Vacancy location controls switch polarity



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Conclusions on Memristors

- The switching mechanism for the devices is field induced drift of positively charged O vacancies in TiO_2 that controls the resistance of the film
- This is the first experimental realization and physical model for a memristor – the fourth nonlinear passive circuit element that has been 'missing' for nearly 40 years
- We see that memristance arises naturally in systems where atomic and electronic equations of motion are coupled – this is far more likely to be observed at the nanoscale

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What might memristors be used for?

Non-volatile RAM
Config Bits
New forms of logic
Electronic Synapse

But need hybrid circuits!

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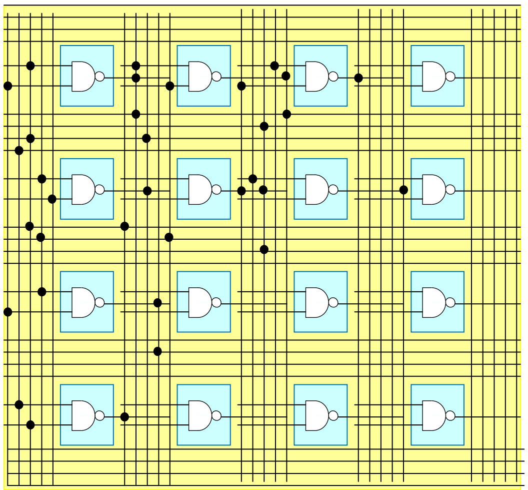
CMOS FPGAs



The good:
- Massive parallelism
- Defect tolerant
- Simple design

The bad:
- 80%-90% area is wires/configuration
- High capacitance → high power

The ugly:
- Defect characterization
- Compilation

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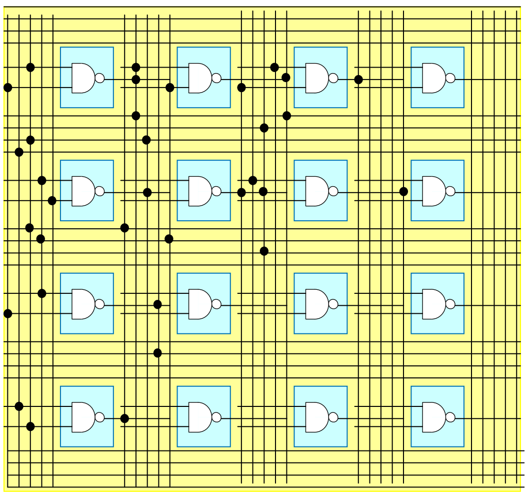
SNIC Strategy



Start with CMOS FPGA

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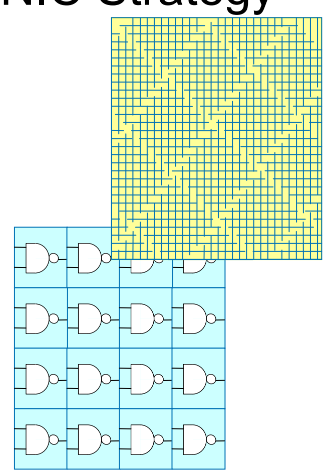
SNIC Strategy

1. Remove interconnect and configuration bits

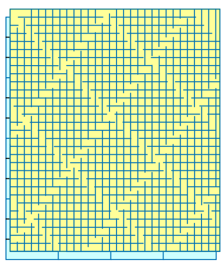
SNIC Strategy



1. Remove interconnect and configuration bits
2. Compress logic
3. Add nano interconnect and configuration

SNIC Strategy

1. Remove interconnect and configuration bits
2. Compress logic
3. Add nano interconnect and configuration



- Inexpensive CMOS design
- Inexpensive process (nanoimprint)
- Nano redundancy → defect tolerance
- Small size, high yield → low cost
- Low energy

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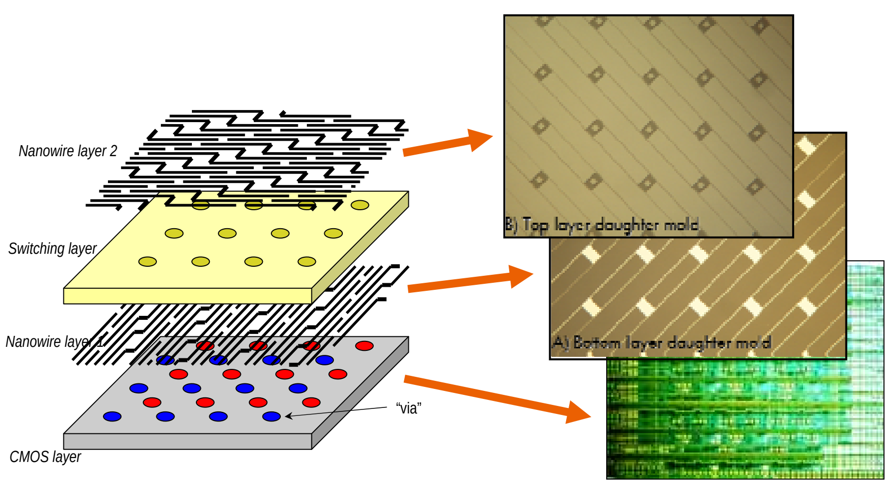
SNIC: Chip Demo



Courtesy Qiangfei Xia

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