Silicon Photonics and the Datacenter

Marco Fiorentino

HP Labs

05/19/2015

“In the last 7 years online data increased 56 times”

Data-centric computing

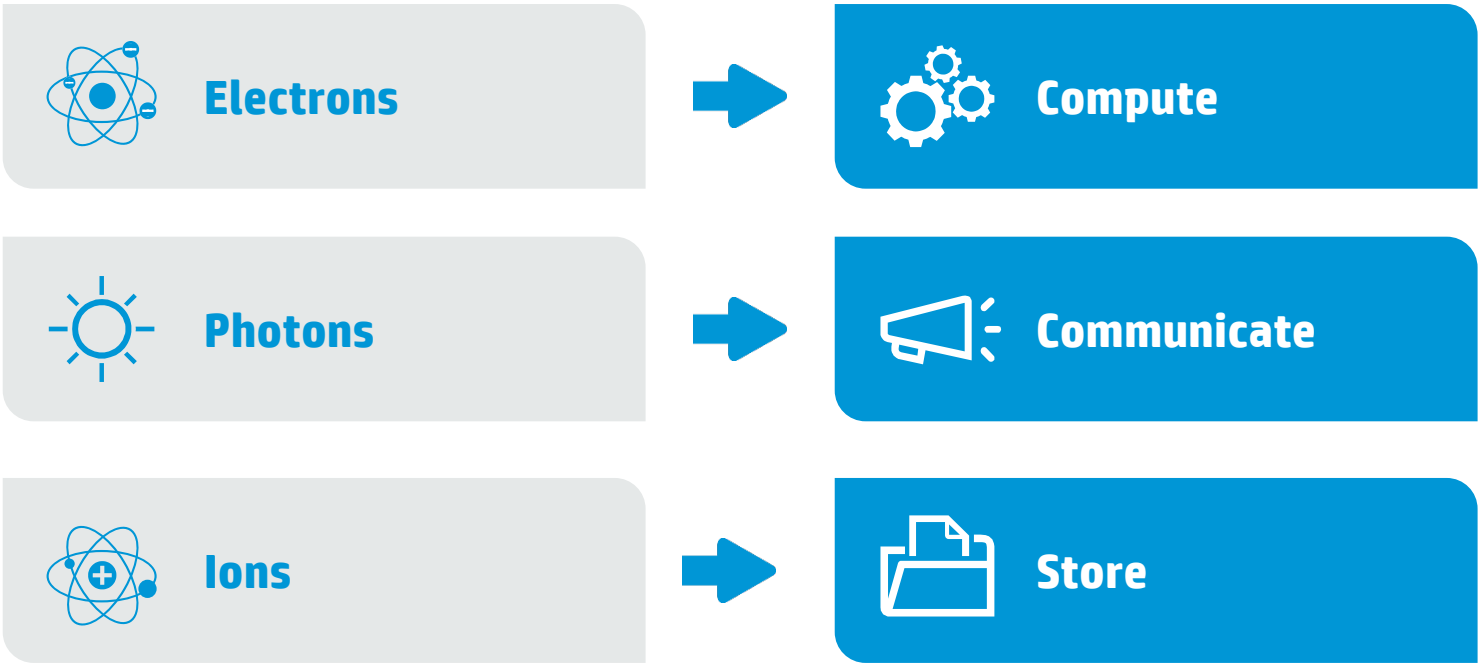
Data grows faster than computation

Data-centric workloads

From performance to efficiency

Scalability

HP’s “The Machine”



http://www.hpl.hp.com/research/systems-research/themachine/

Silicon Photonics is almost here

Luxtera and Kotura display first 100-gigabit QSFP modules

18/4/2013 0 Comments

Luxtera and Kotura have both demonstrated 100 Gbps QSFP optical modules based on silicon photonics technology.

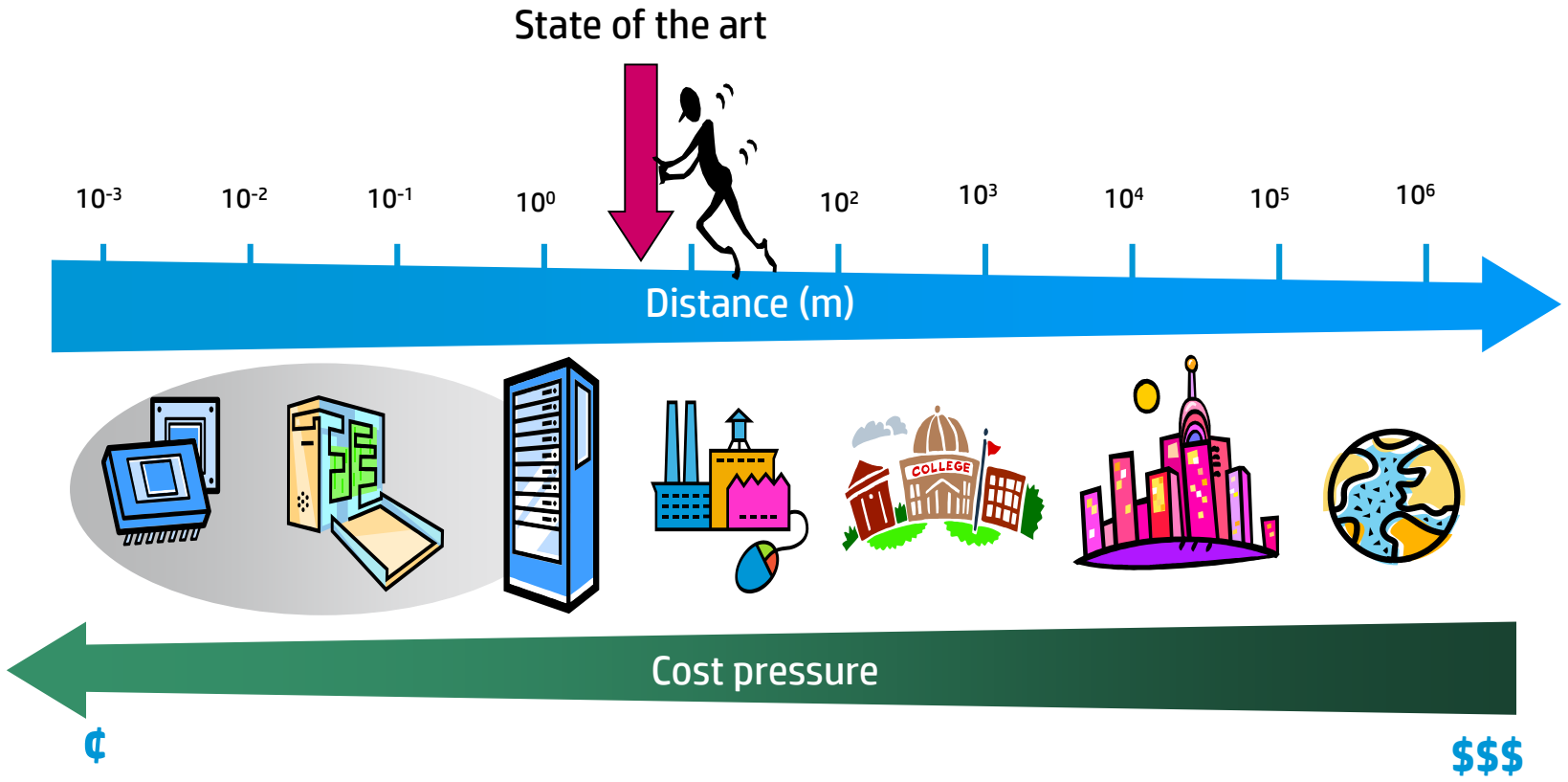
The Luxtera QSFP is a four-channel integrated transceiver that uses a single laser and is tailored for 500m although

Intel delays part for high-speed silicon photonic networking

Agam Shah
IDG News Service Feb 2, 2015 4:35 PM

Intel has delayed shipment of a component module required for its silicon photonics technology, which uses pulses of light to move data between servers at extremely high speed.

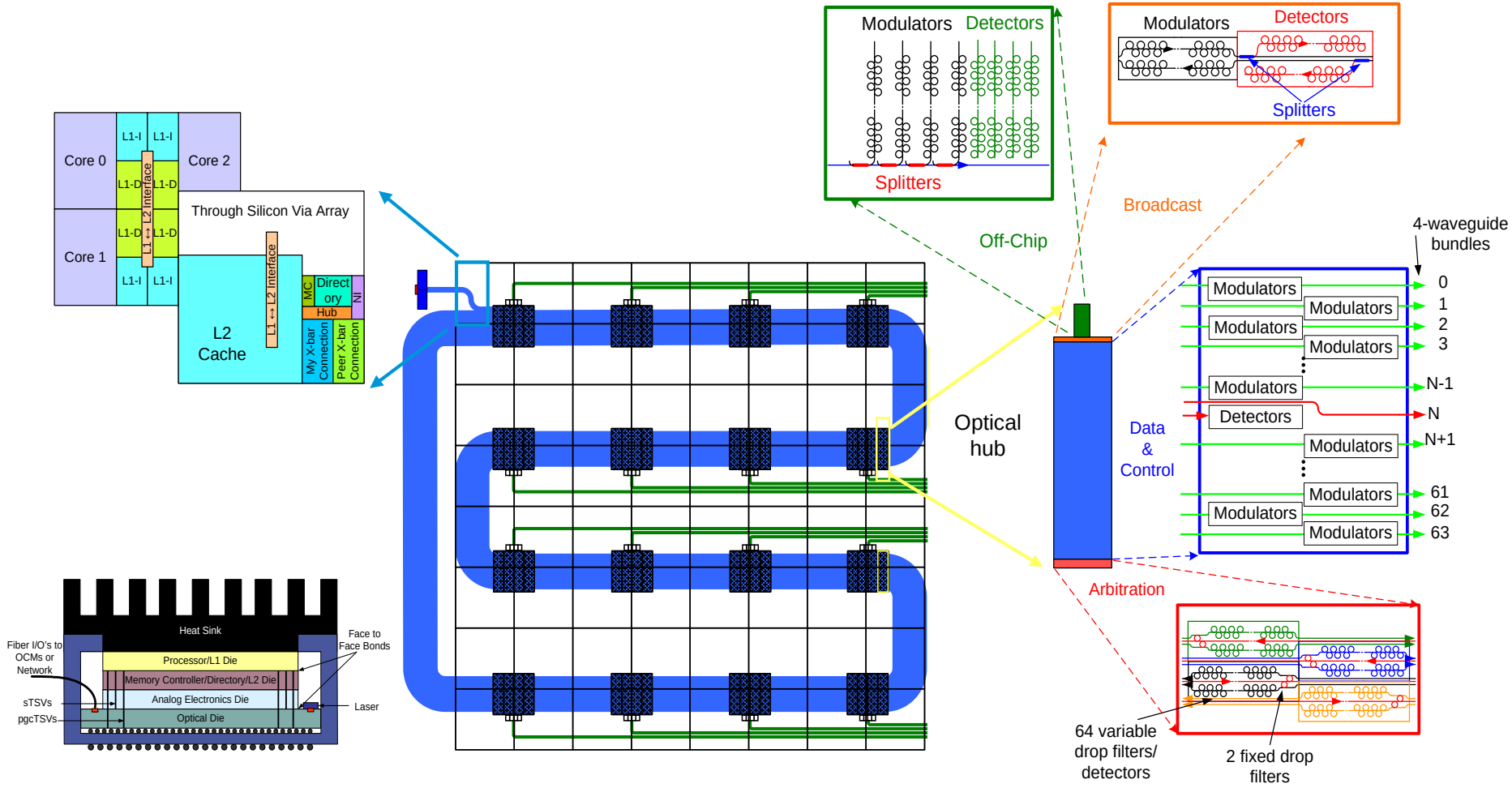
Optical interconnects



Advantages

More bits per “wire”	Less power per bit	Better signal integrity
New architectures		

Architecture example 1
HP Corona

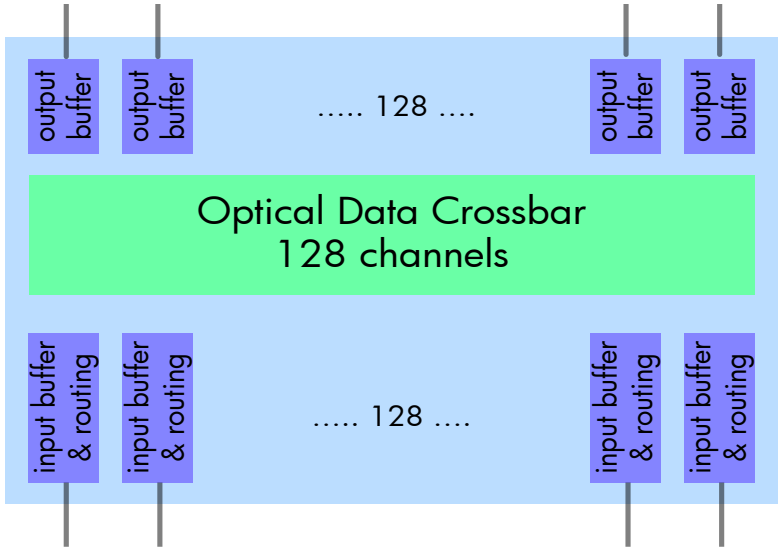


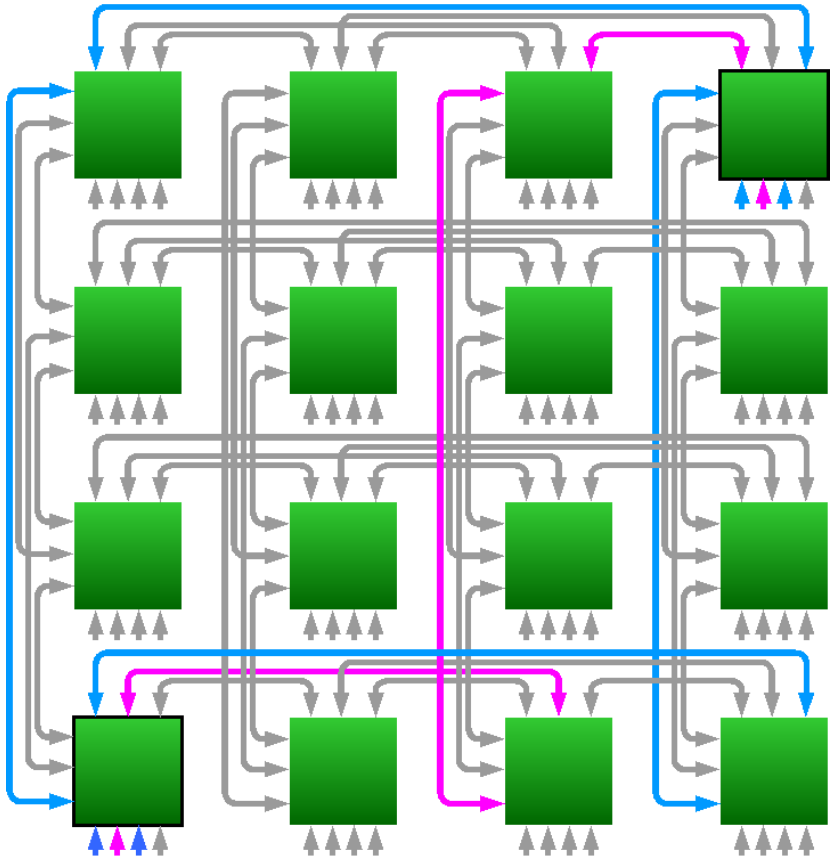
- Multiple-sender single-receiver links
- 1 byte/flop on chip and to memory
- 250W power envelope (compute + network)
- 20x improvement over electrical

Vantrease, Dana, et al. "Corona: System implications of emerging nanophotonic technology." *ACM SIGARCH Computer Architecture News*. Vol. 36. No. 3. IEEE Computer Society, 2008.

Architecture example 2
HP HyperX

- Crossbar used in high-radix switches
- Switch enables high connectivity topology

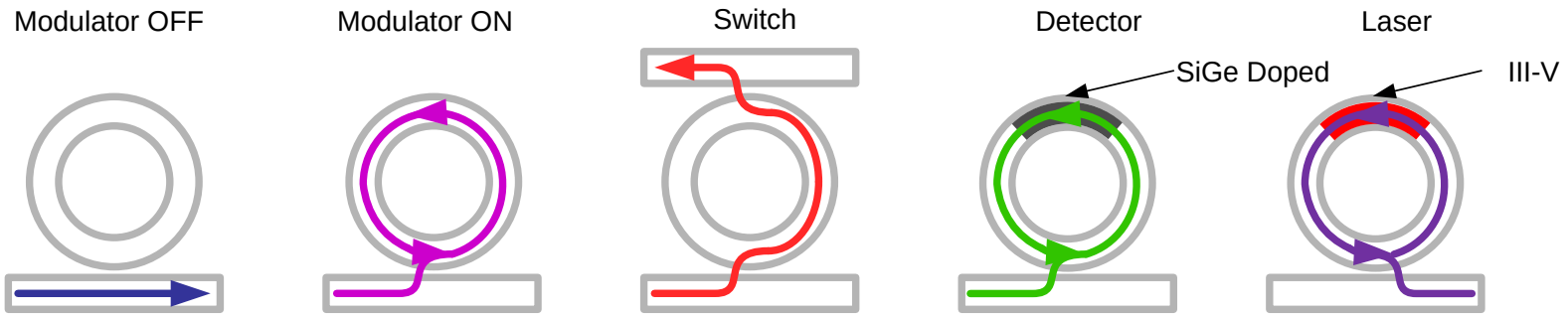




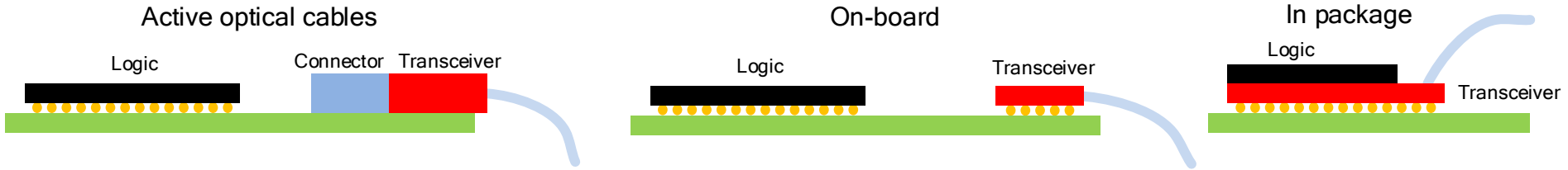
Ahn, Jung Ho, et al. "HyperX: topology, routing, and packaging of efficient large-scale networks." *Proceedings of the Conference on High Performance Computing Networking, Storage and Analysis*. ACM, 2009.

Technology requirements

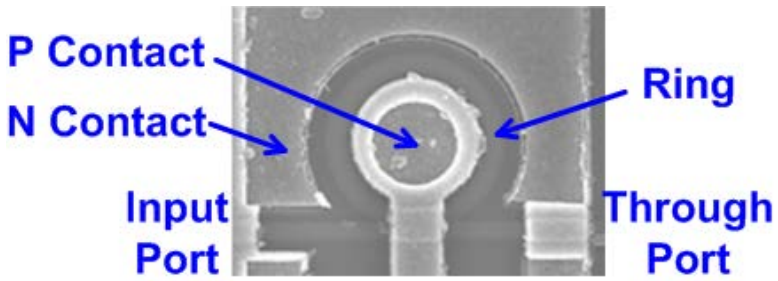
- **DWDM: bandwidth density**
- **Silicon photonics: cost and scalability**
- **Ring resonators: technology of choice**

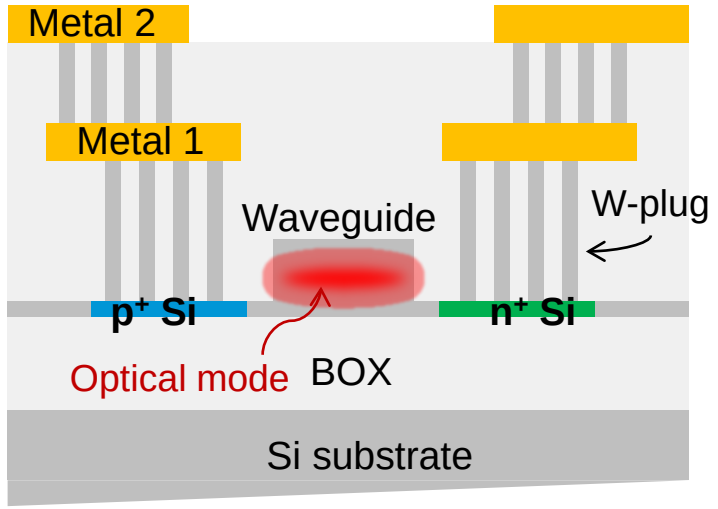


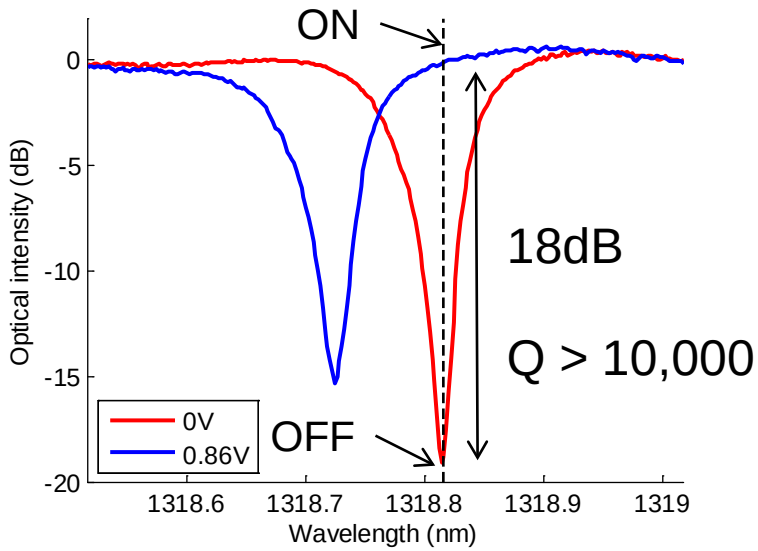
- **Packaging evolution**



Carrier-injection-based microring modulator







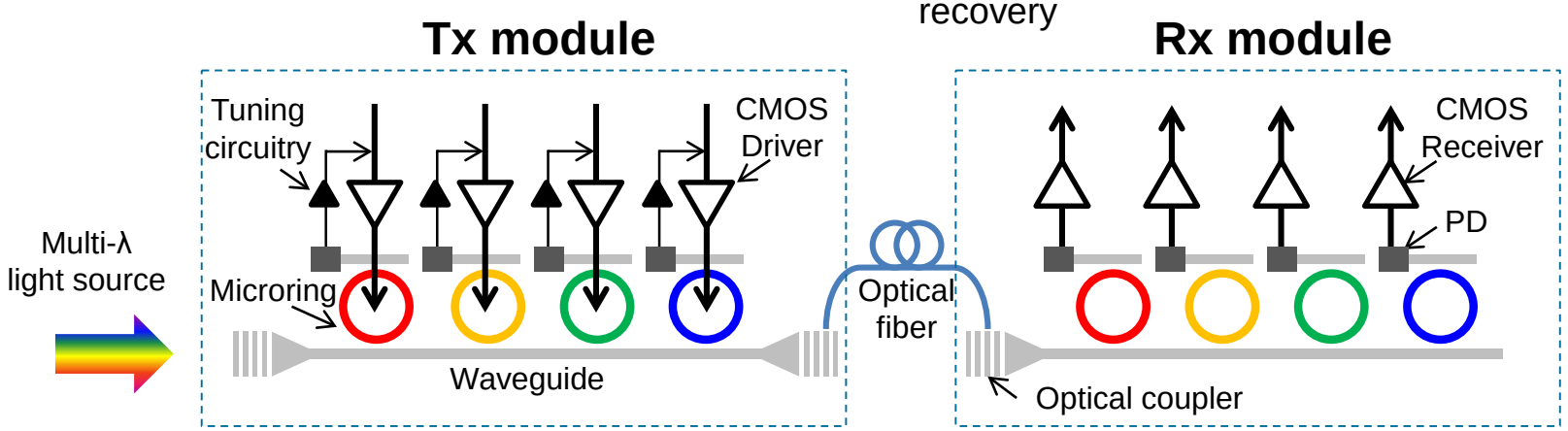
- P-I-N junction
  - → **low optical loss**
  - → **beneficial for link power budget**
- Large change in refractive index
  - → **high modulation depth**
  - → **beneficial for link power budget**
- Adjustable bias current
  - → **alternative tuning mechanism (blue-shift)**

- Slow carrier dynamics
  - → **pre-emphasis equalization**
- Sensitive wavelength shifts
  - → **closed-loop stabilization**

Si Photonics DWDM link

Transmitter
- Carrier-injection-based microring modulator
- Driver with pre-emphasis + thermal & bias tuning

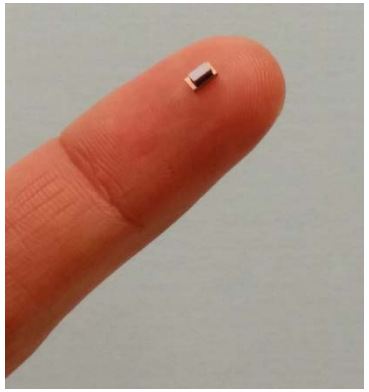
Receiver
- Drop filter + Ge waveguide Photodiode (PD)
- Self-adaptive data receiver + forward clock recovery

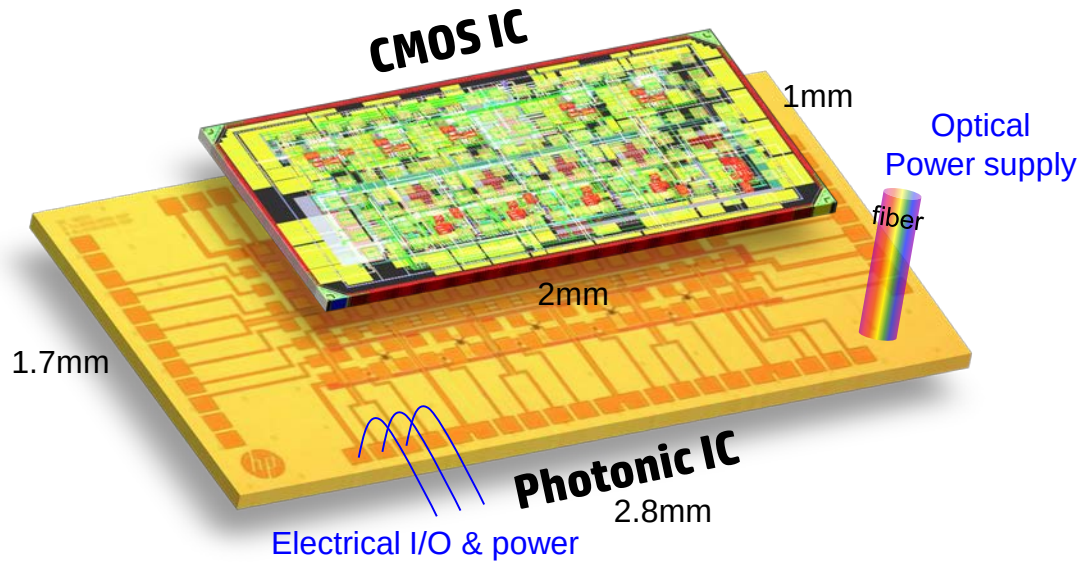


Comb laser
- InAs/GaAs quantum-dot Fabry-Perot laser module @ 1.3µm
- Multi-channels with 80GHz spacing at operating point
- Improved performance at higher temperature
- high wall plug efficiency (20%)

Hybrid integration
- 1st generation: wirebonding
- 2nd generation: flip-chip bonding

Prototype 5-channel transceiver



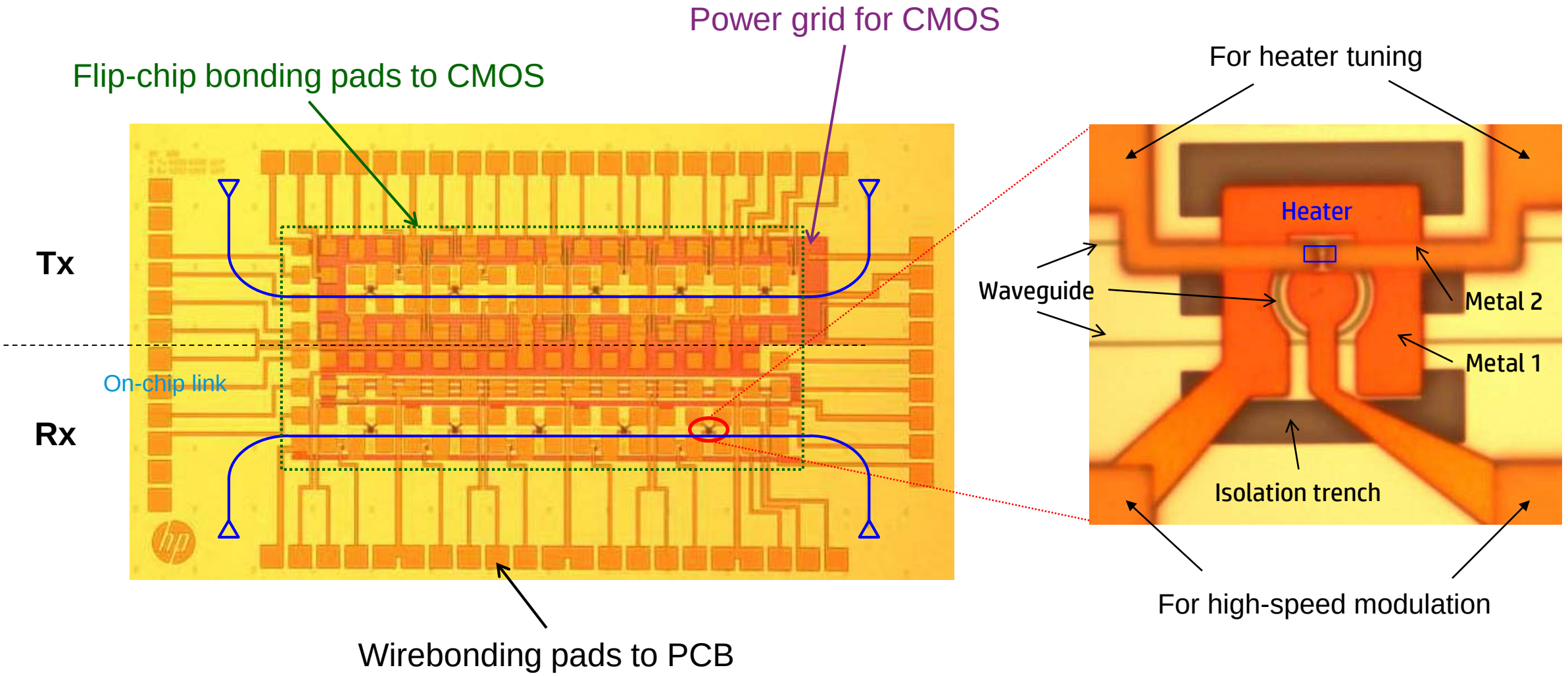


Tx: 5 microring modulators + integrated monitor PD + heater
Rx: 5 microring drop filters + integrated Rx PD + heater

Photonic chip manufactured by LETI

Footprint limited by flip-chip bonding pads and CMOS circuit (TSMC 65 nm)

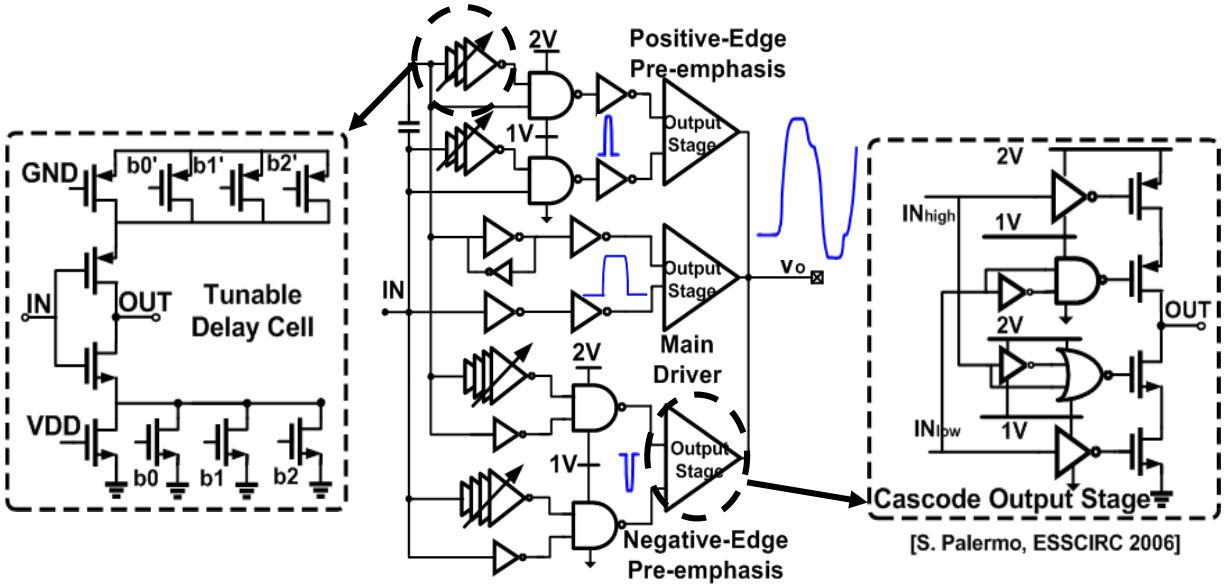
Photonic IC

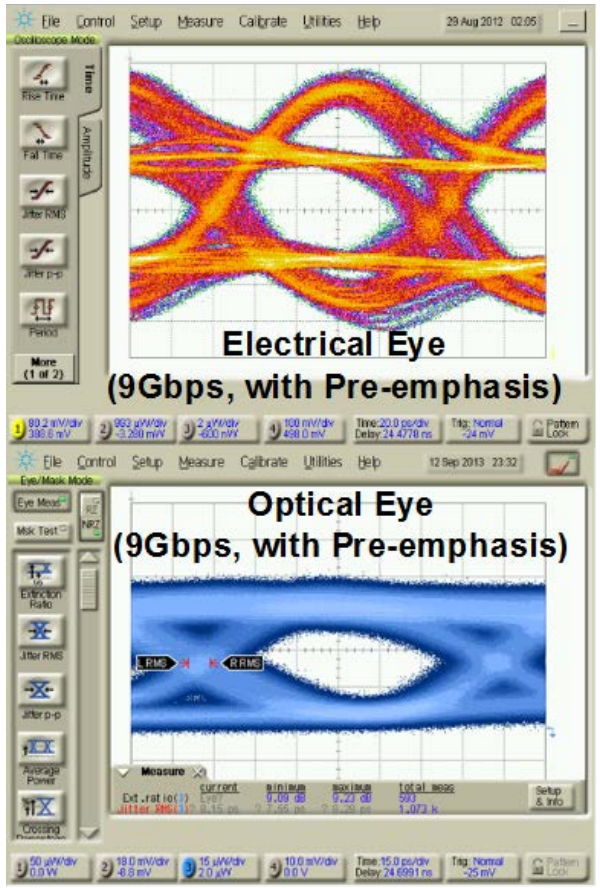


Transmitter results

Dual-edge pre-emphasis with pulse width controlled by tunable delay cells (30ps~60ps)

Cascode output stage used to meet high modulation swing requirement





Open problems and future directions

HP sees Photonics as the future of datacom

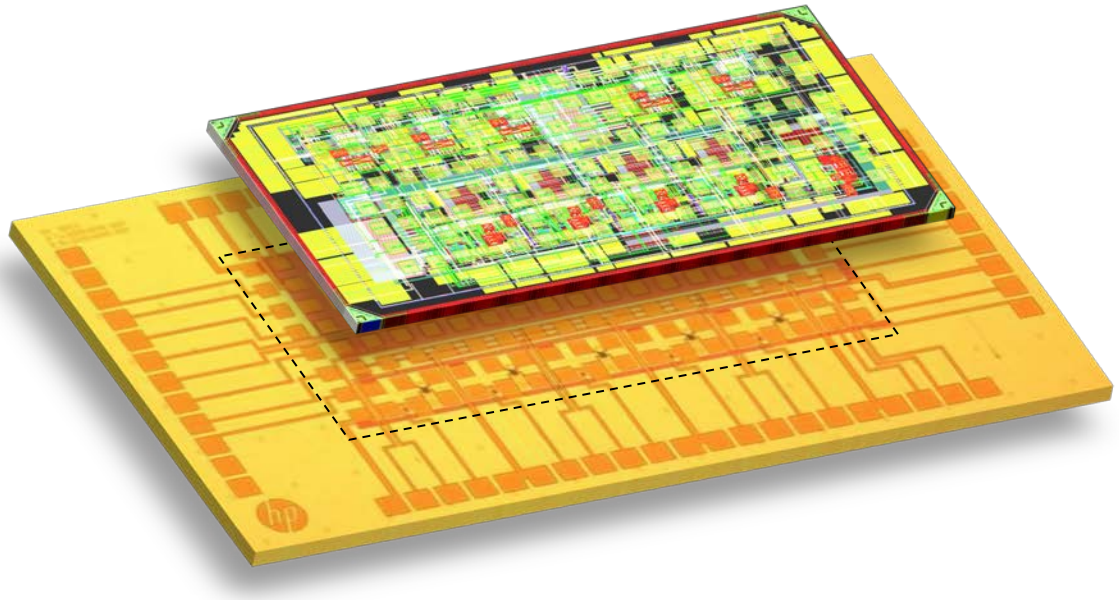
- Integration
  - How do we put it all together?
- Co-design
  - Drivers and receivers
- Fabrication
  - 1000s of devices on a chip?
- Power consumption and thermal

...and most importantly

Business case

Solution roadmap

Supplier ecosystem



Acknowledgements

HP Labs

- Ray Beausoleil (Group leader)
- Janet Chen (SiP design and testing)
- Cheng Li (CMOS design, area estimates)
- Al Davis & the architecture Group

CEA-Leti

- Sylvie Menezo & the SiP team

Our collaborators

- Sam Palermo at Texas A&M
- Patrick Chiang at Oregon State