Ultra-Thin Chips

- A New Paradigm in Si Technology -

Joachim N. Burghartz
• Ultra-thin chips: the paradigm shift

• Applications of ultra-thin chips
  – Traditional, recent and potential future applications
  – 3D ICs: Overcoming a bottleneck in CMOS scaling
  – Systems-in-Foil (SiF): enabler for new applications

• Ultra-thin chip fabrication
  – Post-process wafer thinning
  – Thin chips based on SOI
  – Chipfilm™ technology

• Characteristics of ultra-thin chips
  – Warpage of thin chips
  – Mechanical stability of thin chips
  – Apparently anomalous piezoresistive effect

• Constraints for circuit design

• Conclusions
Ultra-Thin vs. Thin Chips: the paradigm shift

- **Thick chips and wafers (conventional)**
  - 300 μm – 1000 μm:
    - Mechanically stiff and stable

- **Thin chips and wafers (conventional)**
  - 100 μm – 300 μm:
    - Mechanically stiff with limited stability
    - Reduced thermal resistance

- **Ultra-thin chips and wafers**
  - 50 μm – 100 μm:
    - Limited stiffness and limited stability
  - 10 μm – 50 μm:
    - Flexible with good stability
  - < 10 μm:
    - Flexible with good stability
    - Optically transparent
Properties of Ultra-Thin Chips and Wafers

• Mechanical
  – Warpage, curl-up
  – Young's modulus may deviate from bulk-Si value!
    – Rough edges, e.g. from dicing
    – Rough backside, e.g. from polishing
    – Topographic frontside from layer depositions

• Electrical
  – Piezoresistive effect
  – Backgate effects

• Optical
  – Absorption spectrum limited
  – Back-surface effects

• Thermal
  – Bi-material displacement
Processing Issues for Ultra-Thin Wafers/Chips

- **Front-end processes**
  - Handle/carrier substrates needed
  - Overheating effects (high-dose implant, RTP)

- **Back-end processes**
  - Excessive warpage from stress in interconnect layer stack

- **Packaging and assembly**
  - Edge chipping in dicing processes
  - Chip detachment from tape and transfer in assembly
  - Chip attachment to package
  - Mechanical pressure in wire bonding processes
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Bottlenecks in CMOS Scaling

3D chip stacking:
- Shorter interconnects
- Relaxed device dimensions
- Power-delay tradeoff (?)

Transistor
- Subthreshold slope
- Gate oxide thickness
- Shallow junctions
- # dopants in channel
- ............

Chip power

Interconnect Delay

Generation (nm)

Delay (ps)
• Smaller interconnect RC delays through shorter wires!

• Higher process yield through smaller chip area!
3D-IC Integration Concepts

**Wafer-to-wafer**
1. CMOS integration
2. Wafer thinning → Minimum thickness?
3. Through-chip vias → Via diameter?
4. Wafer attachment → Process yield?

**Chip-to-wafer and Chip-to-Chip**
1. CMOS chip
2. Chip thinning → Throughput?
3. Through-chip vias → Throughput?
4. Chip attachment → Process yield!
### Via Formation for VSI – *Via Metal Filling*

<table>
<thead>
<tr>
<th>Via Diameter</th>
<th>CVD of</th>
<th>Electroplating of</th>
<th>PVD of Seedlayer</th>
<th>Process for filling</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 µm</td>
<td>copper</td>
<td>copper</td>
<td>Ti:W/Cu</td>
<td>new!</td>
</tr>
<tr>
<td>3.5 µm</td>
<td>tungsten</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 µm</td>
<td>TiN</td>
<td></td>
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<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Aspect Ratio</th>
<th>10 µm</th>
<th>70 µm</th>
<th>100 µm</th>
<th>Via-Depht</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10:1</td>
<td>3:1</td>
<td>2:1</td>
<td>7:1</td>
</tr>
</tbody>
</table>

- **More than 10:1 aspect ratio is difficult to achieve!**
- **Need for ultra-thin chips postulated on ITRS Roadmap**

*Source: FhG-IZM*
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RF ID Tag

Warehouse storage

Department store sales

Roll-to-roll assembly

Low-cost printing

Source: Metro

Warehouse storage

Probable department store sales

Probable roll-to-roll assembly

Probable low-cost printing
Source: Unidym
Document Security

Source: NXP
Hybrid Systems-in-Foil

Thin Film Electronics
- **Pro:** devices widely spaced
- **Con:** low integration density
- **Pro:** flexibility

Si Integration
- **Con:** devices on chip
- **Pro:** high integration
- **Con:** thick Si chips

\[ \text{Pro: thin, flexible chips!} \]

→ Hybrid systems-in-foil = combining technologies with complementary merits!

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Process Technologies for Ultra-Thin Chips

Chipfilm™

Additive process

Subtractive processes

Wafer back thinning

SOI layer transfer
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Wafer Back-Thinning: Process Sequence

→ Economically practical wafer thickness >50 μm! (NXP)
Fast grinding processes introduce more defects than slow etch processes
Combination of fast grinding followed by defect removal steps
Process Effects on Mechanical Stability

- Ball-Ring-Method
  - 75 µm 10x10 mm²

- 3-Point-Method
  - 75 µm 10x10 mm²

→ Surface and edge quality of thin chips affect mechanical stability

Source: PVA-TePla
**Manufacture and transfer of 20 µm thin chips**

- **Prepare front side groves by etching or sawing**
- **Reversible bonding onto carrier and wafer thinning**
- **Chip separation by wafer thinning, transfer of thin dies**

**Wafer thinning:** Grinding, etching, polishing

→ **Improved edge quality and thus mechanical stability**

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Accidental detachment of Si-on-Glass
Lead to Philips’s Circonflex technology

Source: R. Dekker, Philips
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Chipfilm™ Technology

**Chipfilm™ Wafer**
- Buried cavities

**CMOS Process**
- Device integration

**Trench & Test**
- Anchor structures
  - lateral (Chipfilm™-I)
  - vertical (Chipfilm™-II)

**Pick, Crack & Place™**
- Chip singulation

*IEDM 2006 Late News: Introduction of Chipfilm™-I*

*IEDM 2010: Introduction of Chipfilm™-II*

*Since July 2008: Joint development with Robert Bosch GmbH*
Chipfilm™ vs. Back-Thinning

### Pre-Process

<table>
<thead>
<tr>
<th>Standard wafer thinning</th>
<th>CMOS</th>
<th>Assembly</th>
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<tbody>
<tr>
<td>-</td>
<td>Thinning → Dicing → Packaging</td>
<td>Thinning and dicing → Handle wafer → Handle wafer → Handle wafer</td>
</tr>
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**Wafer thinning for very thin chips**

- Chipfilm™ Technology

**Chipfilm™ Technology**

- Pick, Crack and Place™

*CMOS Pre-Process: Standard wafer thinning leads to Thinning, then Dicing, followed by Packaging.

*Assembly Pre-Process: Wafer thinning for very thin chips involves Thinning and dicing, followed by the placement of Handle wafers and Packaging.*
The Chipfilm™ Pre-Process

Step 1:
- **Anodic etching of a Si wafer**
  - Dual porous Si formation
  - Masking through $n^+$ doping

Step 2:
- **Sintering in oxygen-free ambient**
  - Silicon reflow
  - Fine porous Si $\rightarrow$ Nano grains
  - Coarse porous Si $\rightarrow$ Buried cavity

![Diagram showing the process steps](image-url)
The Paick, Crack & Place™ Post-Process

Pick, Crack & Place of Thin Square Chip
Technology Comparison

- **Chipfilm™-I**  
  - Continuous cavity  
  - Lateral anchors
  
  **Pros:**  
  + Thickness limit < 20μm

  **Cons:**  
  - Surface steps (~ 200nm)  
  - Predefined chip size

- **Chipfilm™-II**
  - Discontinuous cavity  
  - Vertical anchors

  **Pros:**  
  + Thickness limit < 20μm  
  + High planarity ($r_{avg}$ ~ 7nm)  
  + Generic wafer substrate
• **Pre-process module (I)**
  - n-implant
  - anodic etching
  - thermal annealing
  - epitaxial growth

• **Device Integration**

• **Post-process module**
  - Trench etching
  - Chip detachment
Chipfilm™-II Technology Process

• Pre-process module (I)
  – n-implant
  – anodic etching
  – thermal annealing
  – epitaxial growth

• Device Integration

• Post-process module
  – Trench etching
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