IEEE SCV-SF Electron Devices Society Seminar

Device and Process Variability

Tomasz Brożek

PDF Solutions Inc.

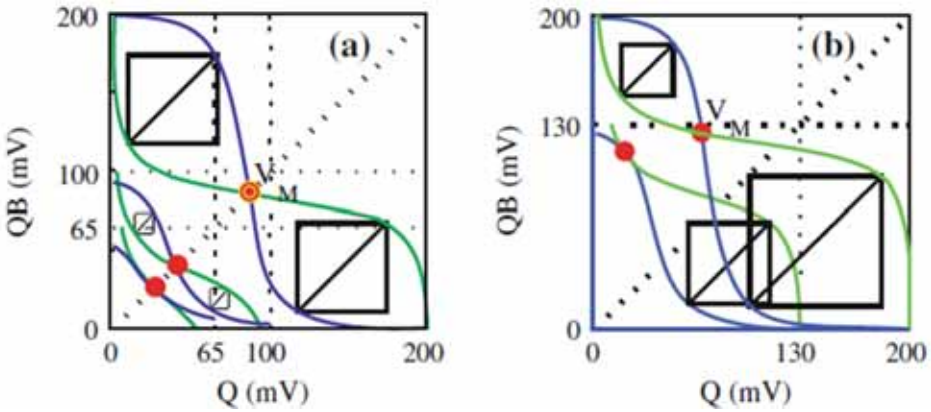
Santa Clara, 12 June 2017

Outline

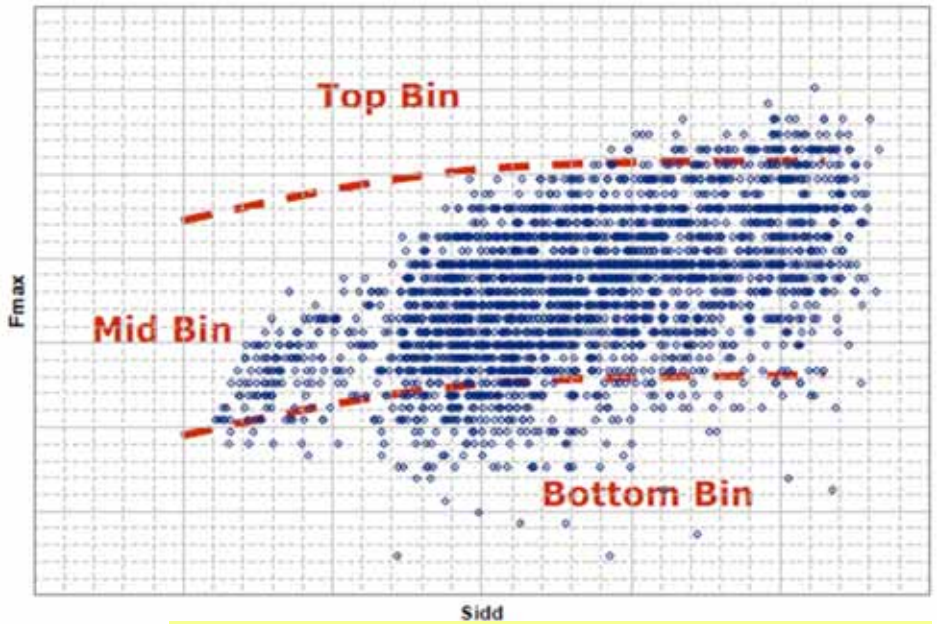
- Why does it matter – Impact on parametric yield, speed, leakage
- Device variability – historical perspective and technology trends
- Sources of Variability and Process dependence
- Local Layout Effects and their Characterization
- Process variability and Characterization
- eMetrology for better process control in advanced nodes

Consequences of Device variability

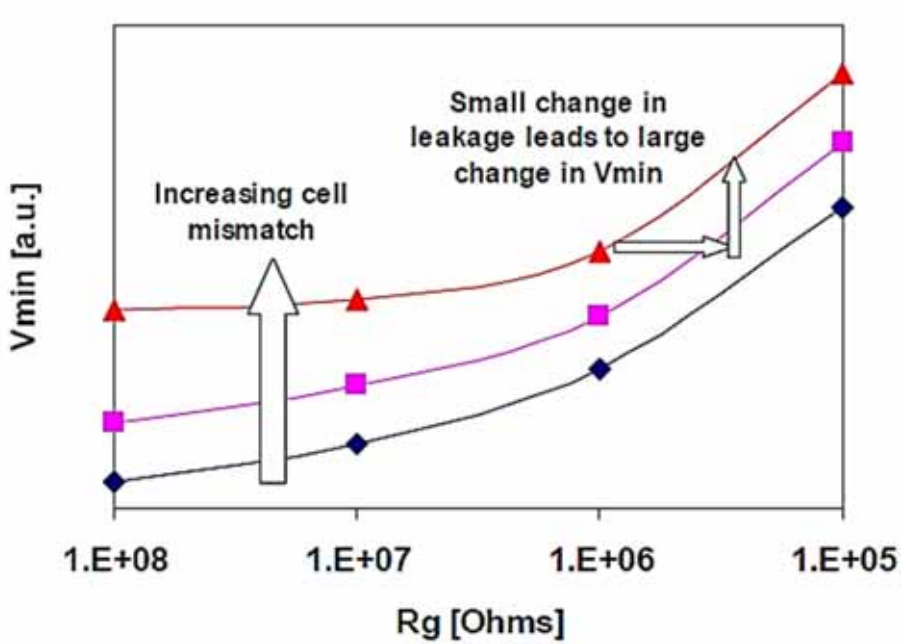
- Processor Speed variability
- Excess Leakage Currents (IDDQ failures)
- SRAM Vmin margin



Balanced and dis-balanced Cells due to Vt mismatch



Source: J. Farrell, AMD, C2S2 Workshop, UCB'2006

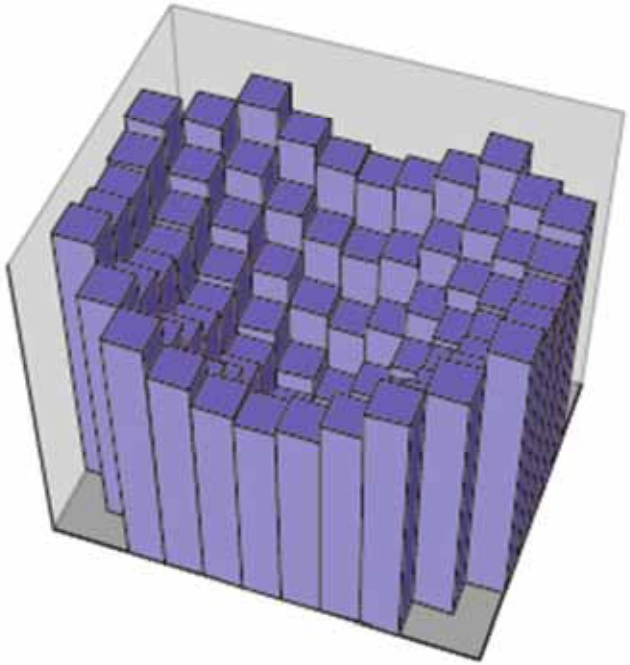


Source: M. Agostinelli, Intel, IRPS'2005

Static Process Variations

After A Strojwas, Tutorial "Variability and DFM", Short Course, VLSI Tech Symp'2014

Die-to-Die (D2D) Variations

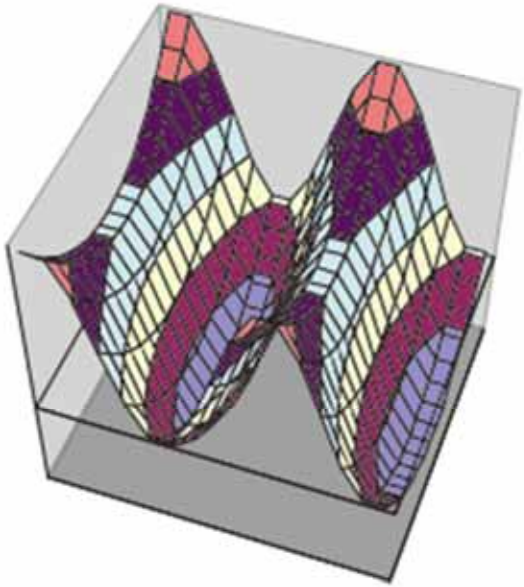


Wafer Scale

E.g., across the Wafer dielectric deposition thickness uniformity or Anneal Temperature

Within-Die (WID) Variations

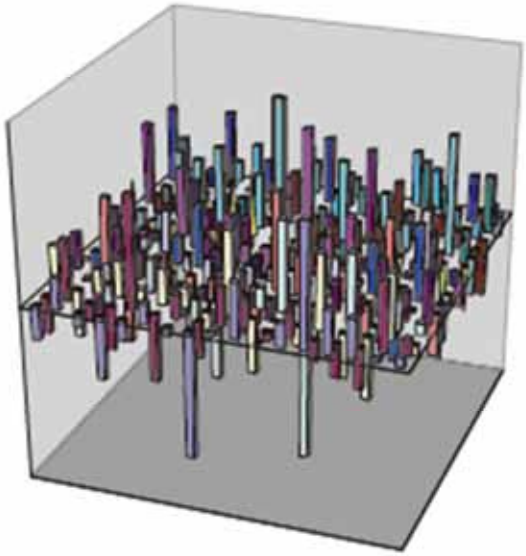
Systematic



Die Scale

E.g., across the Die CMP uniformity (Gate height) or Die level Litho Overlay

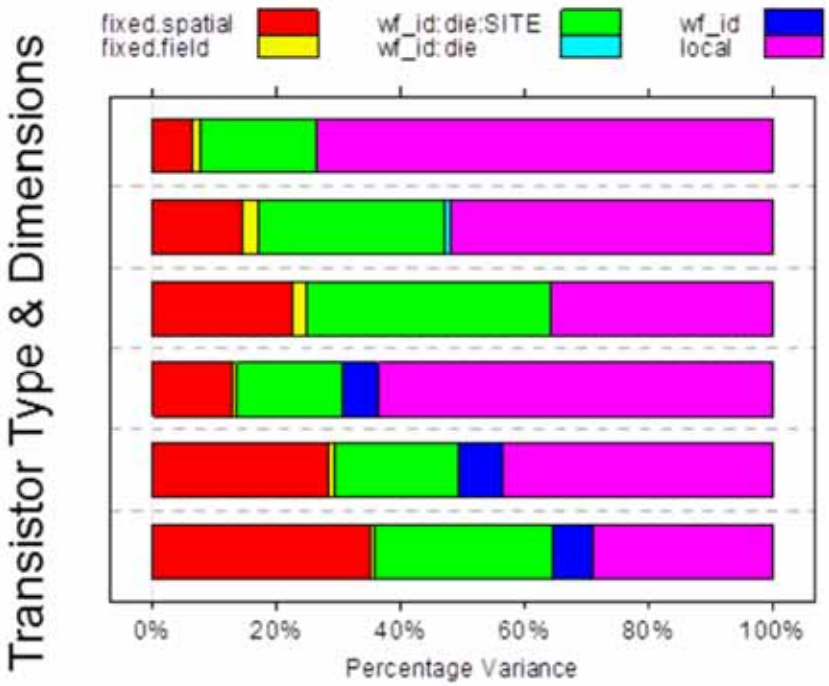
Random

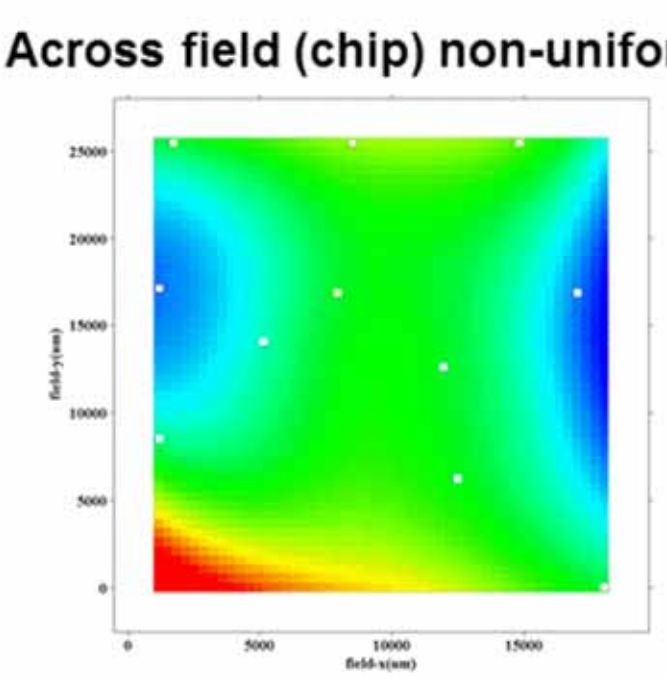


Feature Scale

E.g., local variation in CD (LER) or Dopant Atom count in the channel

Variability Decomposition





- **Variability characterization and decomposition**
  - Provides information for variability reduction

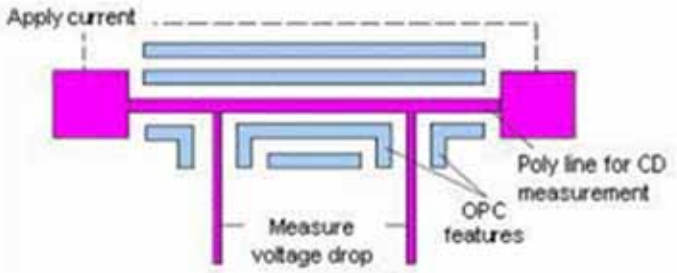
After A Strojwas, Tutorial "Variability and DFM", Short Course, VLSI Tech Symp'2014

PDF SOLUTIONS

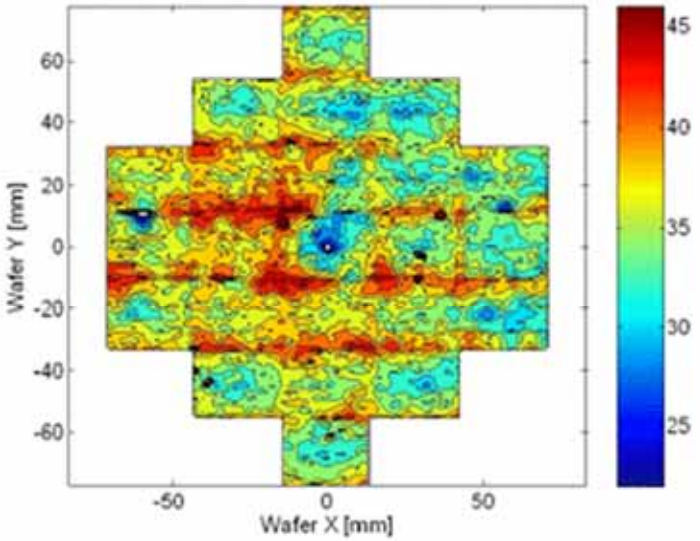
Example of Decomposition of Process Parameters

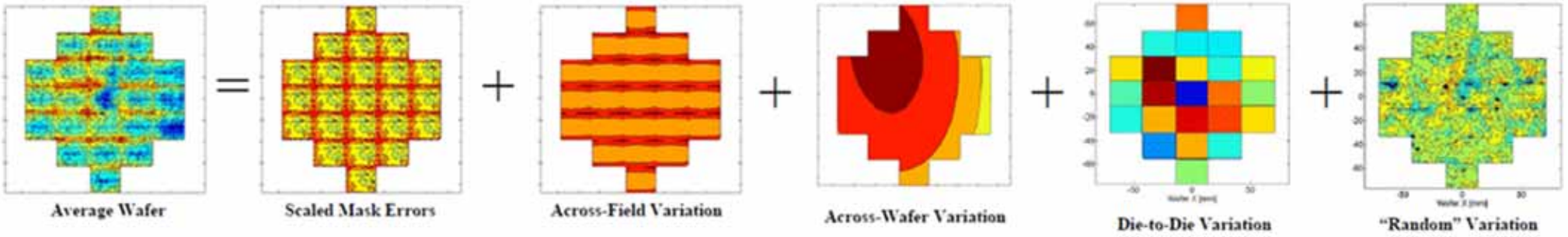
Gate CD Variability

- Electrical Poly CD measurement
- 280 Measurements/Reticle Field



Combine voltage drop measurements with sheet resistance measurements from neighboring Van der Pauw structures to get CD



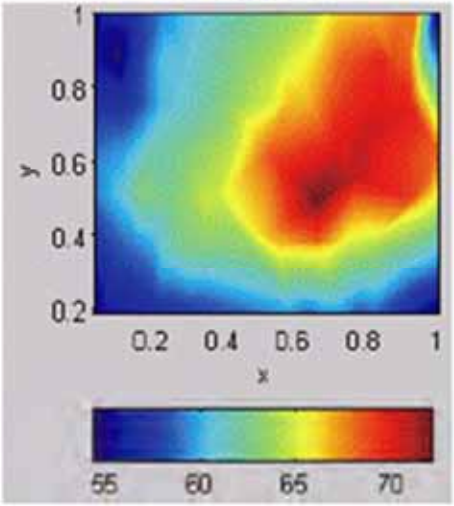


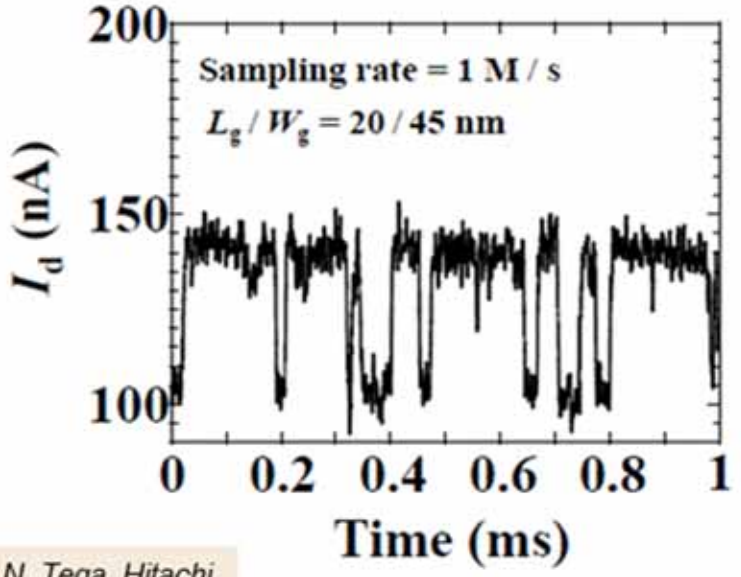
After: Prof. C. Spanos Group SPIE 2003/2006

PDF SOLUTIONS

Dynamic Variations

Thermal

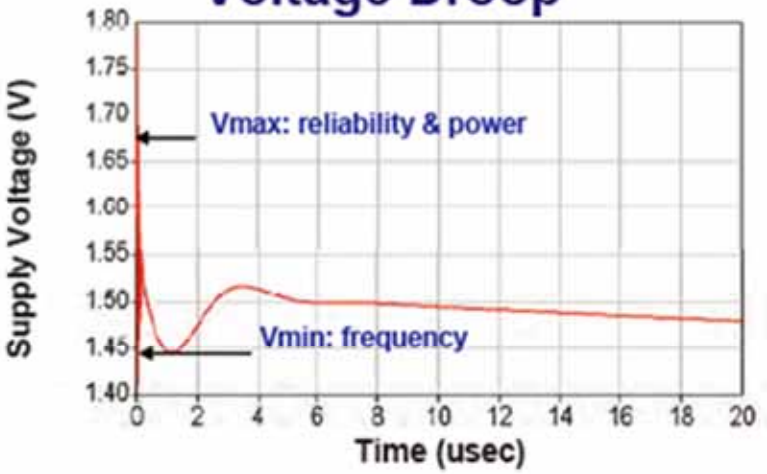




N. Tega, Hitachi, IRPS'2011

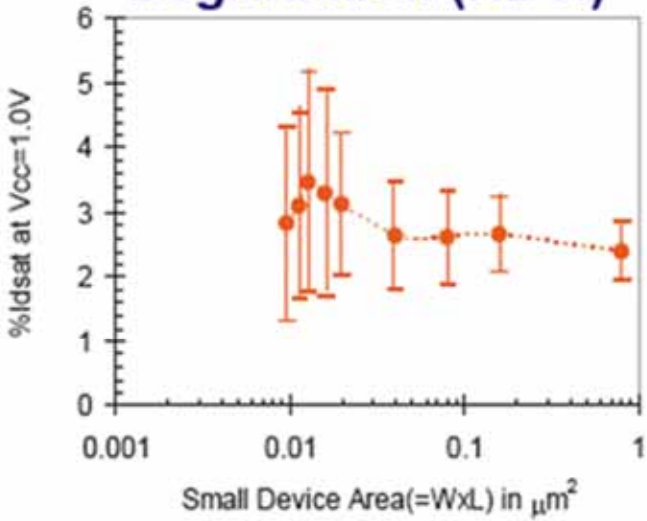
Typical RTN dependence on time.

Voltage Droop



After A Strojwas, Tutorial "Variability and DFM", Short Course, VLSI Tech Symp'2014

Degradation (NBTI)



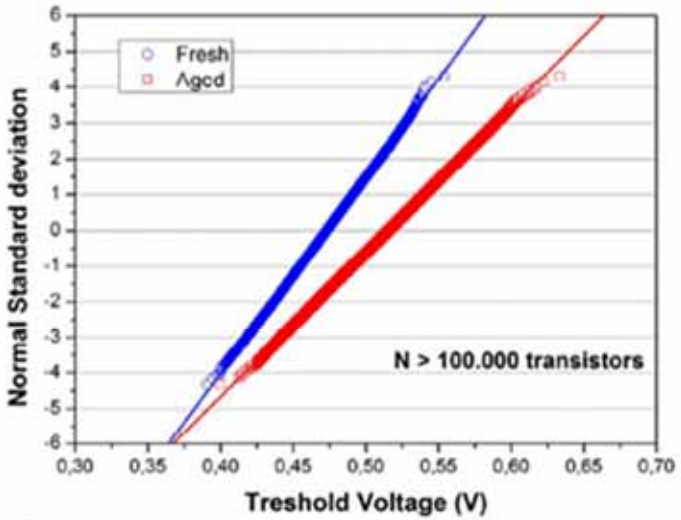
Agostinelli et. al, IEEE Intl. Reliability Physics Symp, 2005

6

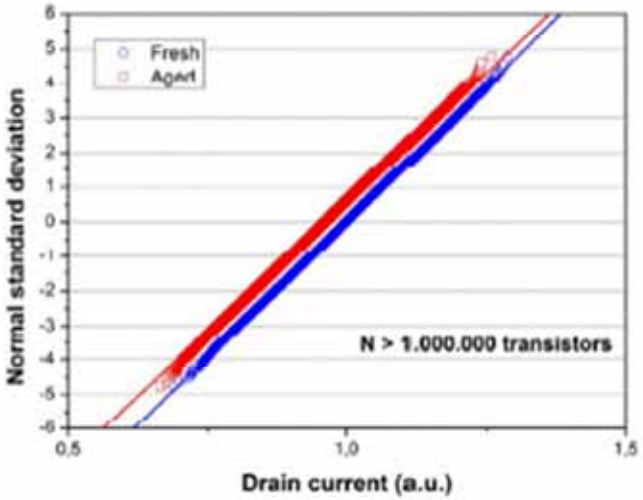
PDF SOLUTIONS

Dynamic Variability - Bias Temperature Instability

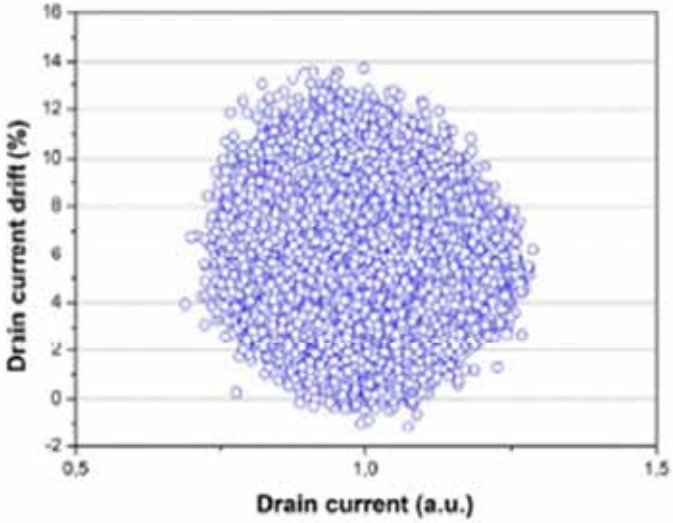
- Study of impact of aging on device parametric variability over multiple nodes
- Large number (>1000000/wafer) needed/used to generate statistics & model accurately
- Key observations / conclusions
  - Fresh and stressed device show a normal distributions
  - Shift distributions have a tail which impacts lifetime prediction
  - NBTI matching in PMOS is increasing with respect to time-zero matching. Similar root cause of the BTI behaviour



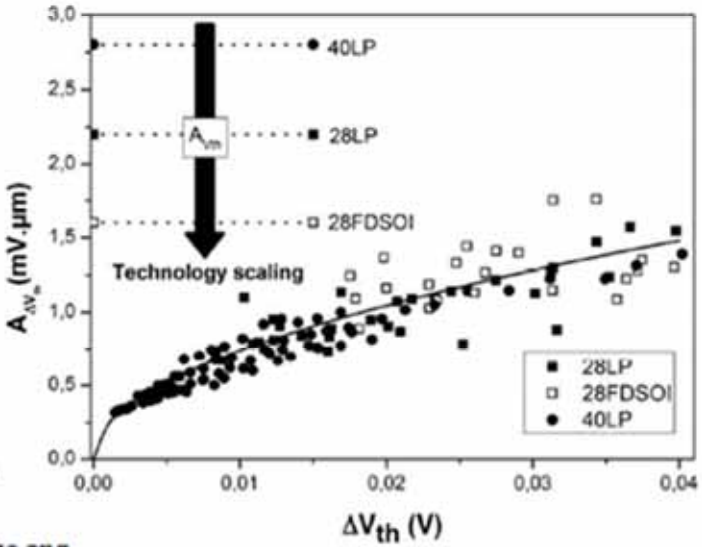
. 3. V_{th} distributions for 130.000 28FDSOI 0.3x0.022µ
istors prior (circles) and after BTI stress (squares) showin



Drain current distributions for very large dataset
1.000.000 28FDSOI 0.3x0.022µm² transistors prior (circles),
after BTI stress (squares) showing no deviation to normality.



Correlation plot between initial drain current value and
current drift after BTI stress, showing the absence of correlation.



Time-zero matching and BTI matching for three technology nodes. The BTI matching remains identical for these three nodes

Source: D. Angot, ST Micro, IEDM'2013

PDF SOLUTIONS

Outline

- Why does it matter – Impact on parametric yield, speed, etc
- Device variability – historical perspective and technology trends
- Sources of Variability and Process dependence
- Local Layout Effects and their Characterization
- Process variability and Characterization
- eMetrology for better process control in advanced nodes

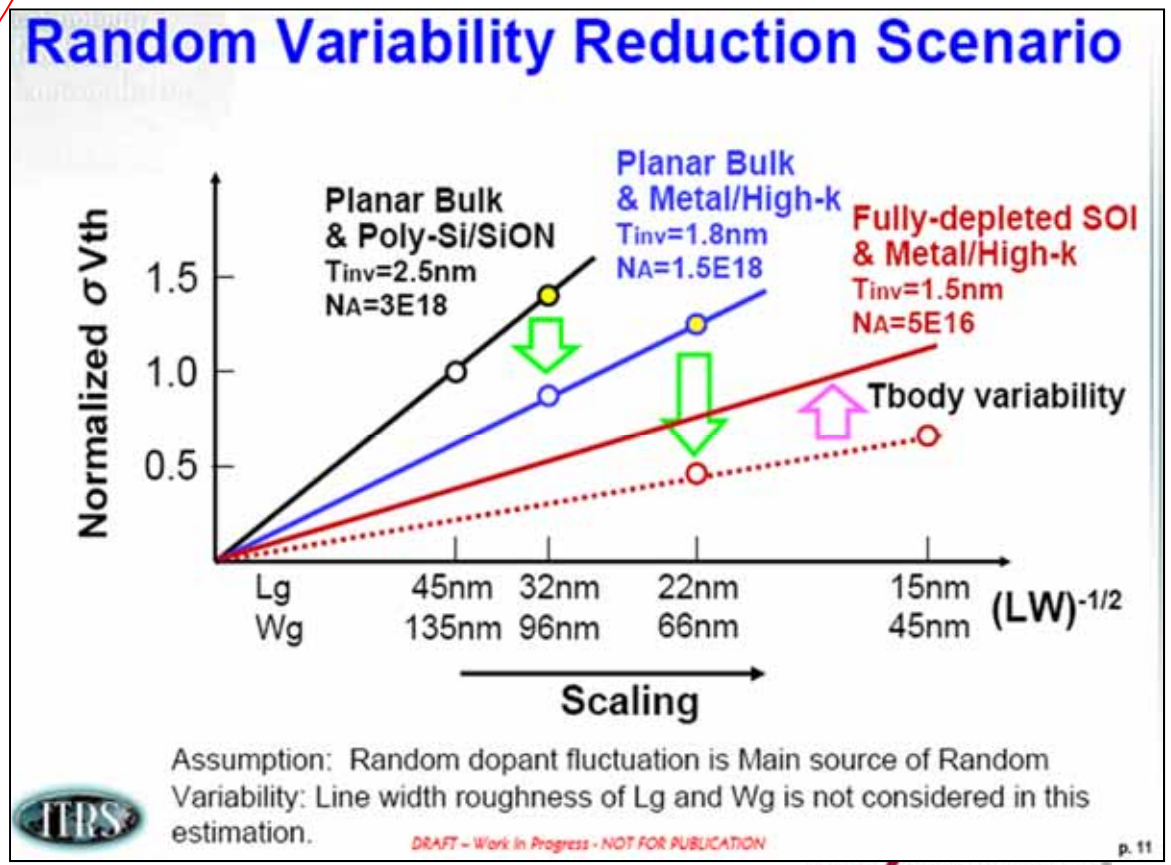
Variability dependence

- Threshold Voltage Variability is a function of Device Size → 1/sqrt(LW)
- Proportionality Coefficient depends on Tox and Channel Doping

$$\sigma(Vth) = \frac{K \times T_{ox}}{\varepsilon_{ox}} \frac{\sqrt[4]{N}}{\sqrt{LW}}$$

Lower doped substrates by using gate φ_M to set V_{TH}

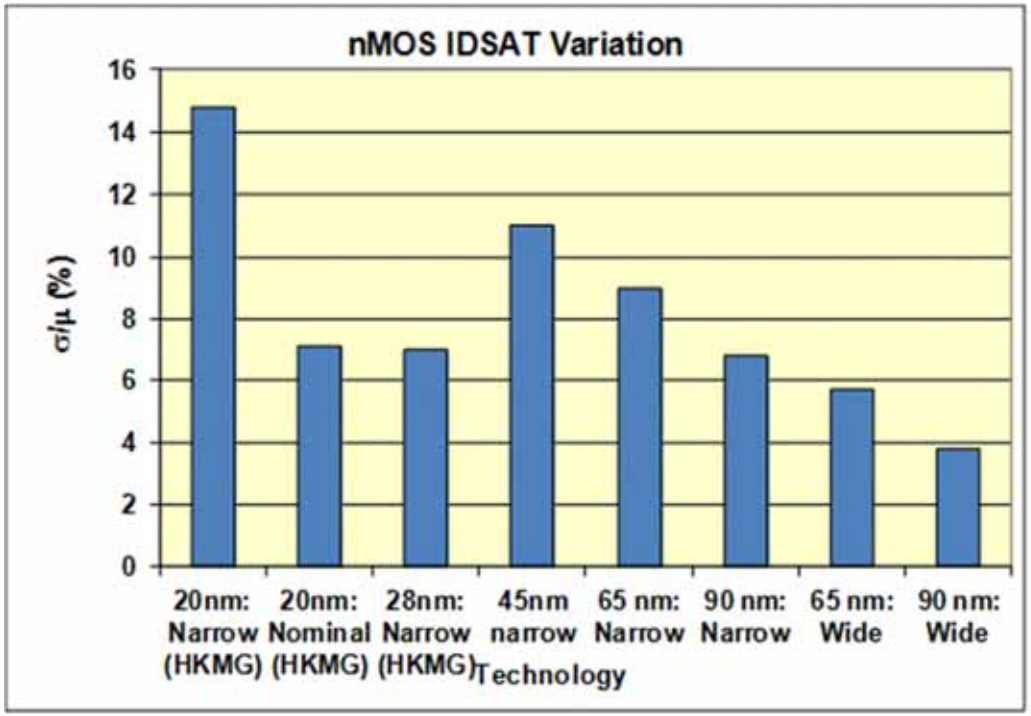
Improved by high-k & gate dielectric scaling

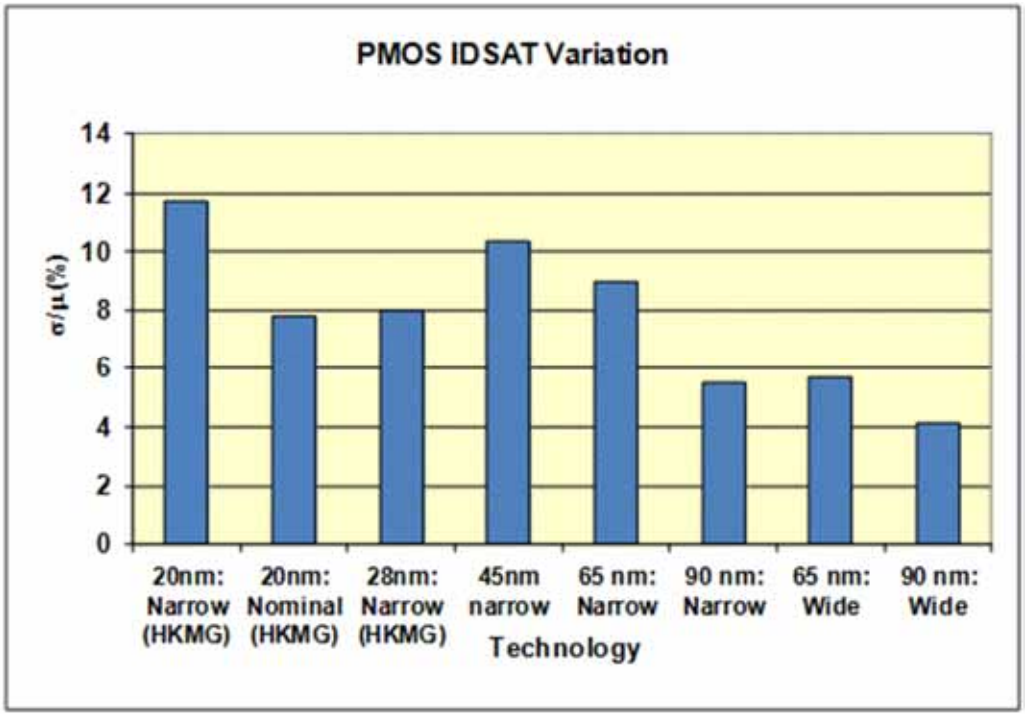


Metal gate/high-k enabled further scaling and reduced variability, but introduced new sources of variation

PDF SOLUTIONS

Variation Trends: Random Variations





Source: Internal PDF Benchmark

- **Identical structure data presented here (no systematic layout dependent effects included)**
- **As expected, HKMG has reduced random variations.**

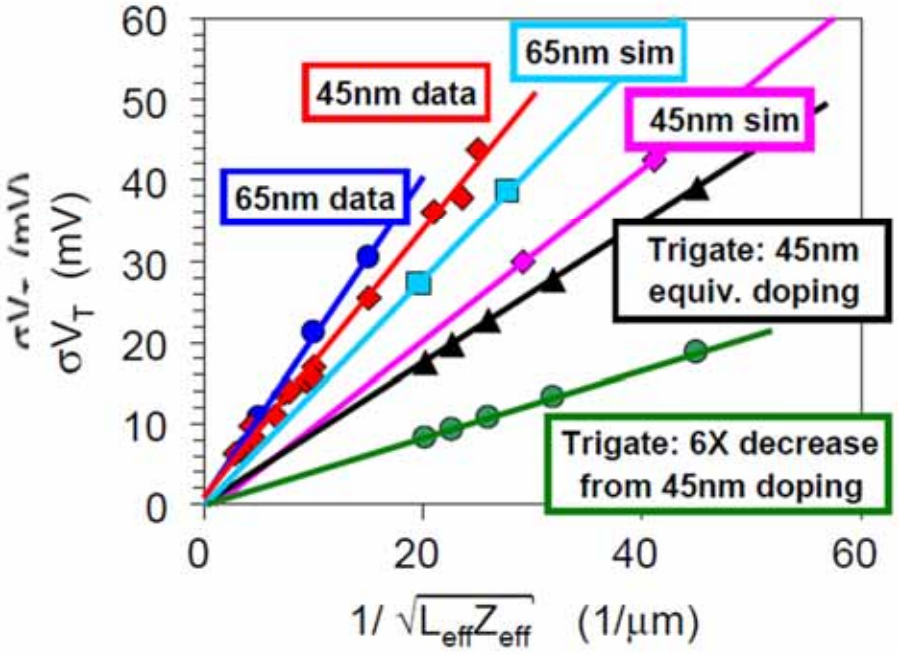
  However, systematic layout pattern driven variations have increased
- **20nm – very short node**

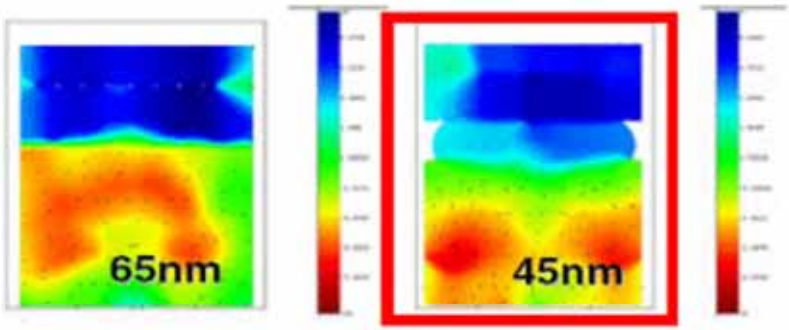
After A Strojwas, Tutorial "Variability and DFM", Short Course, VLSI Tech Symp'2014

PDF SOLUTIONS

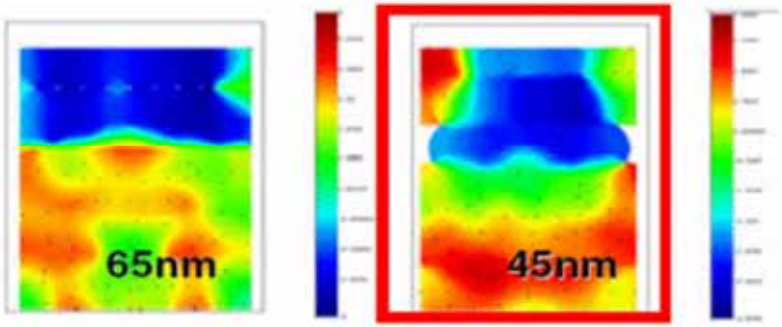
Variability reduction with HK-MG

- **Demonstrated Variability improvement in 45 nm**



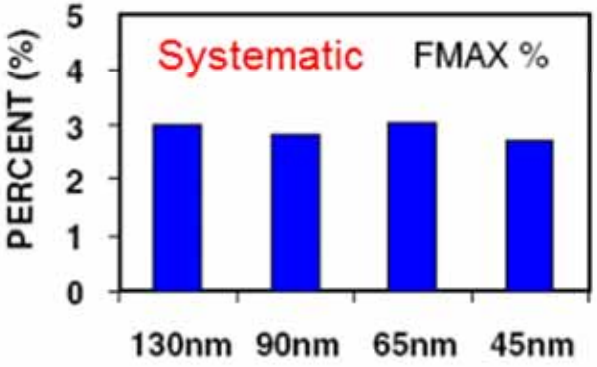


VTN variation (Mean die VTN – VTN)
Range: 20mV for 65nm → 11mV for 45nm



VTP variation (Mean die VTP – VTP)
Range: 9mV for 65nm → 7mV for 45nm

Intel within wafer Variation



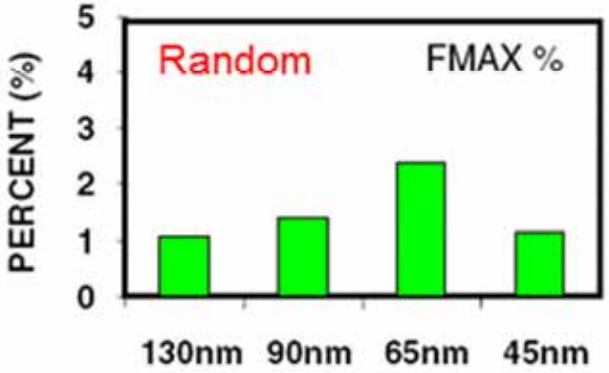
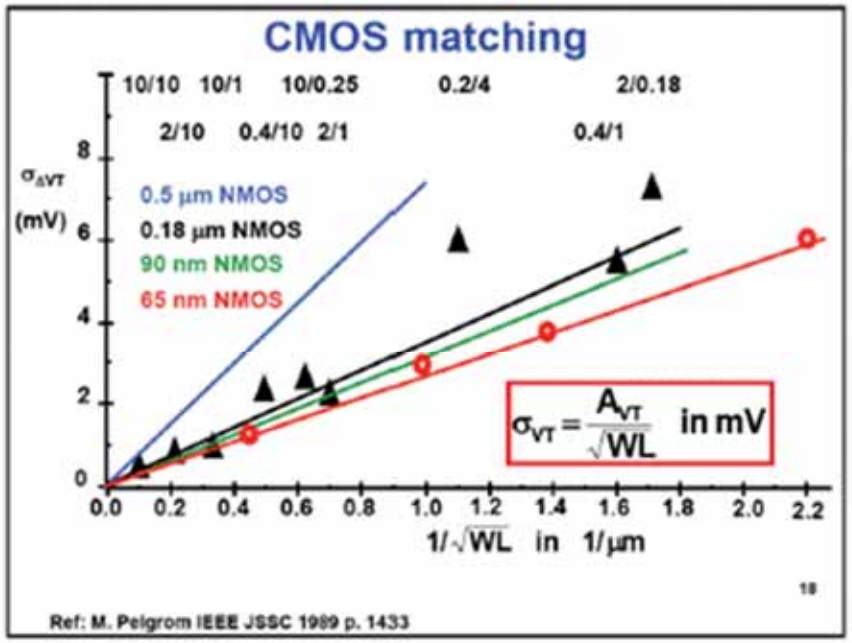


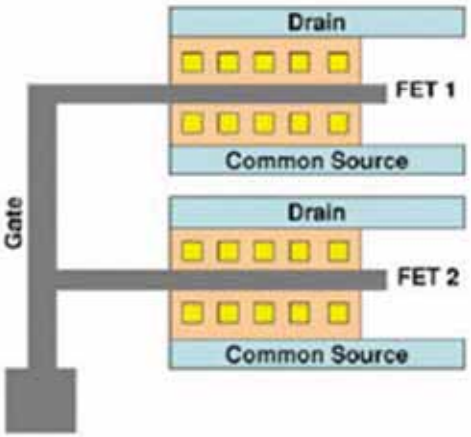
Figure 25: Ring-oscillator data (used in conjunction with a calibration structure) to extract 65nm to 45nm systematic within-die NMOS and PMOS V_T variation illustrating the improvement is enabled by HiK+MG between the 65nm and 45nm generations

Source: Intel, IEDM 2007, TechJour., 2008

PDF SOLUTIONS

Variability - Scaling Trends





$$\sigma V_T = \sigma \Delta V_T / \sqrt{2}$$

$$\sigma \Delta V_T = A_{VT} / \sqrt{WL}$$

$$\sigma V_T = C2 / \sqrt{WL}$$

After: Prof. A. Asenov, GSS, SC IEDM'2015

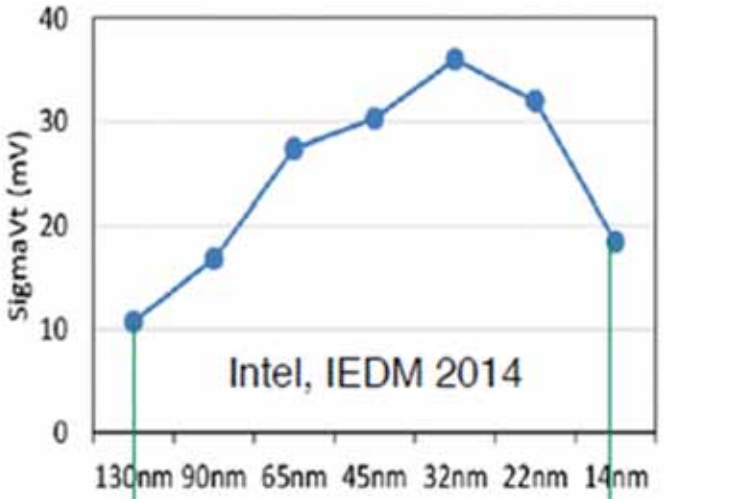
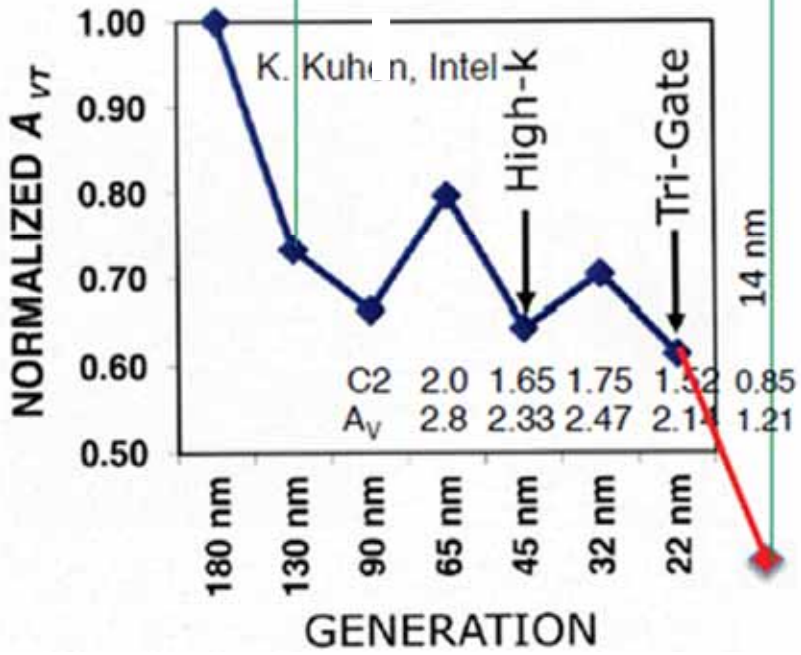


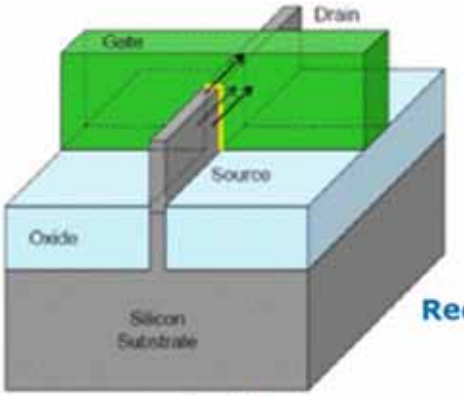
Figure 7: Random Varation Trend (σVt)



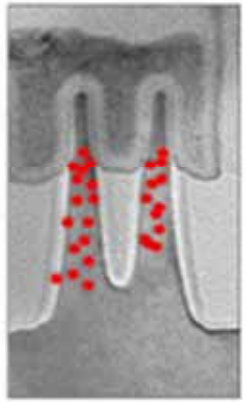
FinFET – Device of choice for Advanced nodes

FinFET: Many Additional Sources of Variation

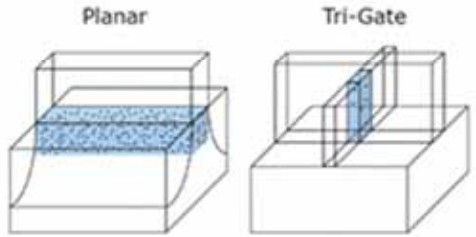
- Multiple sources of variation (WID, WIW, WTW)
  - Fin height
    - Variation from : STI dep, STI CMP, wet etch
  - Fin width
  - Fin shape
  - Fin doping
  - Fin line edge roughness
  - Fin side wall plane
  - Gate LER (gate etch over fin topography)
  - Etched fin plane interface traps
  - Additional Epi variation (growth on etched plan)
  - SDE doping along fin height



Source: Intel



Reduced Channel Doping



M. Bohr, Intel,

Fully depleted Tri-Gate structure has reduced channel doping, providing improved performance and reduced variability

IDF2012

Additional variation will be one of biggest challenges for SOC

After S.Thompson, U. Florida, Device Tutorial, IEDM'2015

PDF SOLUTIONS

Variability in FinFET – parameter contribution

- **Experimental study of effective current (Ieff) variability in 14nm SOI FINFETs is reported which identifies:**
  - threshold voltage (Vtlin)
  - external resistance (Rext)
  - channel transconductance (Gm)

  as three independent sources of variation
- **Gm variability dominates overall Ieff variability for 1-2 Fin device, while Rext variability becomes important for high Fin count**

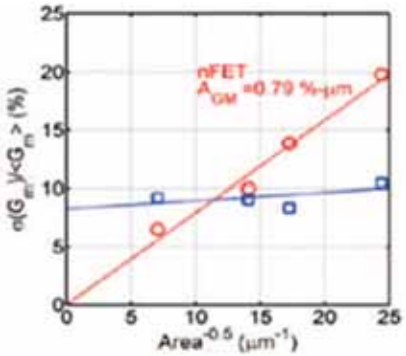


Figure 13: $G_{m,max}$ variation shows Pelgrom nature for n/pFETs. pFETs show non-zero intercept reflecting global variations whereas nFETs are impacted by local variations only (zero intercept).

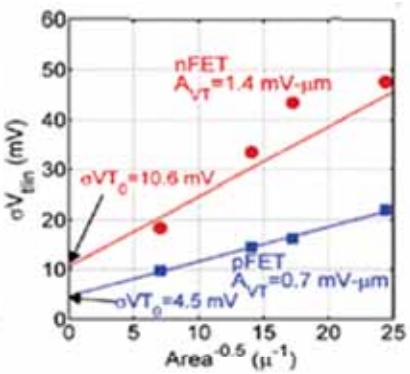


Figure 14: V_{tlin} variation shows Pelgrom nature for n/pFETs. n/pFETs show non-zero intercept reflecting global variations. A_{VT} of 1.4/0.7 mV-µm shows small local variation in n/p FETs,

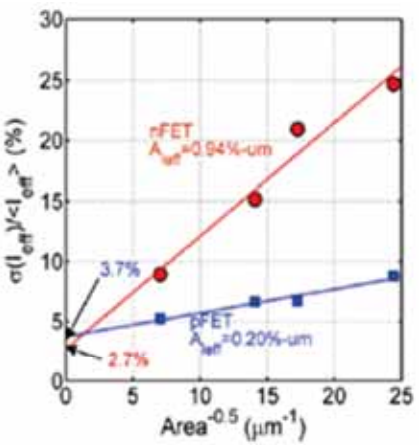


Figure 15: Ieff variation shows Pelgrom nature for n/pFETs. The non-zero intercept shows global variation in FINFETs.

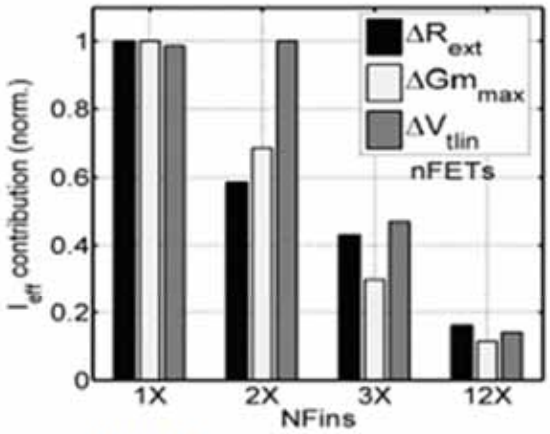


Figure 16: Relative comparison of the impact of individual fluctuation on total I_{eff} variation

After: A. Paul, GlobalFoundries/IBM, IEDM'2013

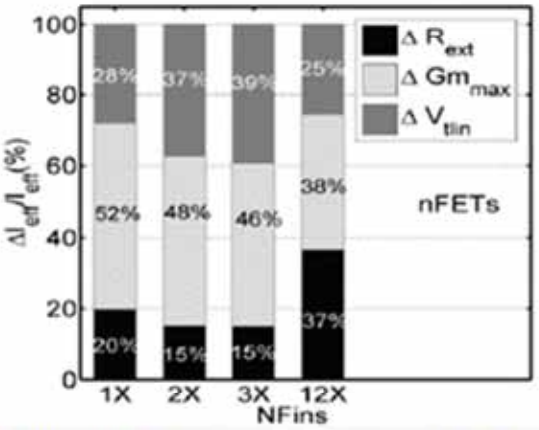


Figure 17: Relative contribution of the three parameters to the overall I_{eff} variability as a function of Nfin for the nFETs. About 30-40% variation is from V_{tlin} which is quite independent of Nfin. R_{ext} (G_{mmax}) contribution decreases (increases) as Nfin reduces from

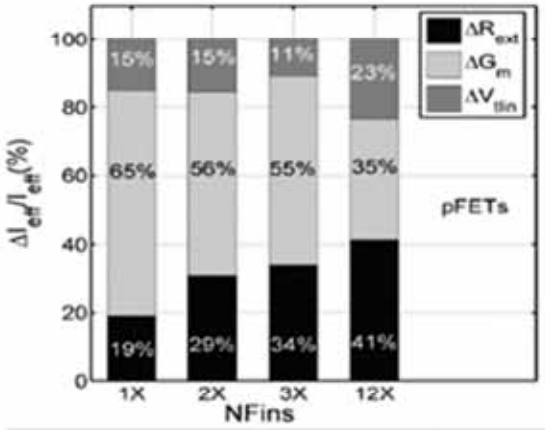
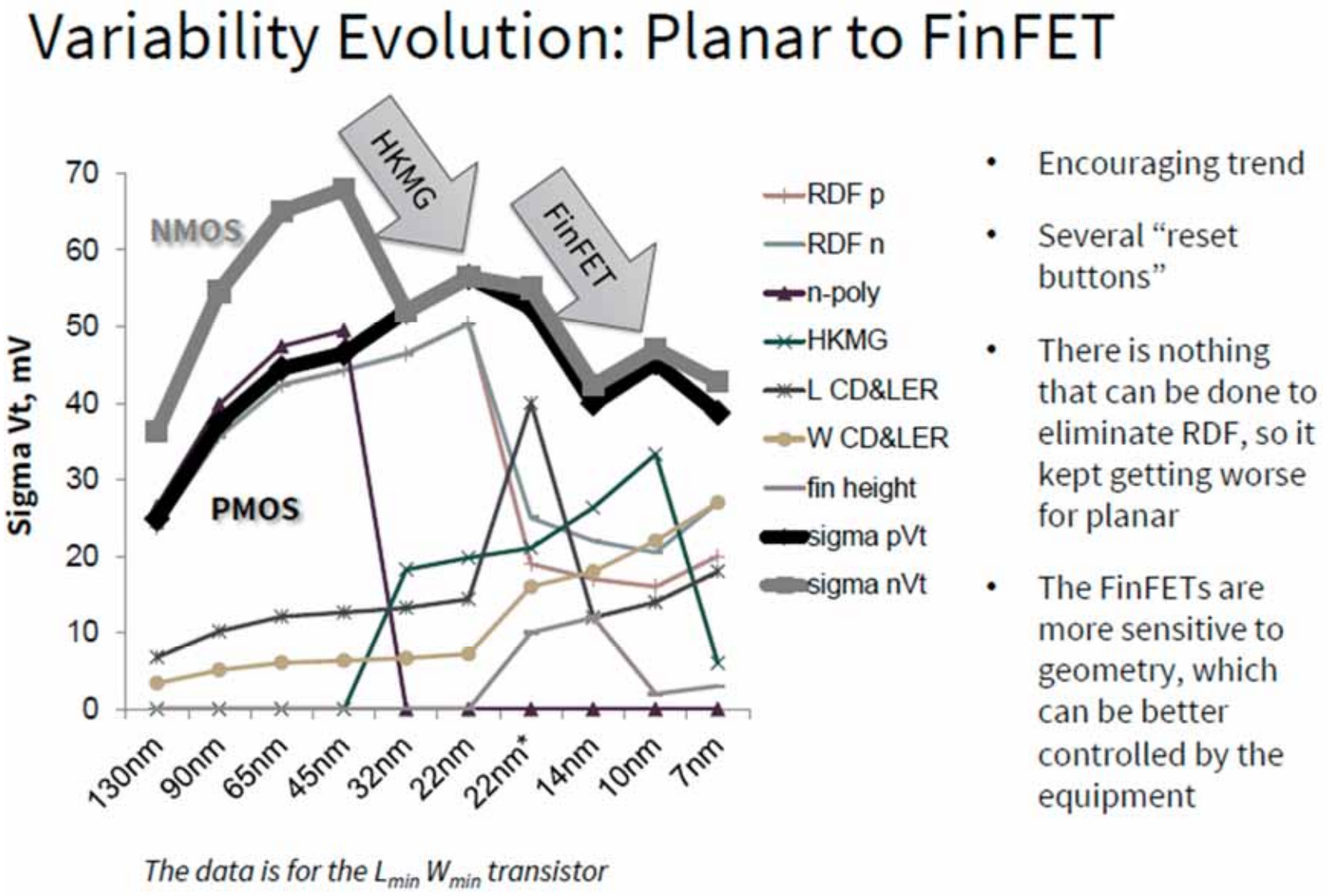


Figure 18: Relative contribution of the three parameters to the overall I_{eff} variability as a function of Nfin for the pFETs. About 15-20% variation is from V_{tlin} which is quite independent of Nfin. R_{ext} ($G_{m,max}$) contribution decreases (increases) as Nfin

PDF SOLUTIONS

Variability - Scaling Trends (Device Architecture)



Modeling random variability: Victor Moroz, invited talk at WMED 2013

After: V. Moroz, Synopsys, IEDM'2014

PDF SOLUTIONS

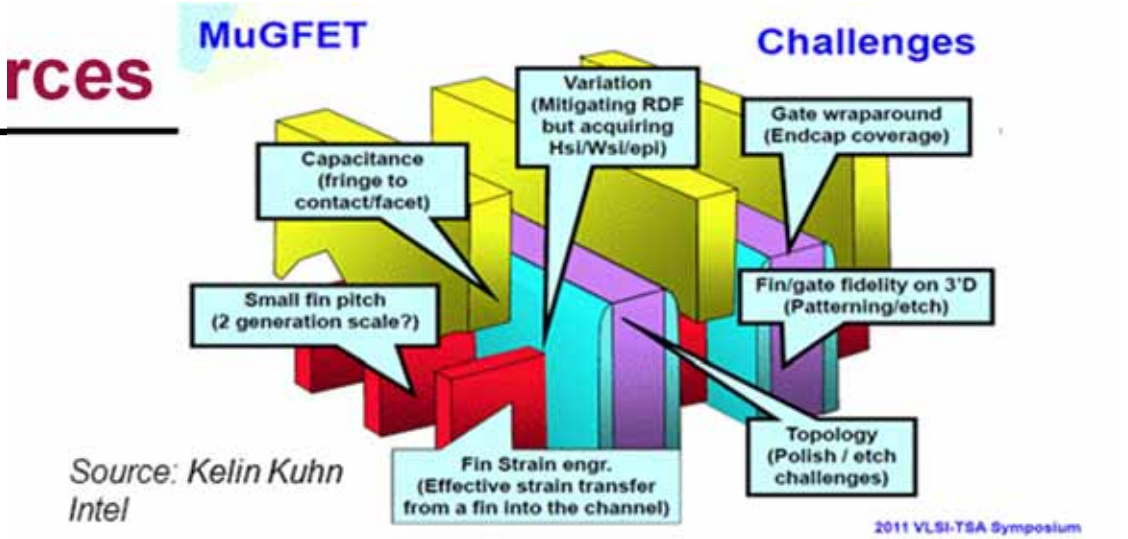
Outline

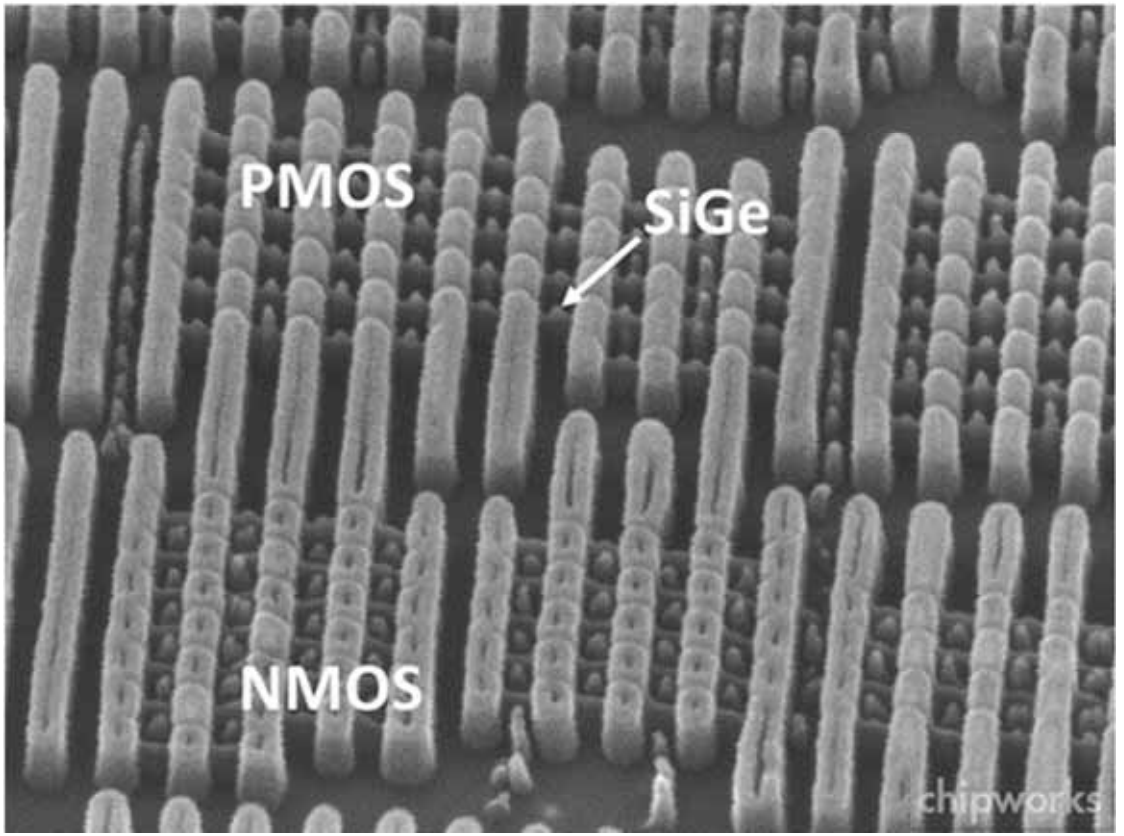
- Why does it matter – Impact on parametric yield, speed, etc
- Device variability – historical perspective and technology trends
- Sources of Variability and Process dependence
- Local Layout Effects and their Characterization
- Process variability and Characterization
- eMetrology for better process control in advanced nodes

FinFET Variability Sources

Device Variability

- **Fins (height and width)**
  - Fin neighborhood
  - Fin density
  - Fin order
  - Fin angle
- **Epi Growth**
  - Number of merged Fins
  - Tuck/Untuck and Tuck PC neighborhood
- **Gate (width and height)**
  - PC density
  - PC cut
- **Trench Contact**
  - Number of Fins in a device
  - Contact density
  - Gate density
- **Extensive Characterization Needs**

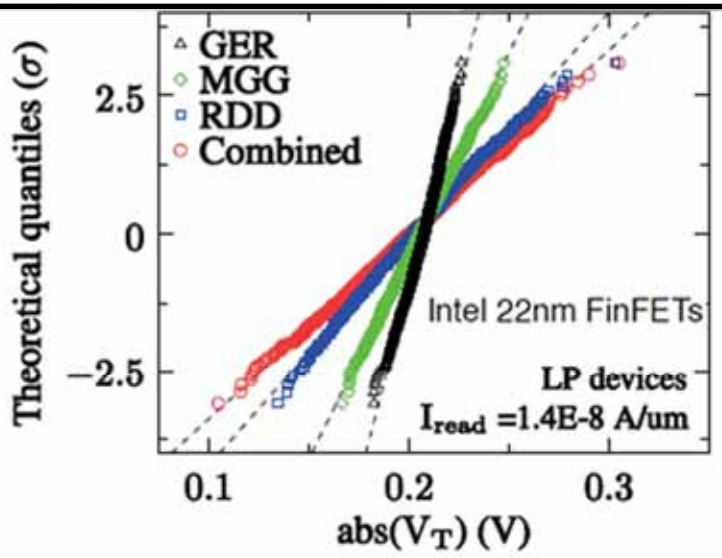




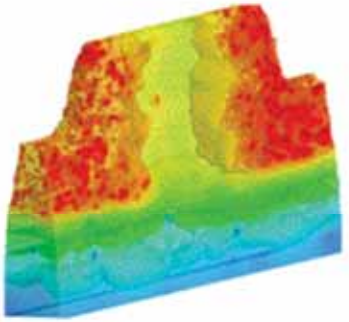
Source: Chipworks – Intel 22nm Trigate

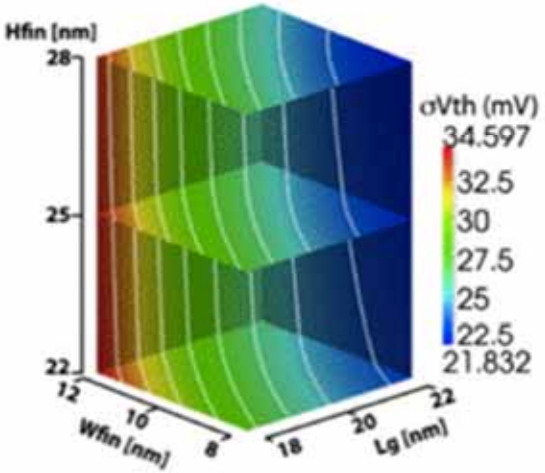
Sources of Variability in FinFET

- **Monte Carlo Simulations of 22nm and 14nm FinFETs to identify main contributors**
  - **Random**
    - Gate Edge Roughness
    - Metal Grains
    - Random Dopants
  - **Systematic**
    - Fin Height
    - Fin Width

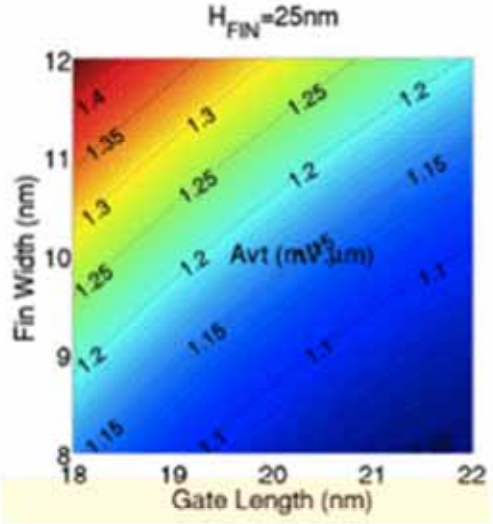


Measured σV_T=32mV
Simulated σV_T=31mV





(a)



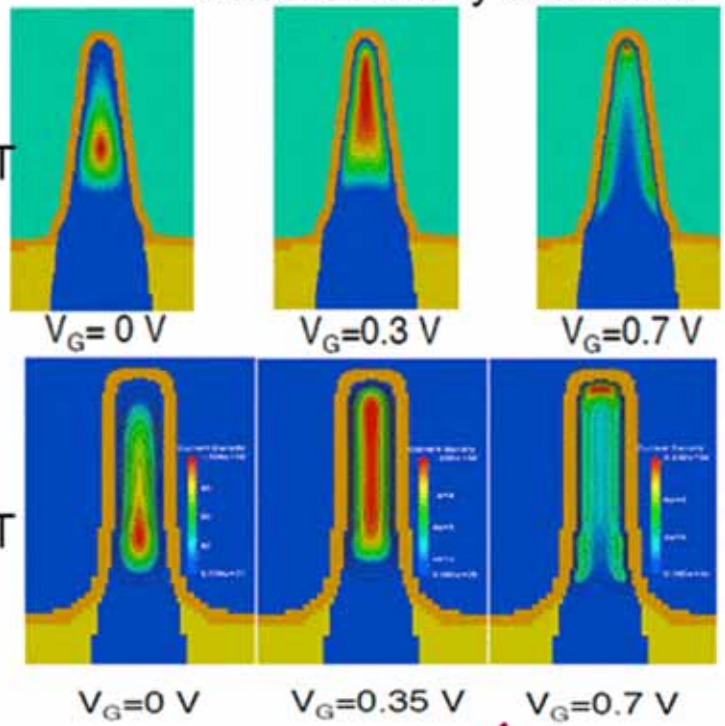
(b)

Vt variation with respect to fin profile and Lg. (a) 3D plot showing sigma Vt at different fin height, fin width and Lg combination. (b) 2D plot showing Avt contour with respect to Fin width and gate length.

IEEE TRANSACTIONS ON
ELECTRON DEVICES
A PUBLICATION OF THE IEEE ELECTRON DEVICES SOCIETY

A. Asenov, GSS, IEEE TED'2015

Current Density Simulation



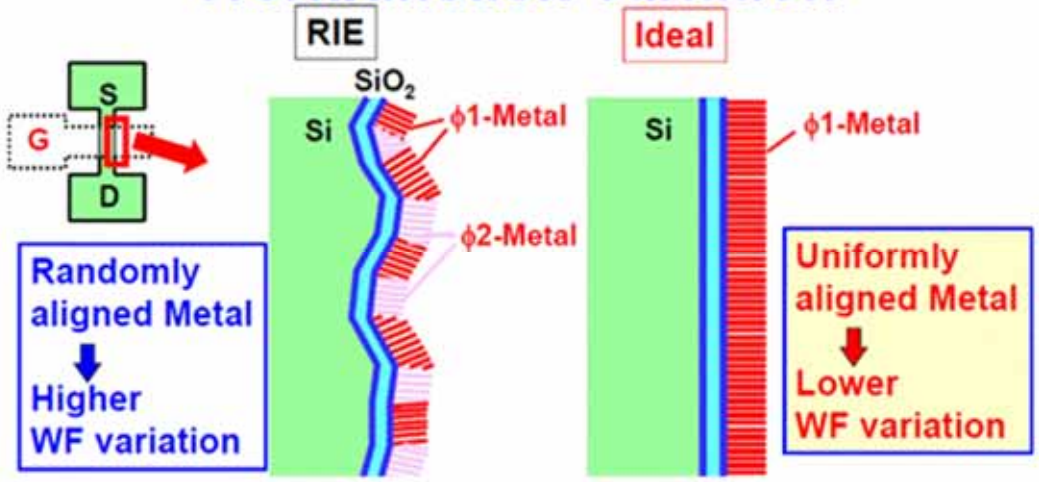
Source: Prof. A. Asenov, GSS,'2015

PDF SOLUTIONS

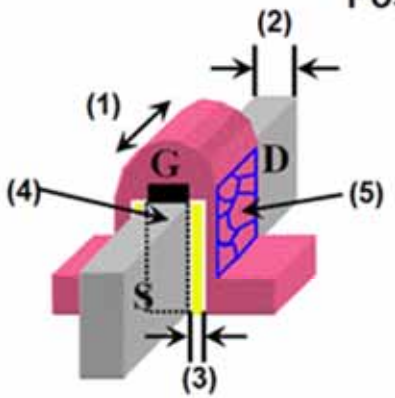
Sources of Variability in FinFET

- Device Variability strongly depends on Process Integration and types of unitary process/tool used to build the transistor
- Identification of sources of variability helps to improve the process and reduce variability

Workfunction Variation



V_{th} Variation for MG FinFETs



Possible V_{th} Variation Sources

(1) Gate Length (L_g)

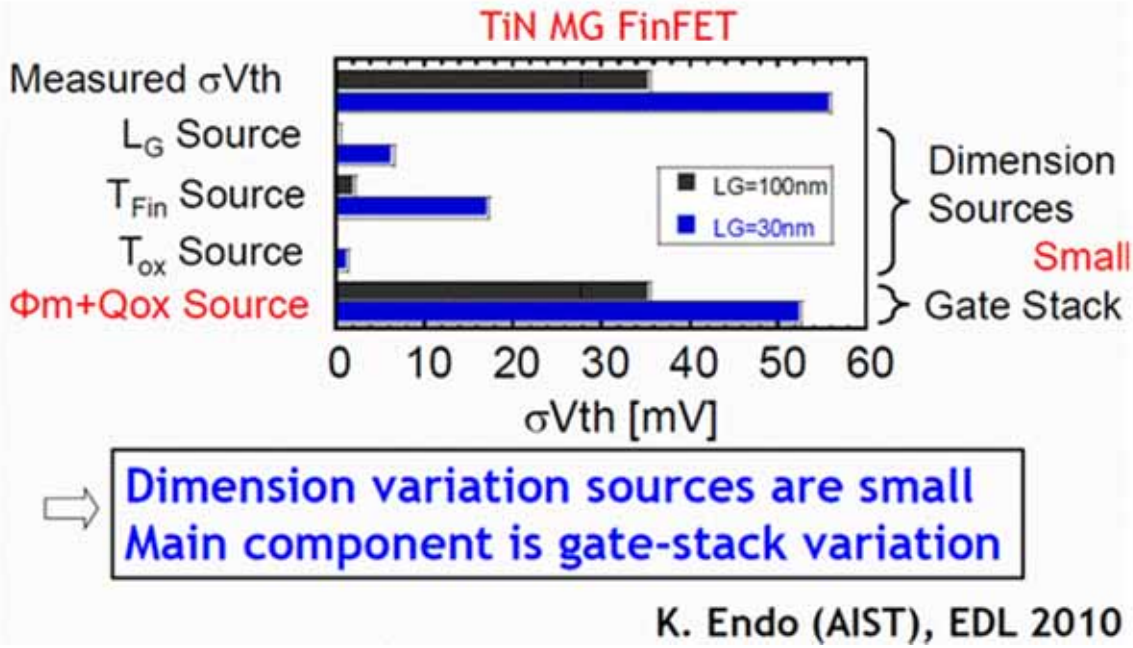
(2) Fin Thickness (T_{si})

(3) Oxide Thickness (T_{ox})

(4) RDF

(5) Work Function WFV (Φ_m)

✓ FinFET variability sources were systematically analyzed

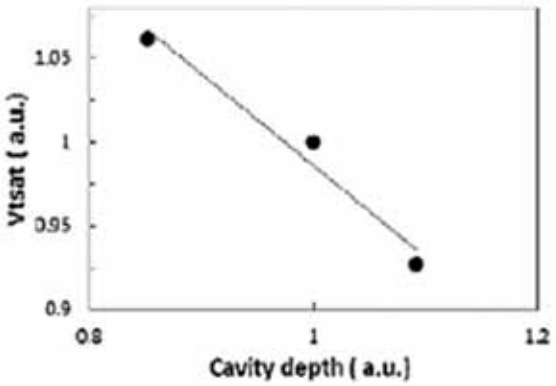


After M. Masahara, AIST, WIMNACT"2012

PDF SOLUTIONS

Process Uniformity Optimization for FinFET

- **Gate stack – WFM and Gate height control – are key features to control Systematic Vt Variability**
  - CMP uniformity across the Die and Wafer (Dummification and Density Control)
- **Pre-Epi Fin Recess variability contributes also to Vt variation**



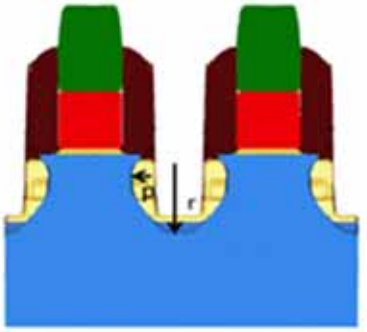
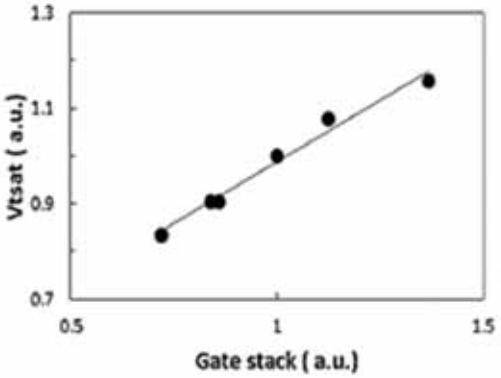
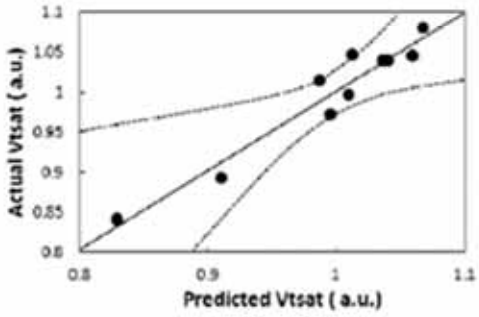


Figure 4: 3D scatterometry measurement techniques are used to measure physical dimensions e.g. proximity (p) and recess depth (r).

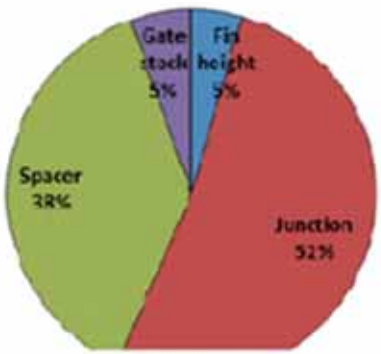




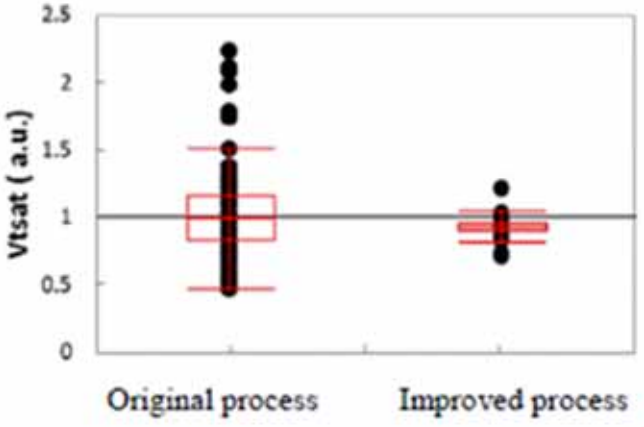
	pValue
Intercept	0.12
Gate CD	0.03
FIN Height	0.20
Recess Depth	0.02
(Gate CD)*(Recess Depth)	0.01
(FIN Height)*(Recess Depth)	0.02

Figure 7: nFET Vt variation as a function of Gate CD, Fin Height, and recess depth. Recess depth is modulated by Gate CD and Fin height.

Original process



Improved process

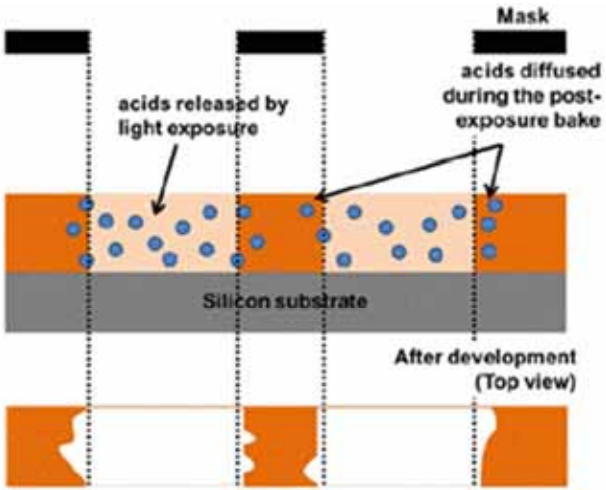


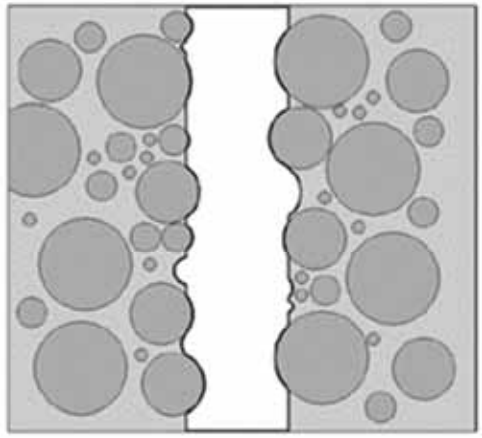
Source: R. Pal, GlobalFoundries, IEDM'2015

PDF SOLUTIONS

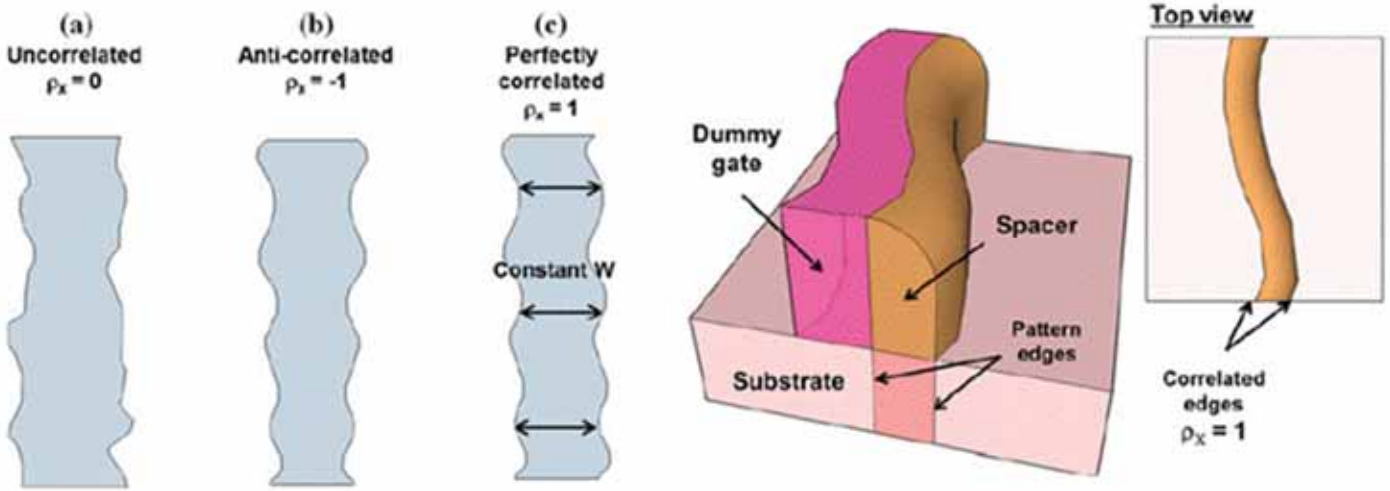
LER and LWR

- Line Edge Roughness and Line Width Roughness increase as the geometrical pattern features decrease, i.e. become more important in scaled nodes
- Litho components - Acids in Chemically amplified resists and Polymer Chain variability contribute to LER

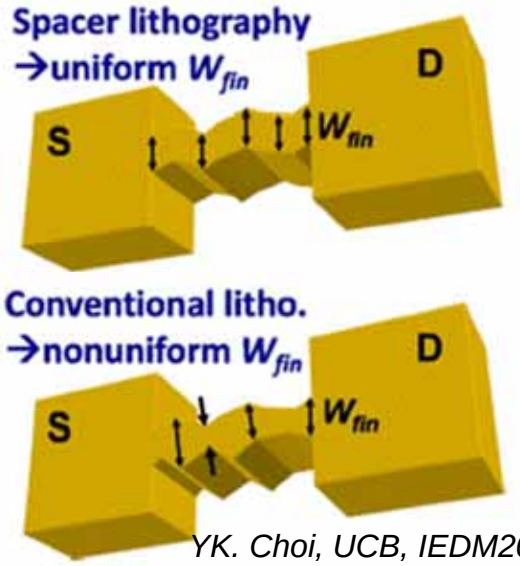




- Spacer-Assisted Dual Patterning (SADP or SIT) can virtually eliminate LWR



After C. Shin, "Variation-Aware Advanced CMOS Devices", Springer 2016



YK. Choi, UCB, IEDM2002

PDF SOLUTIONS

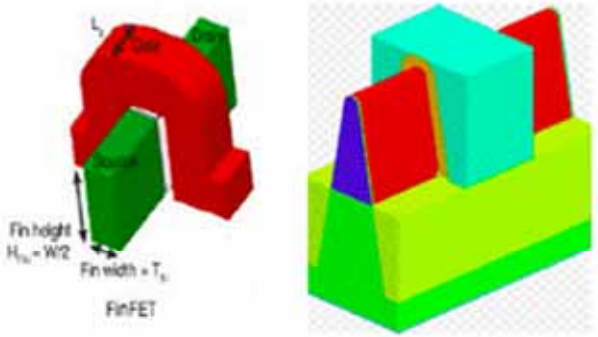
FDSOI – parallel path

Possible Solutions

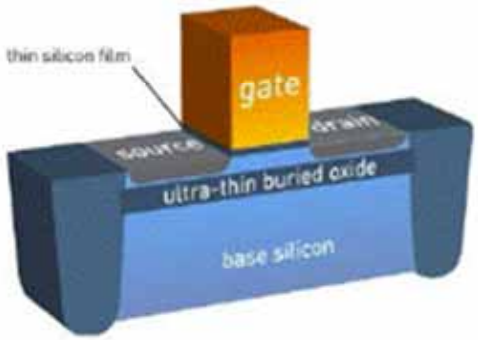
FinFET

FD-SOI

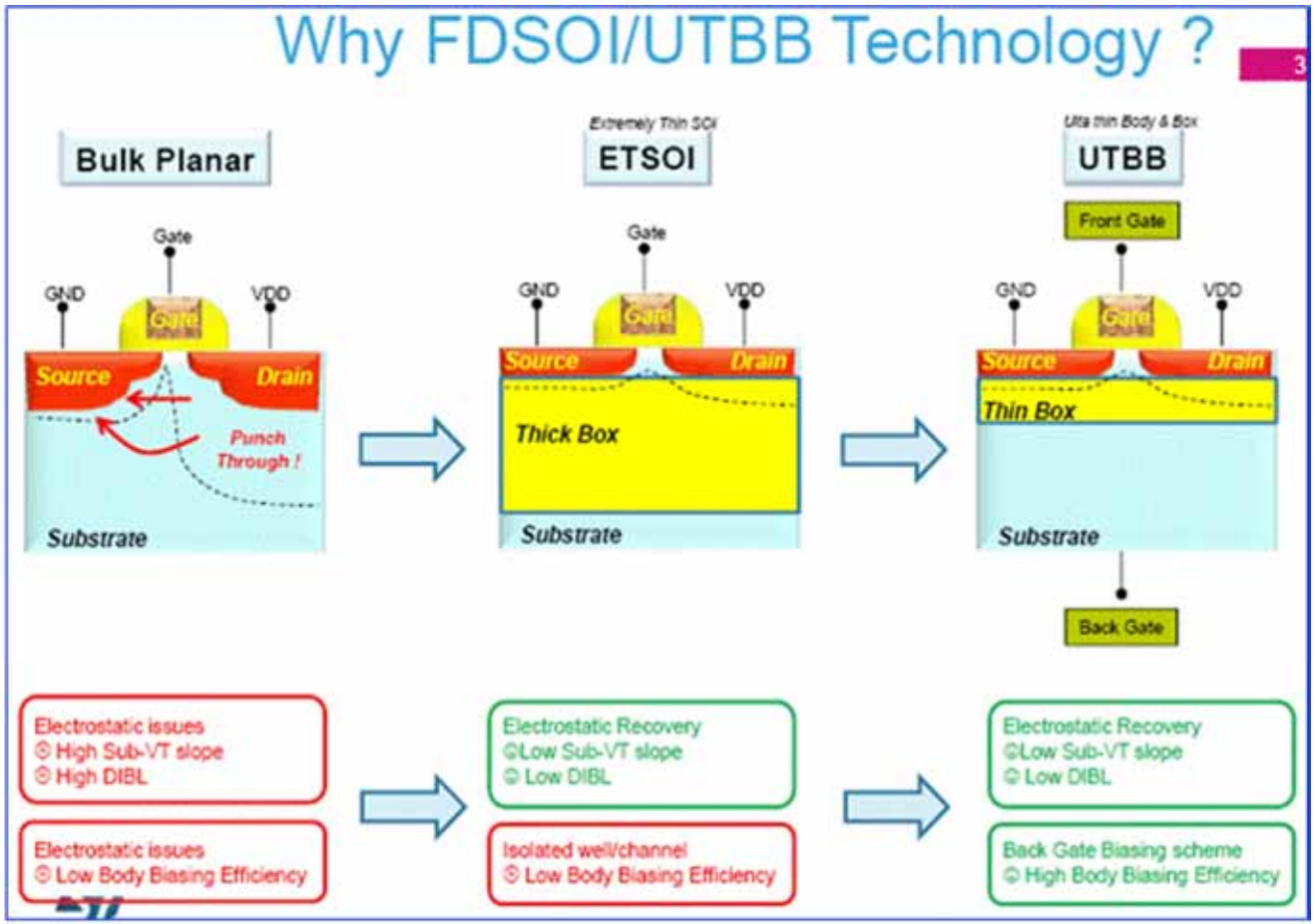
- Alternative to FinFET to provide better electrostatic control
- Simpler integration – less expensive Process
- Less sources of Variability



Fin (shaped) Field Effect Transistor

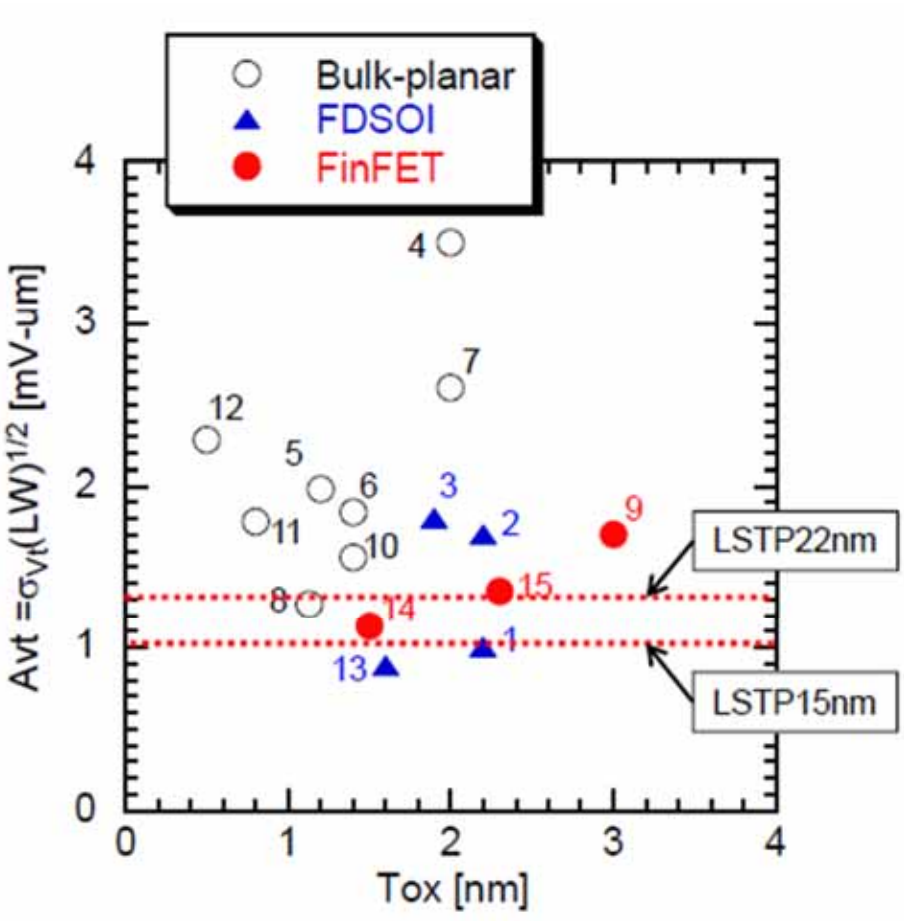


Fully Depleted Silicon on Insulator



PDF SOLUTIONS

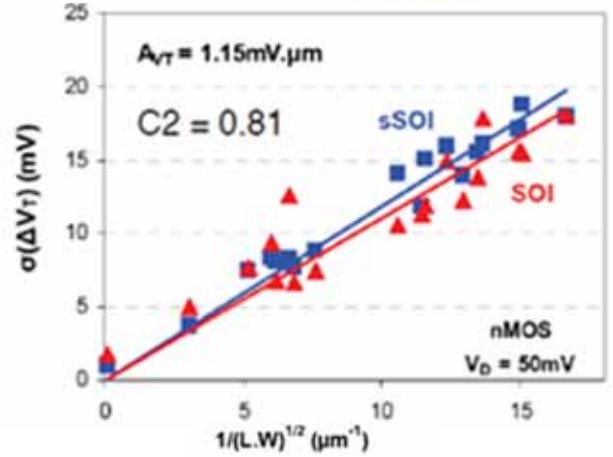
Fully Depleted devices - FinFET and FDSOI



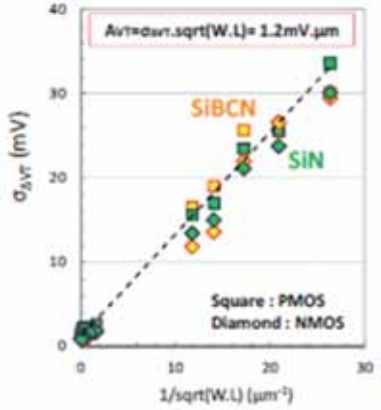
List of reported A_{Vt} values

Ref. #	Device Structure	Gate Stack	Author.	Organi-zation	Reference
1	FDSOI	Poly/SiO2	A.Cathignol	ST	ESSDERC2006
2	FDSOI	TiN/HfO2	C. Fenouillet-Beranger	ST	IEDM2007
3	FDSOI (SOTB)	NiSi/	Y.Morita	Hitachi	VLSI2008
4	Bulk-planar	Poly/SiON	T.Tsunomura	Selete	VLSI2008
5	Bulk-planar	MG/HK	F.Arnaud	ST	IEDM2008
6	Bulk-planar	MG/HK	S.Hasegawa	Toshiba	IEDM2008
7	Bulk-planar	s-Si/SiON	H.Fukutome	Fujitsu	IEDM2009
8	Bulk-planar	HK/MG	M.Goto	Toshiba	VLSI2009
9	FinFET	Mo/SiO2	T.Matsukawa	AIST	VLSI2009
10	Bulk-planar	MG/HK	F.Arnaud	ST	IEDM2009
11	Bulk-planar	MG/HK	L.A.Ragnarsson	IMEC	IEDM2009
12	Bulk-planar	MG/HK	L.A.Ragnarsson	IMEC	IEDM2009
13	FDSOI	MG/HK	K.Cheng	IBM	IEDM2009
14	FinFET	TiN/HfSiO	T.Chiarella	IMEC	ESSDERC2009
15	FinFET	TiN/SiO2	Y.Liu	AIST	VLSI2010

T. Matsukawa, et al., (AIST.) SOI Conf, 2011, 7.1.



O. Faynot, IEDM 2010



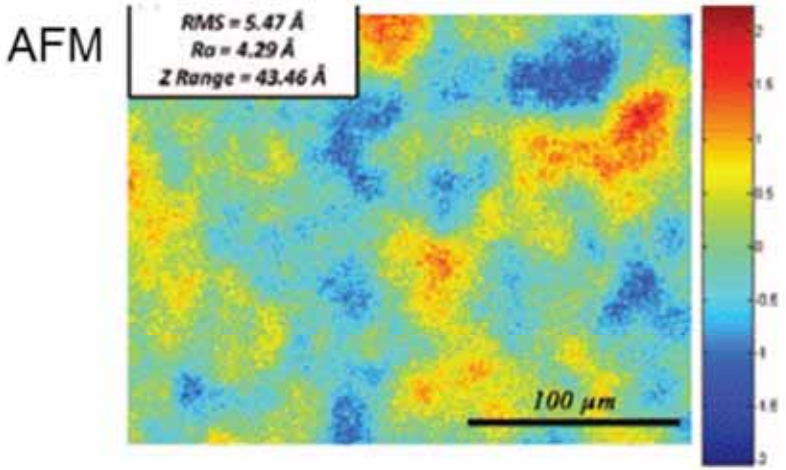
O.Weber, VLSI'2015

FDSOI shows very good potential for Variability reduction due to suppression of RDF and simpler process flow compared to FinFET

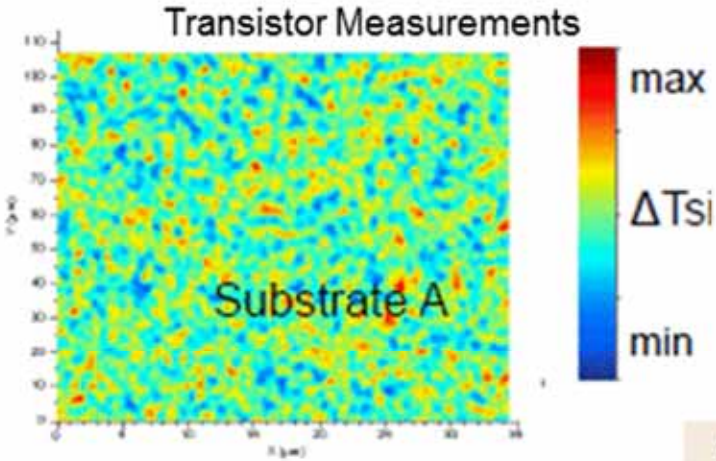
PDF SOLUTIONS

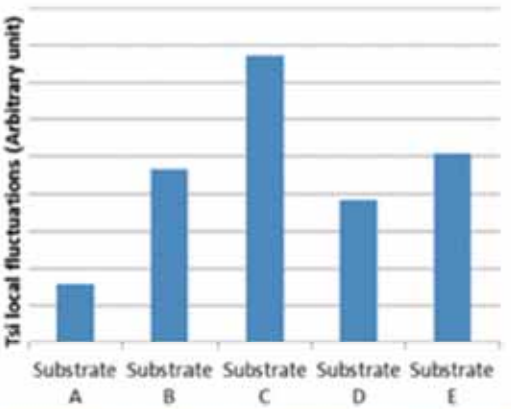
FDSOI – technology with reduced variability

- Ultra Thin Body on Thin BOX – reduced Vt roll-off (Short Channel Effects)
- Reduced RDF – undoped channel
- High-K gate dielectric with Metal Gate
- … but… increased sensitivity to Silicon Thickness variability

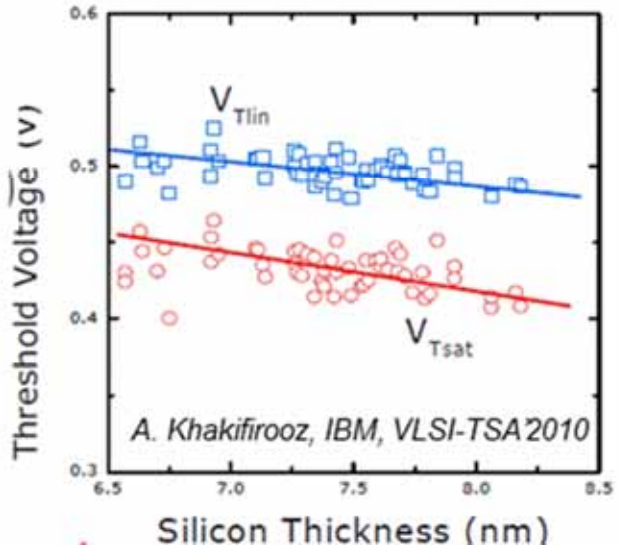


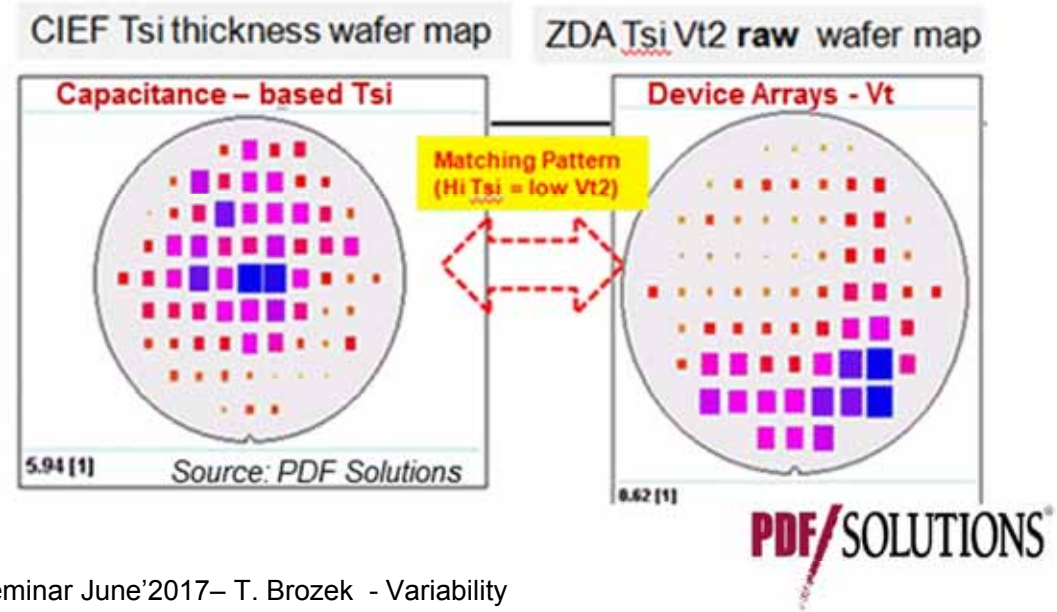
P.E. Acosta-Alba, SOITEC, ECS J. SolSt.SciTech, 2013





Source: A. Cros, STMicro, ICMTS'2014





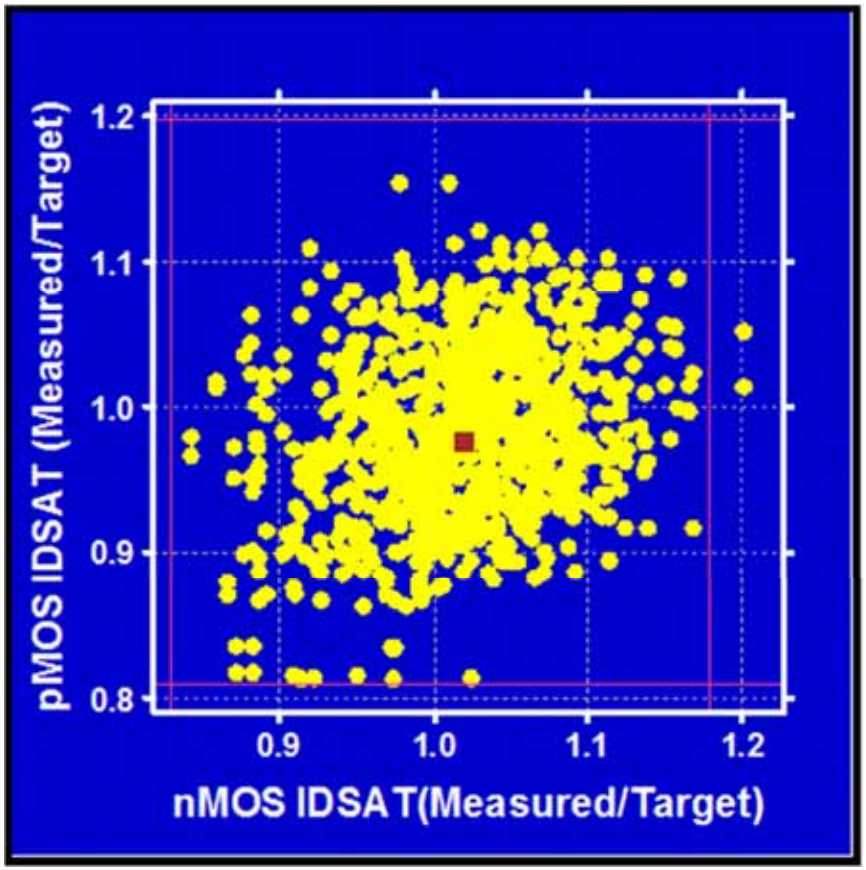
Outline

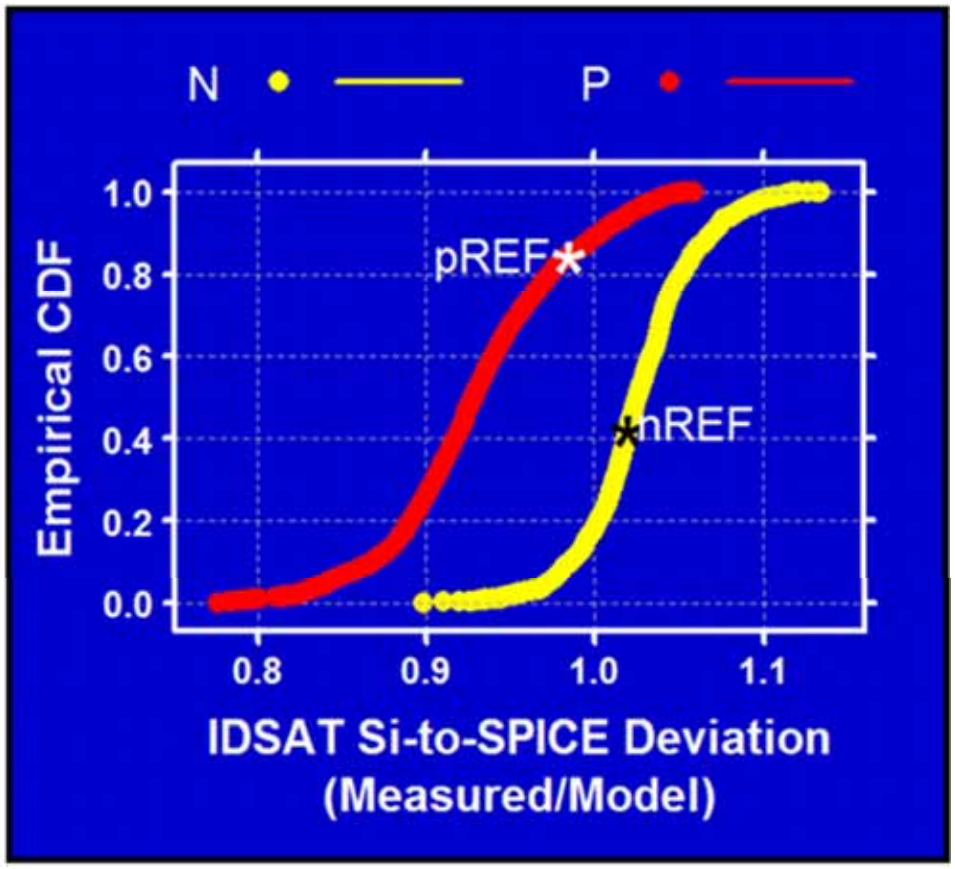
- Why does it matter – Impact on parametric yield, speed, etc
- Device variability – historical perspective and technology trends
- Sources of Variability and Process dependence
- Local Layout Effects and their Characterization
- Process variability and Characterization
- eMetrology for better process control in advanced nodes

Characterization Requirements for Layout Effects

- PCM/WAT structures are close to target (within 2%)
- But the product does not meet performance and/or yield targets
- Example from a 28nm HKMG technology in production

- > 1400 design rule clean layouts
- Simulation of LPE extracted netlists, modeled layout effects included
- Each point is a median of > 450 devices
- Layout induced variability is of the same magnitude as manufacturing variation

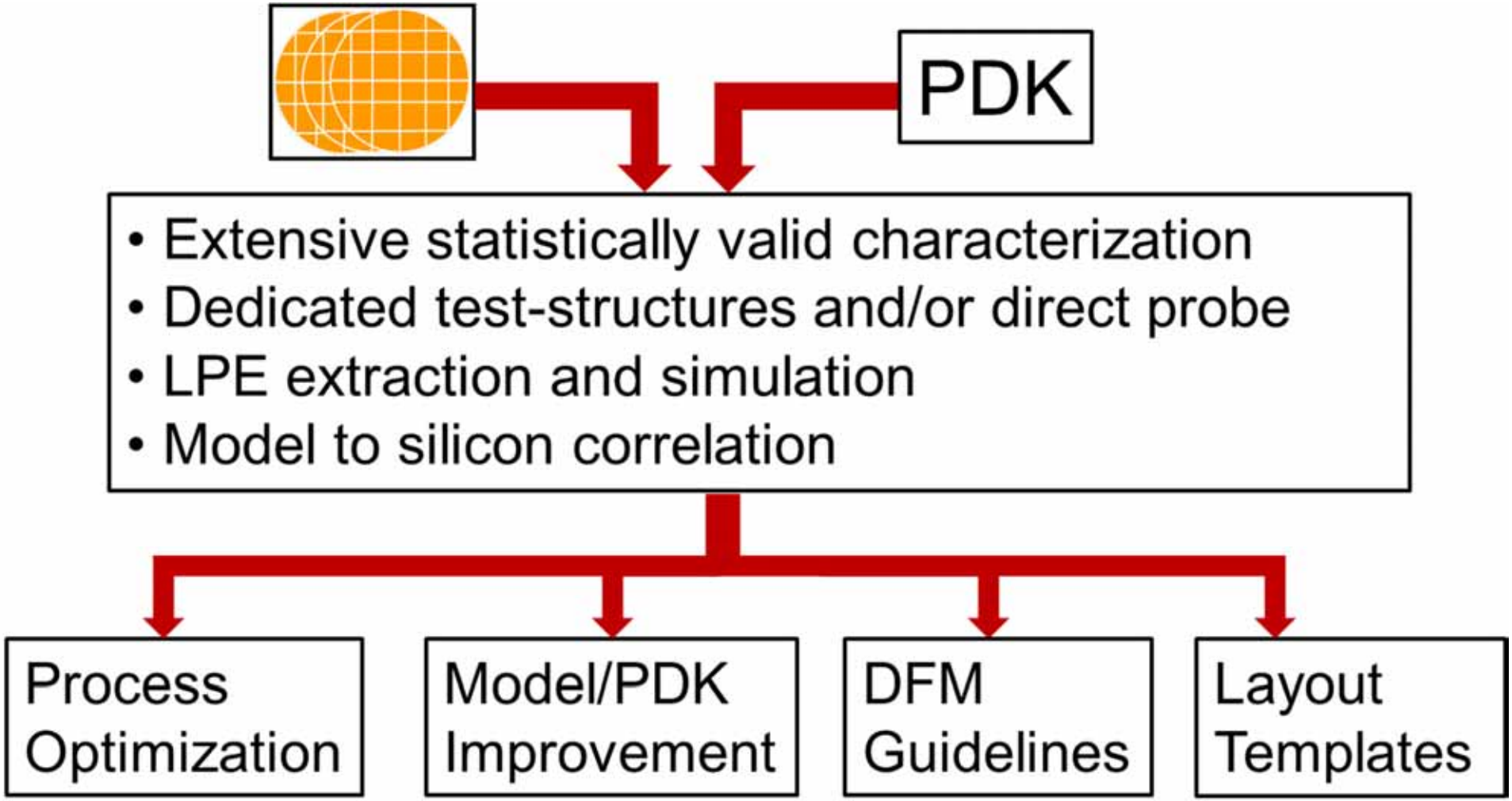




Source: S. Saxena, PDF IEDM 20013

PDF SOLUTIONS

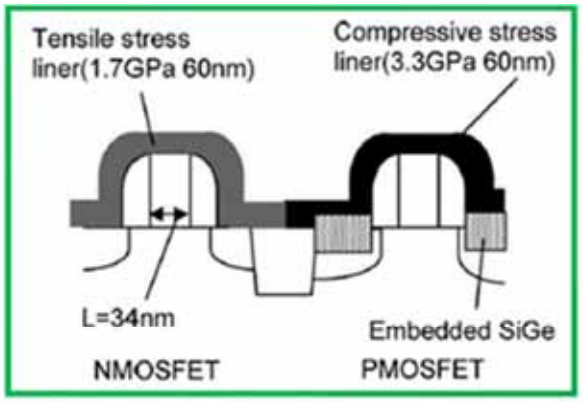
Addressing the Problem



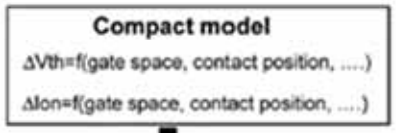
Source: S. Saxena, PDF IEDM 20013

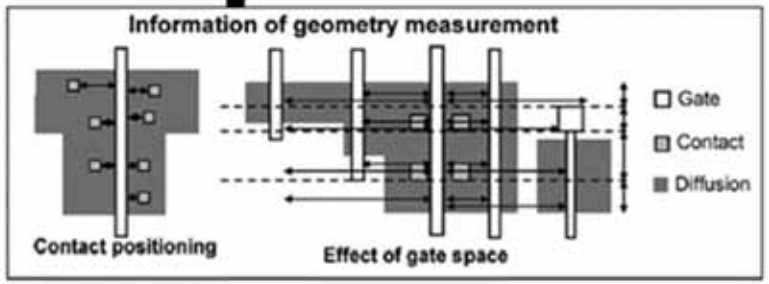
PDF SOLUTIONS

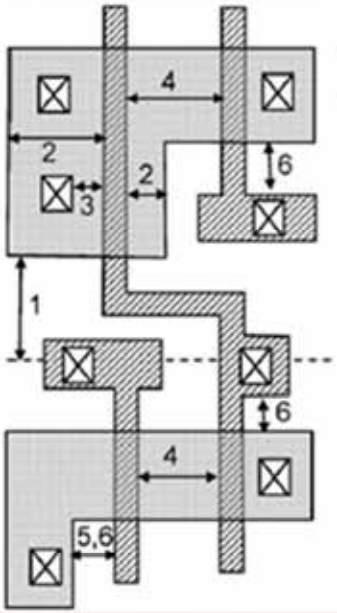
Early Layout Effects - 45nm Strain



- **Successful Compact Models to predict variability due to Strain interaction and relaxation**
- **45nm Bulk CMOS process with stress boosters**
  - Dual Stress Liner + eSiGe for PMOS S/D

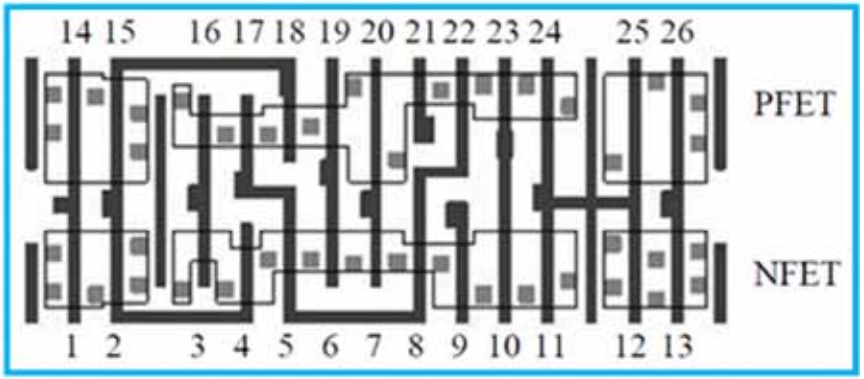


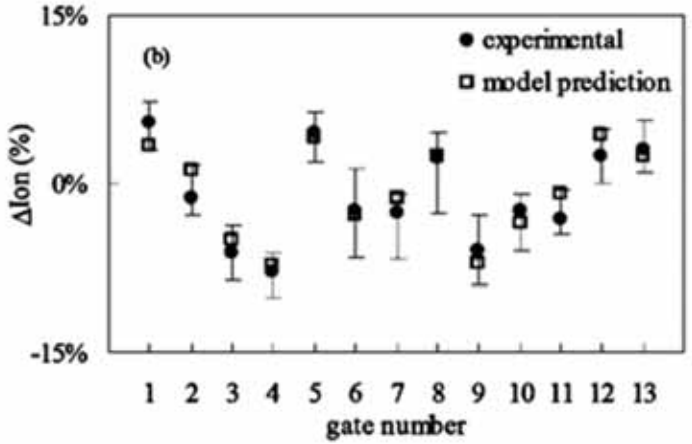


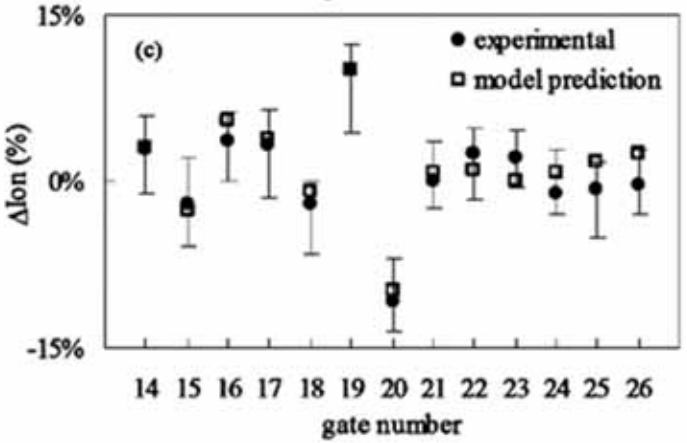


1. Well proximity effect
2. STI stress effect
3. Stress modulation with contact
4. Stress modulation with gate space
5. Bent shaped diffusion (eSiGe effect)
6. Rounding effect (lithography effect)

d-Flip-Flop





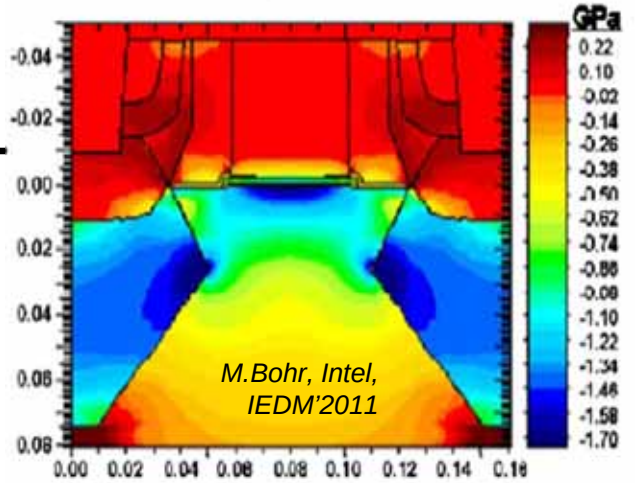


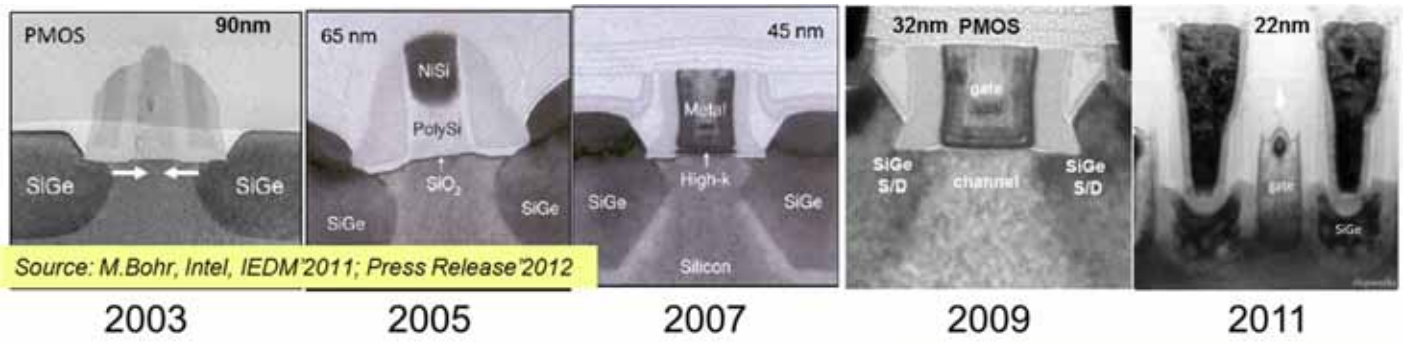
Source: E.Morifuji, Toshiba, IEDM'2011
IEEE TED'2011

PDF SOLUTIONS

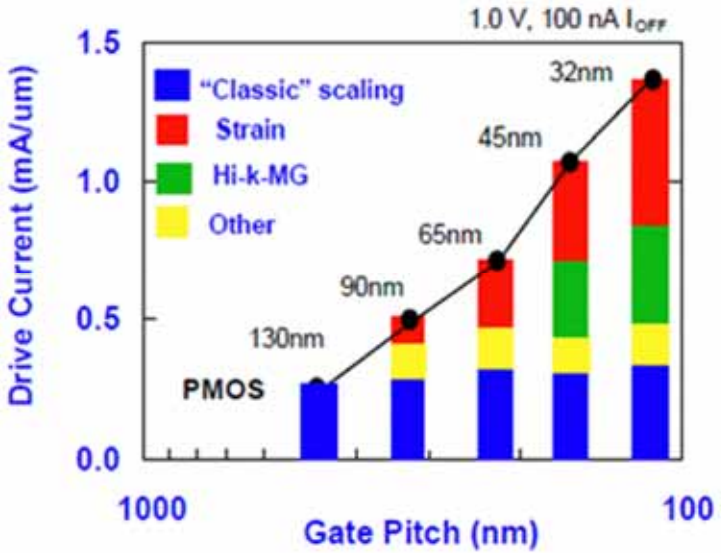
Embedded-SiGe stress in PMOS

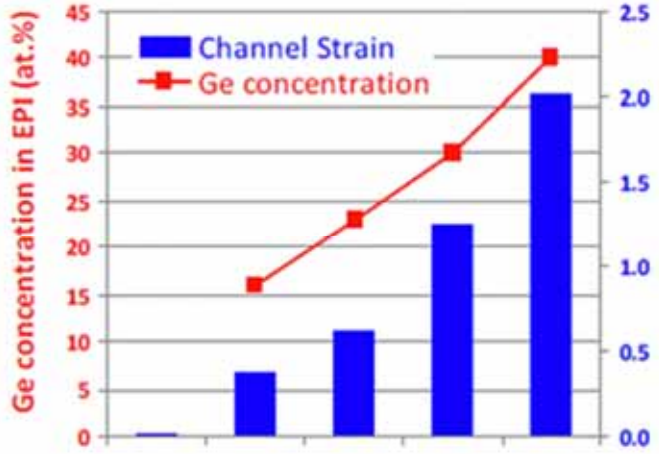
- e- (embedded, epitaxial) SiGe is a key performance booster in scaled PMOS, and at the same time main source of Variability and Layout dependent effects
- Factors impacting Strain and Variability
  - Recess Shape and Depth
  - Recess Proximity Tip-Tip
  - Ge% content and profile
  - Epi overgrowth
  - Density/Loading effects
  - S/D extension length
  - Gate Pitch
  - Device Width
  - L-shape Active
  - S/D termination ("TuckedUnder/Untucked")



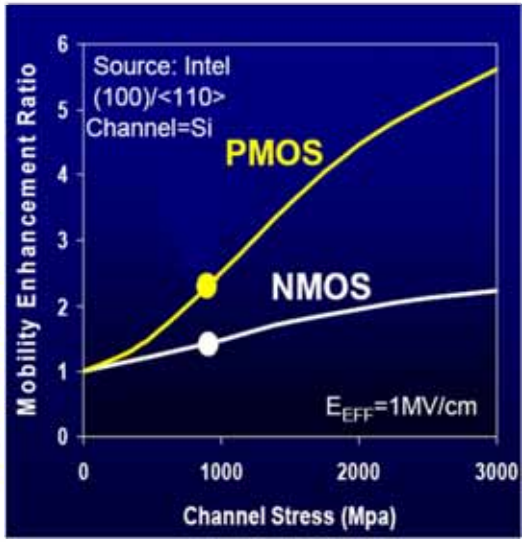


Source: M.Bohr, Intel, IEDM'2011; Press Release'2012





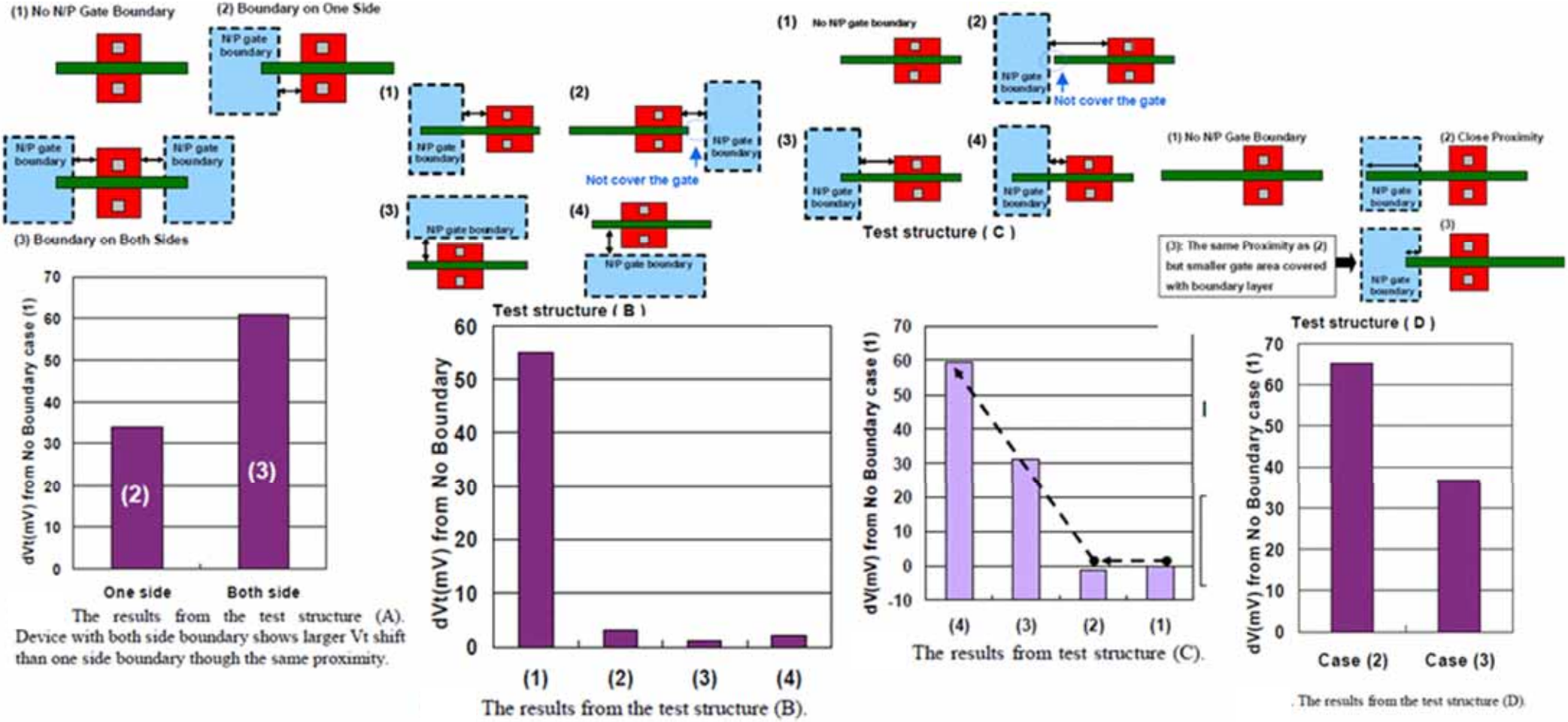
Source: K. Kuhn, Intel, JECS, 2010



PDF SOLUTIONS

HK-MG Layout effects - impact on Device Vt

- **Additional sensitivities identified for Metal Gate proximity (in Gate First process)**
  - **Structure A – Both side boundary of opposite type Metal Gate has stronger impact**
  - **Structure B – "sharing" opposite type of WF Metal in one Gate causes the shift (not just proximity)**
  - **Structure C – distance from the device to the boundary of the opposite type of WF Metal matters**
  - **Structure D – larger amount of the opposite WF Metal type in the Gate causes larger effect**

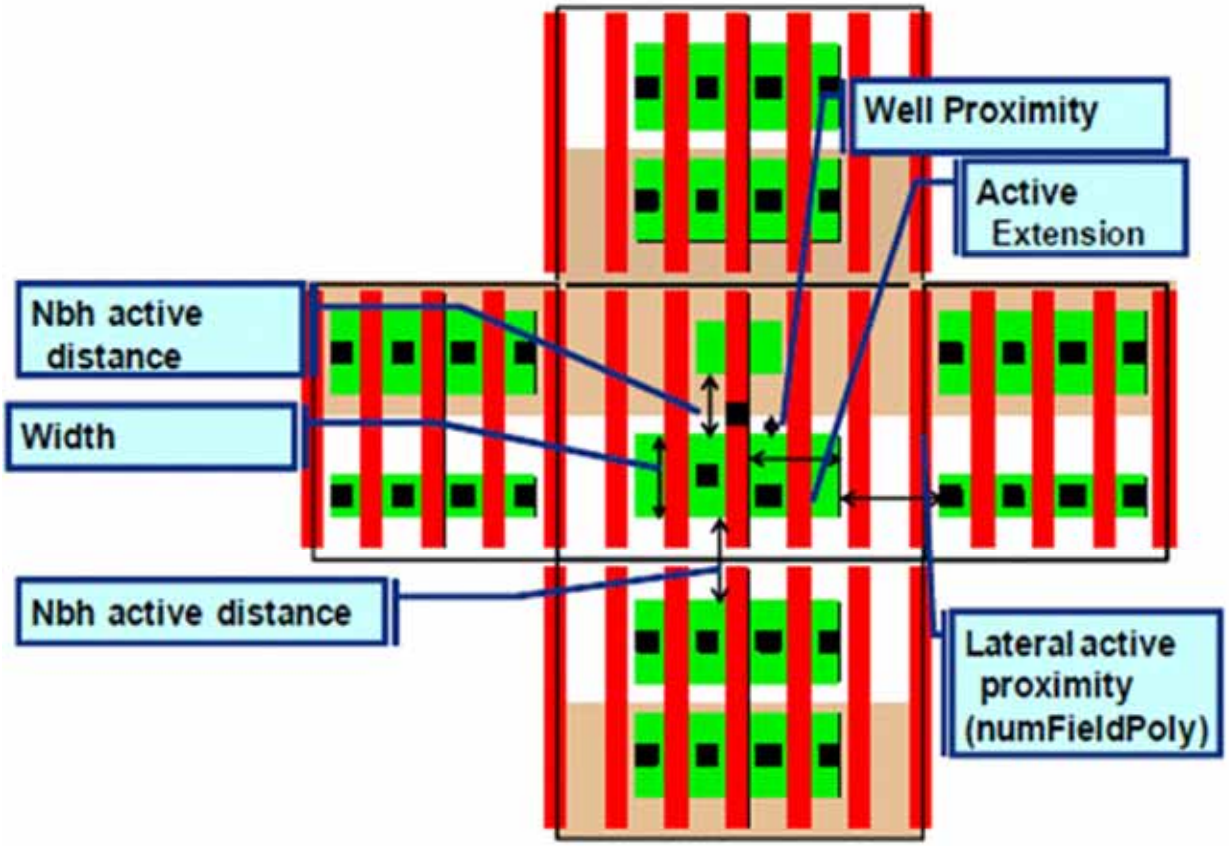


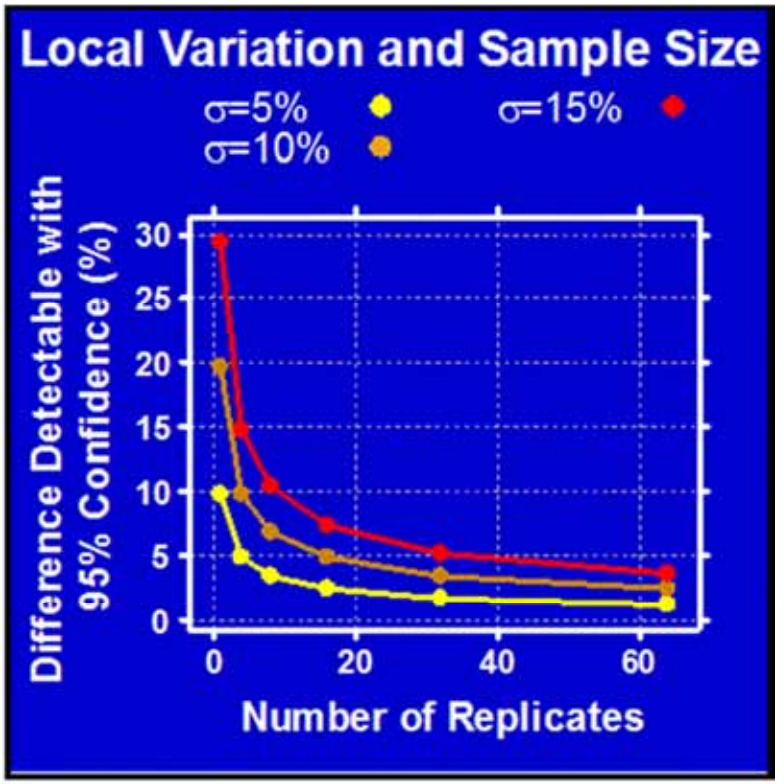
Source: M. Hamaguchi, Toshiba/IBM/ISDA, IEDM'2011

PDF SOLUTIONS

Problem Complexity: Many interacting layout effects

- **Attributes from cell layout and cell-abutment**
- **Large experiment (DOE)**
  - Gate Length/Gate Pitch
  - Device Width
  - Active Extension (SA/SB)
  - Diffusion Break (Single/Double, Continuous)
  - L-shape Jogs
  - Neighborhood/Proximity



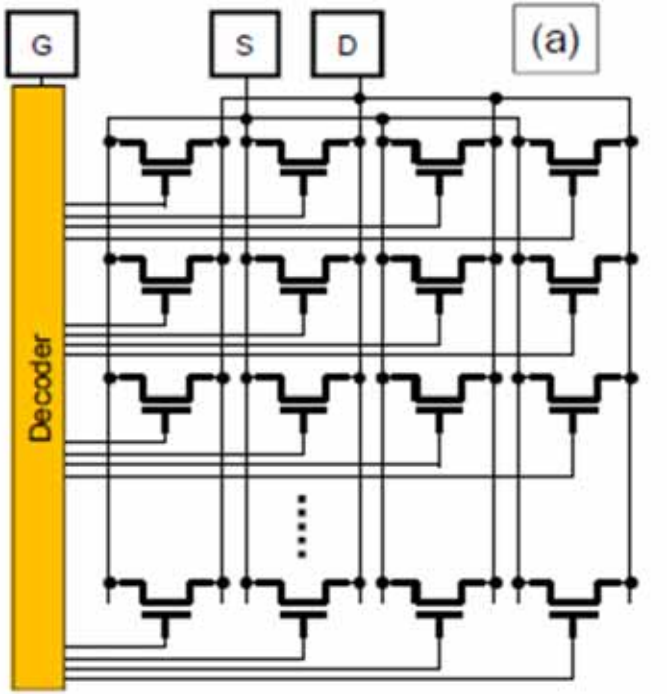


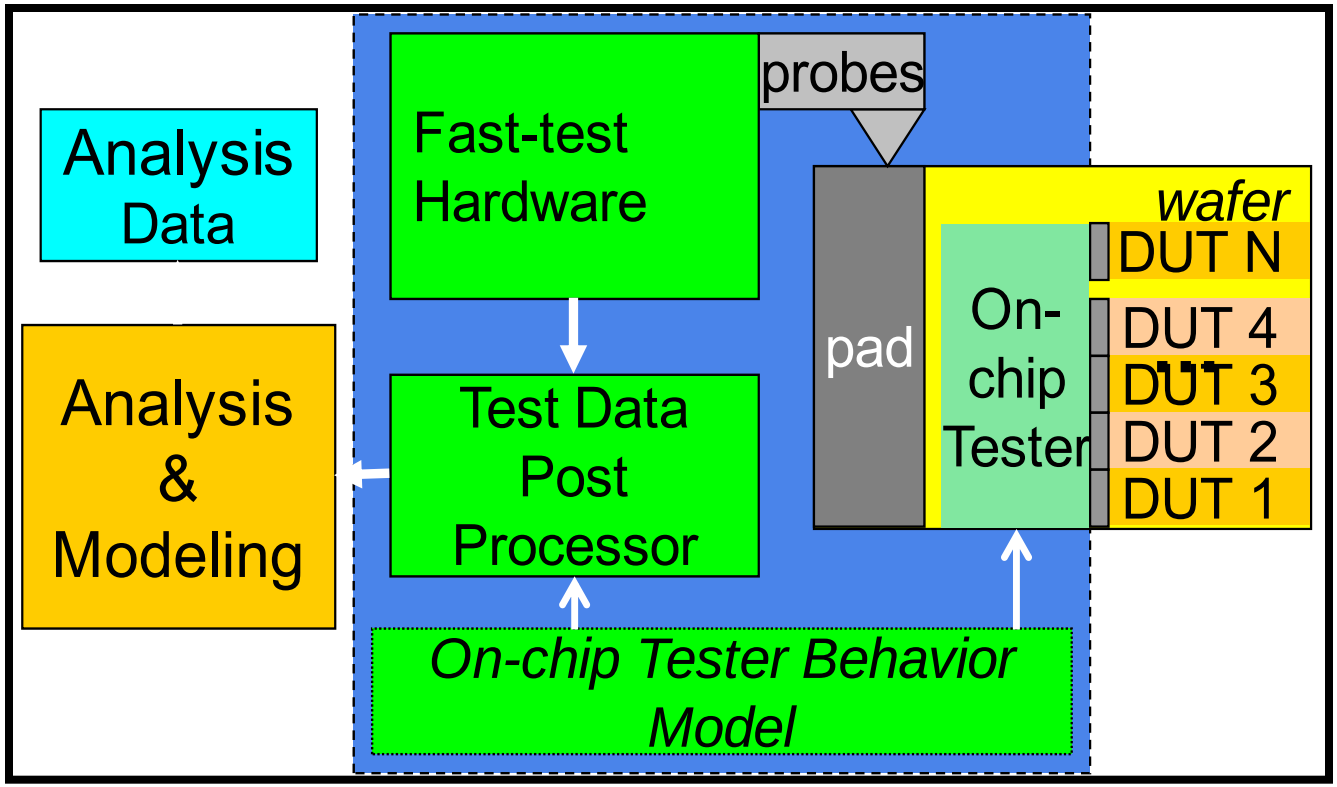
- Local variation (σ) adds noise to the measurement of layout effects
- Replicates: averaging & local variation estimation
- Large DOE & replicates → intractable with traditional characterization

Source: S. Saxena, PDF IEDM 20013

PDF SOLUTIONS

High Volume Characterization





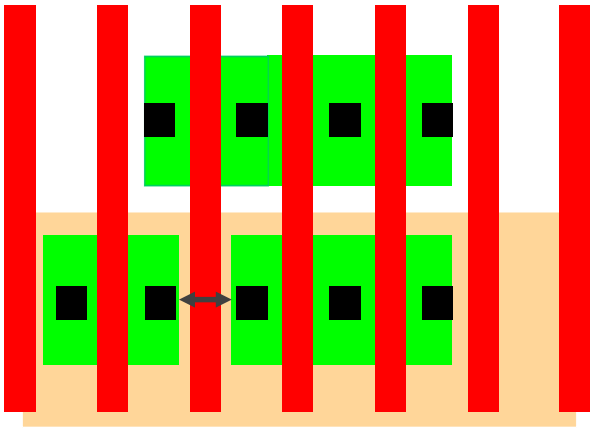
Source: S. Saxena, PDF IEDM 20013

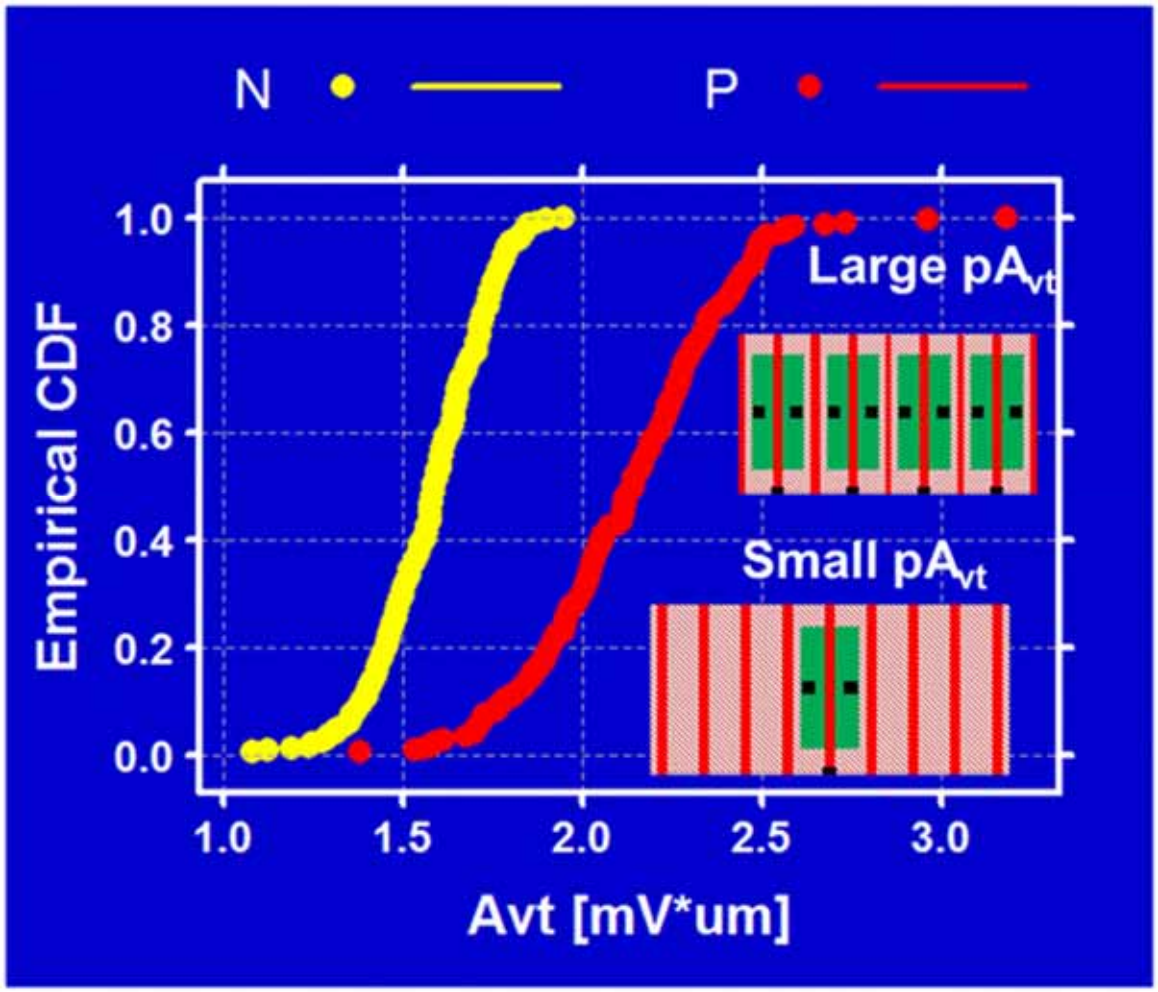
- **Tractable with a dedicated test infrastructure**
  - Array test structures with on-chip test circuits
  - Fast parallel test (e.g. up to 256 parallel channels)
- **Example: >1400 unique layouts, >= 8 replicates**
  - 100 X speed up over traditional approach

PDF SOLUTIONS

Local Variation

- Local variation estimated for each layout
- $A_{VT}(p) > A_{VT}(n)$
- Lateral active proximity impacts local variation





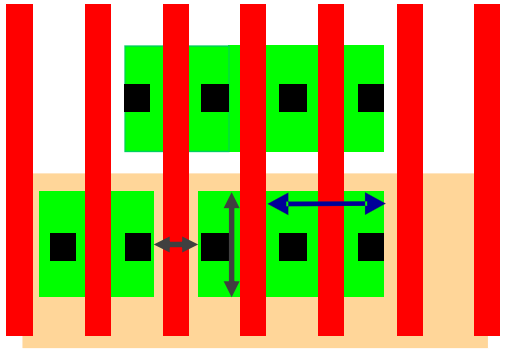
Source: S. Saxena, PDF IEDM 20013

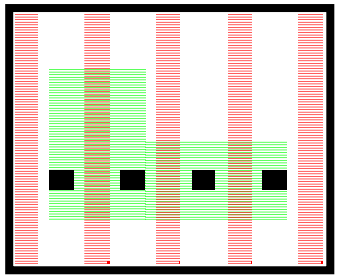
$$A_{VT} = \sigma_{local} \times \sqrt{2} \times \sqrt{WL}$$

PDF SOLUTIONS

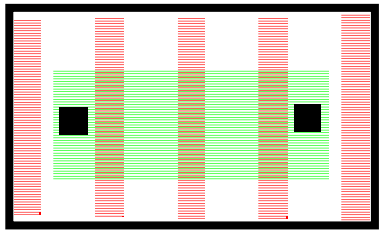
Interactions and Main Layout Effects

- **Interaction of three pMOS active (RX, OD) related layout attributes**
  - Active extension
  - Lateral proximity
  - Active width

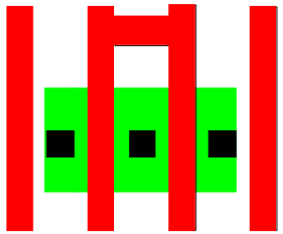




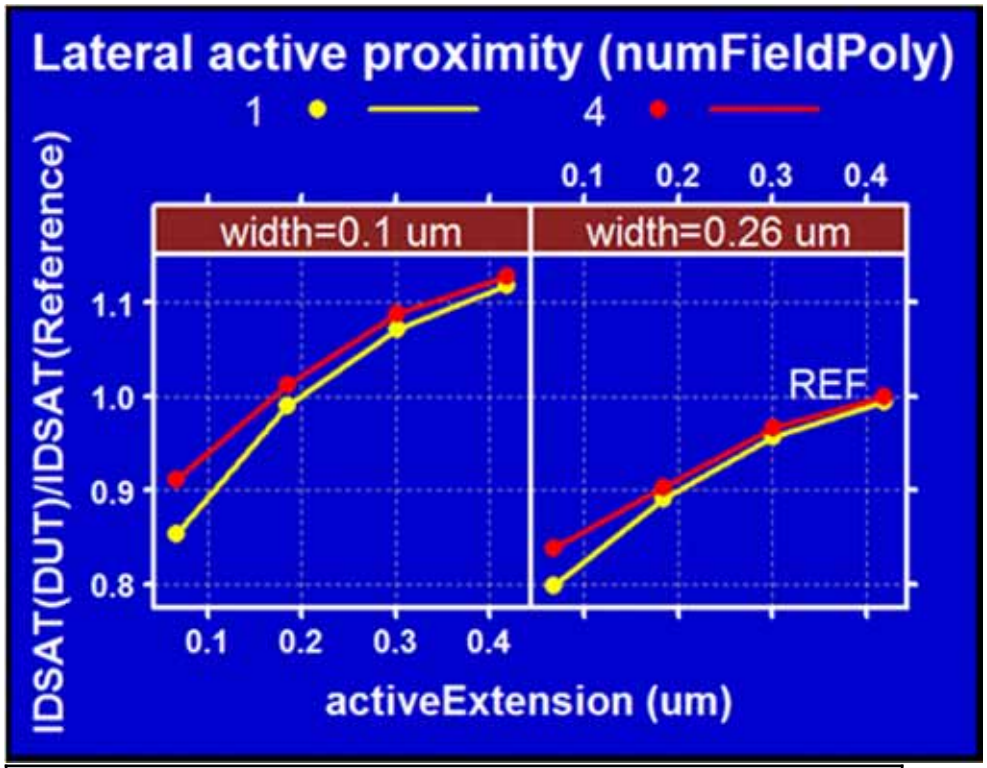
Notched



Series



Wrong way poly



Common Layout Attributes Causing > 10% Model-Silicon Gap (28nm)
Narrow width transistors
Notched Actives (L-shaped, T-shaped)
Series (stacked) gates
Active Extension (SA, LOD)
Well Proximity & Neighborhood active
Lateral active proximity & width
Poly spacing
"Wrong" way poly (when allowed)

Source: S. Saxena, PDF IEDM 20013

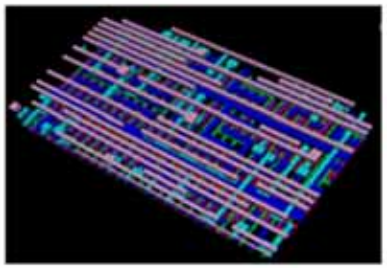
PDF SOLUTIONS

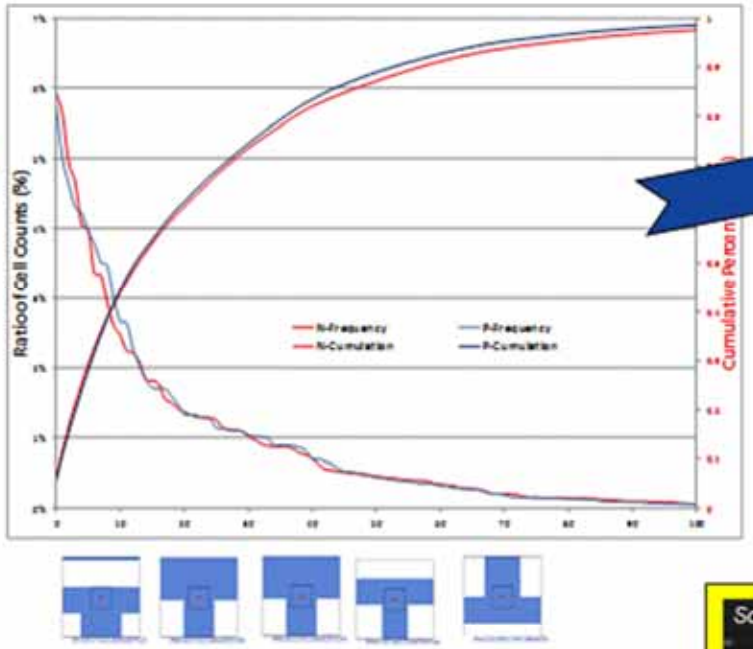
Outline

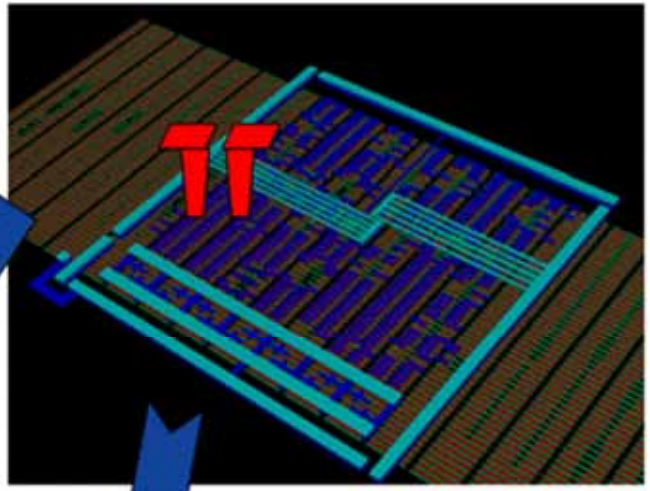
- Why does it matter – Impact on parametric yield, speed, etc
- Device variability – historical perspective and technology trends
- Sources of Variability and Process dependence
- Local Layout Effects and their Characterization
- Process variability and Characterization
- eMetrology for better process control in advanced nodes

Direct Probe CV® Approach : *Concept*

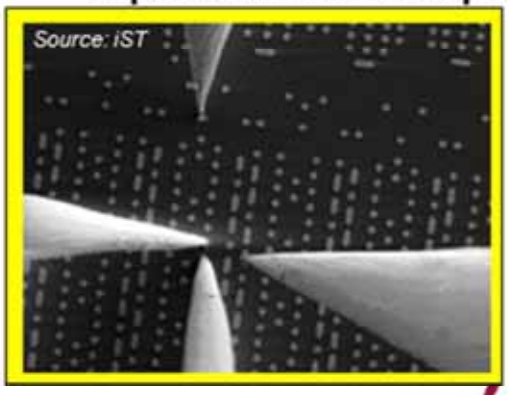
- Analyze product layout to classify layout patterns and build Pareto to drive test chip DOE/DUT selection
- Build Contact & M1 mask to direct tap-out transistor / resistor on product wafers







Equivalent to Micro-probing



Example of 20nm high performance CPU :
Top-100s transistor w/i billions of transistor represent 95% of total transistor count

Probe thousands of transistors per die using fast test speed on PDF pdFasTest tester

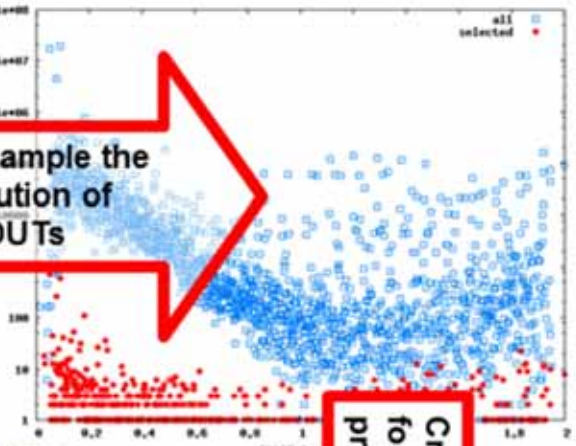
After A Strojwas, Tutorial "Variability and DFM", Short Course, VLSI Tech Symp'2014

PDF SOLUTIONS®

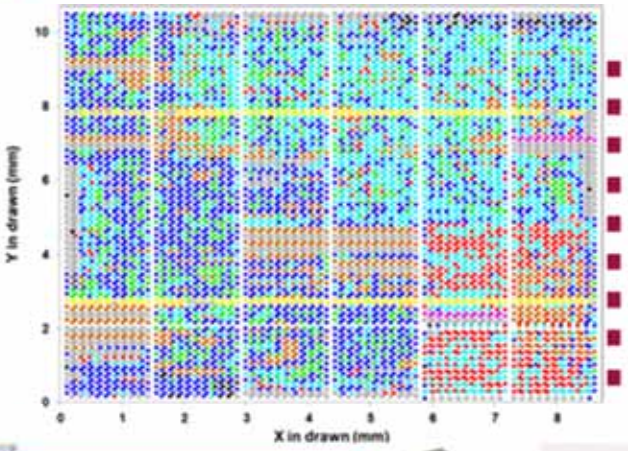
To Create a "Direct Probe Characterization Vehicle"

Analyze complete product GDS
Classify all unique patterns & transistor environments

Statistically sample the actual distribution of patterns for DUTs



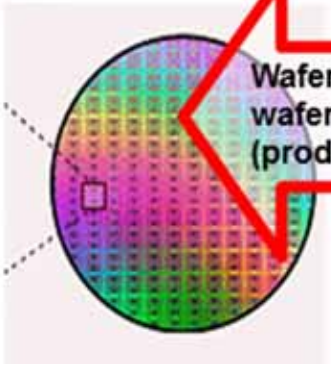
Create 2 test masks for use on some product wafers



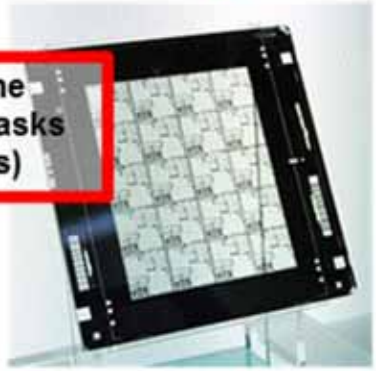
Brown: SRAM transistor
Black: I/O transistor
Yellow: Open/Short test
Green: High Vt transistor
Blue: Reg Vt transistor
Lt Blue: Low Vt trans
Red: Super-low Vt
Magenta: Passives
Black: M1-resistor

> 5,000,000 transistors per wafer I-V comparison to model in 2 days

pdFasTester F-series with massively parallel parametric testing



Wafer fab & test some wafers with 2 test masks (product base wafers)

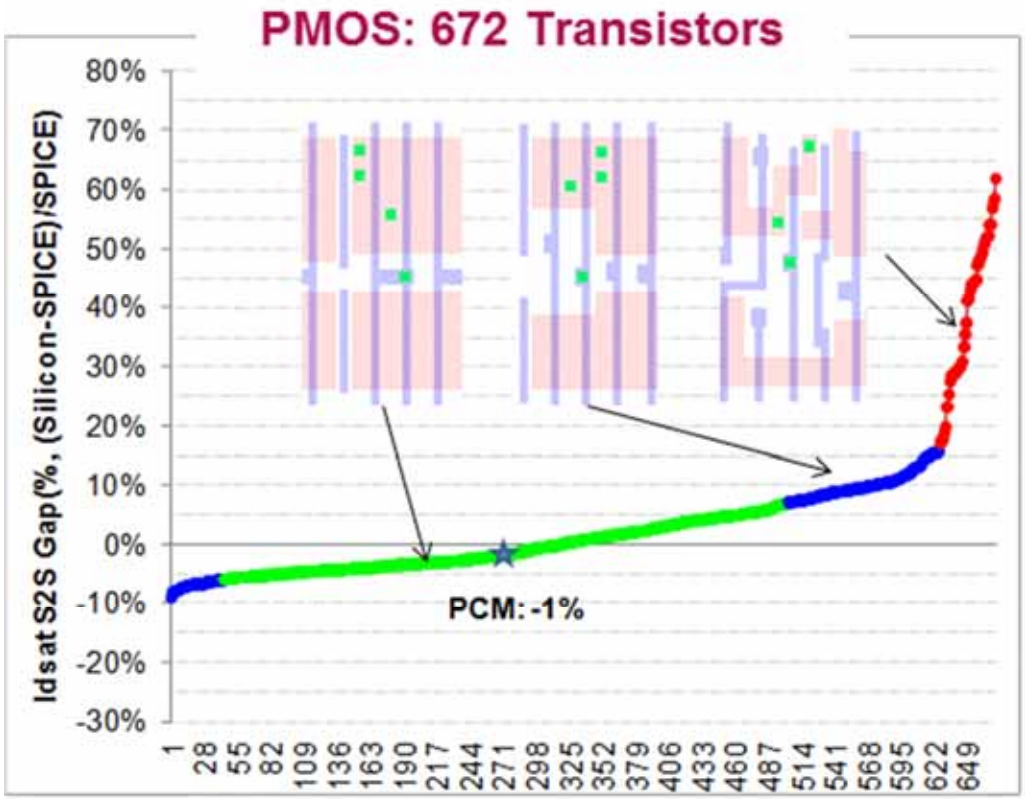


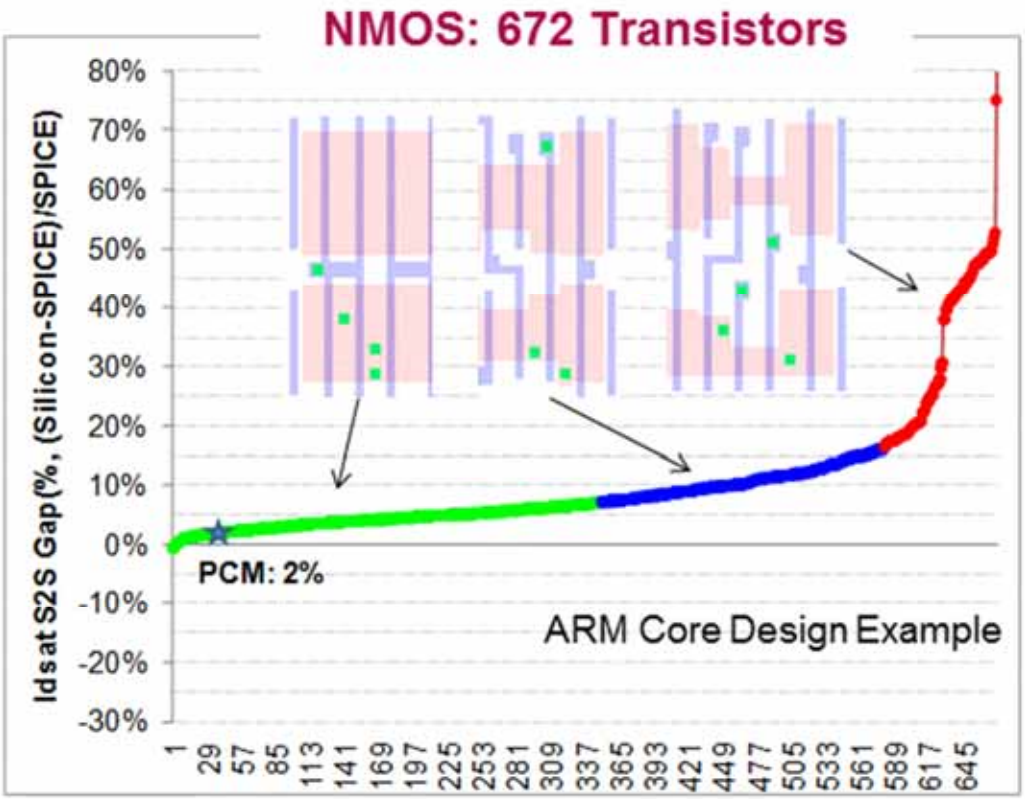
DATA → Update SPICE (and timing) models, improve layout, adjust the process

Source: B. Nehrer, PDF, EDTM'2017

PDF SOLUTIONS

Silicon-SPICE Gap Summary from DPCV Example





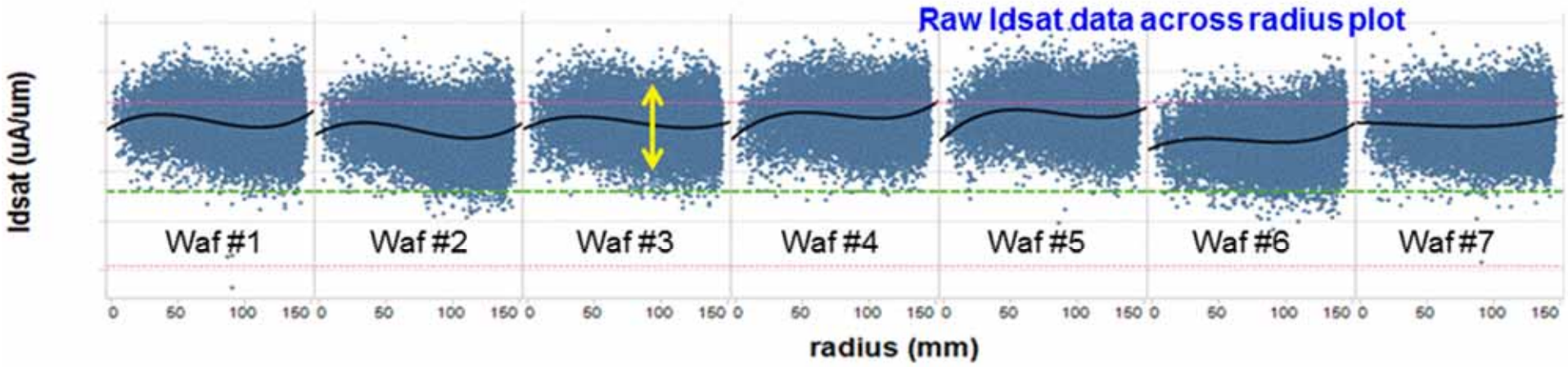
Direct Probe CV® Results

- Green parts: can be explained by model accuracy (target +/- 5%) or covered through corner setting
- Blue parts: Foundry needs to improve device Id/Vt uniformity through tightening process control, thus Fabless can use smaller guard-band for design
- Red parts: effects beyond SPICE modeling

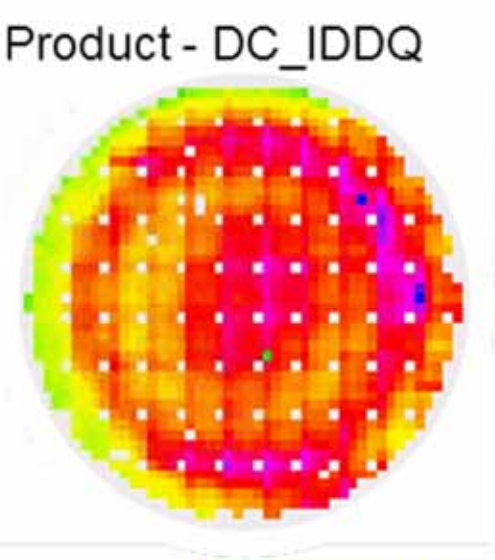
After A Strojwas, Tutorial "Variability and DFM", Short Course, VLSI Tech Symp'2014

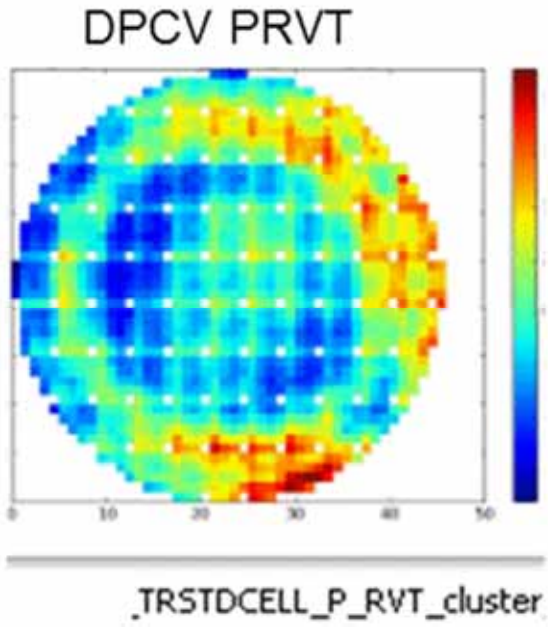
Within Wafer Variability impacting Yield

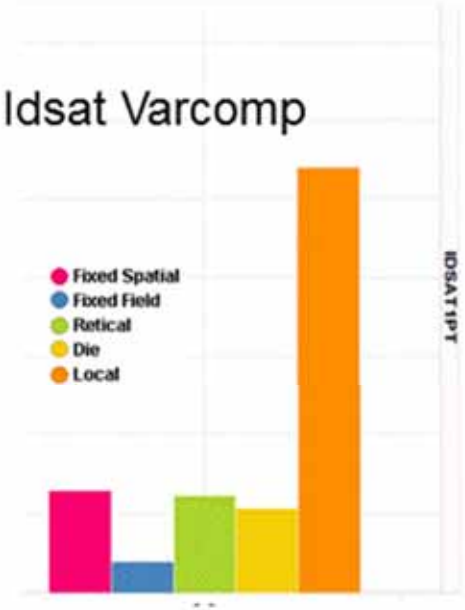
- **Statistical Data Collection and Variability Decomposition (VarComp)**



- **Wafer Maps for many devices of different Layouts tested with DPCV on Product wafers – Pattern Matching to explain IDDQ Yield Loss**



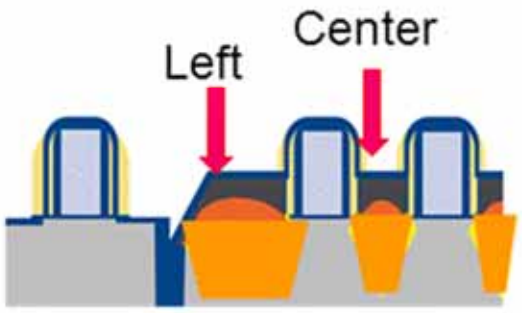




Source: PDF Solutions

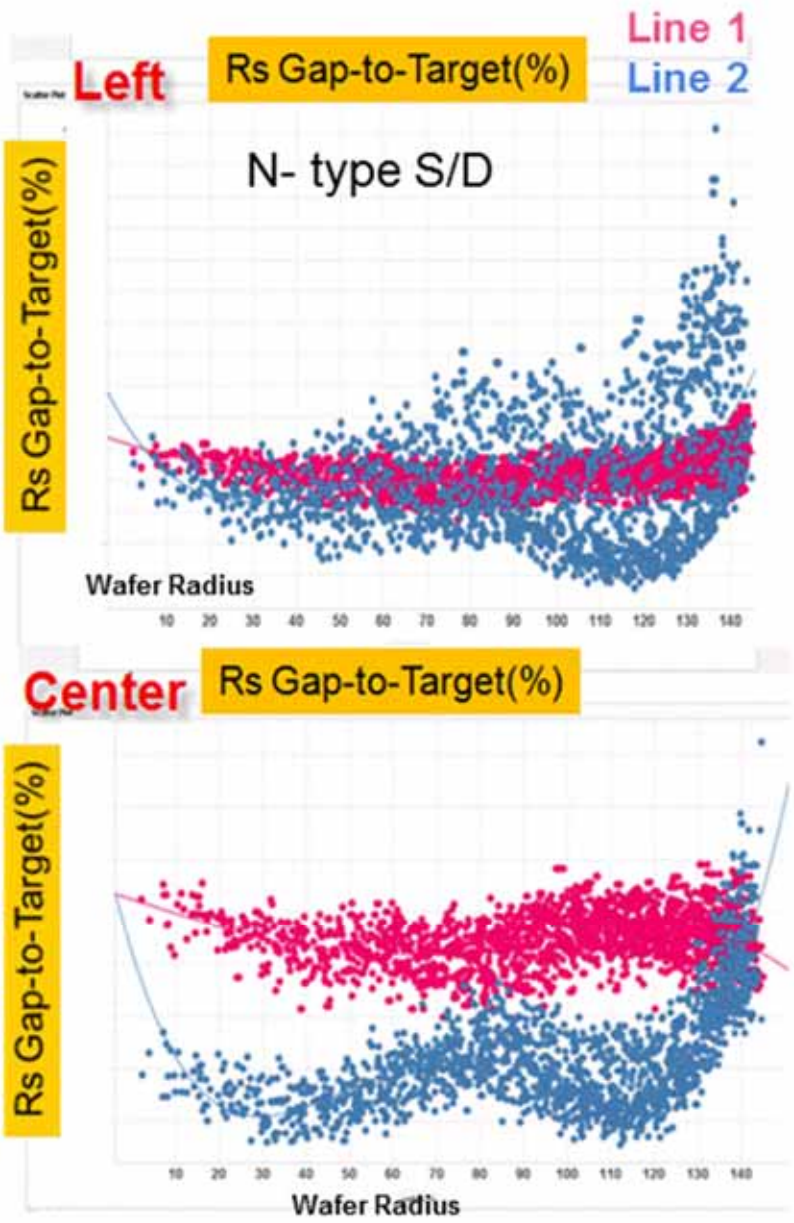
Direct Probe CV for Parametric Process Control

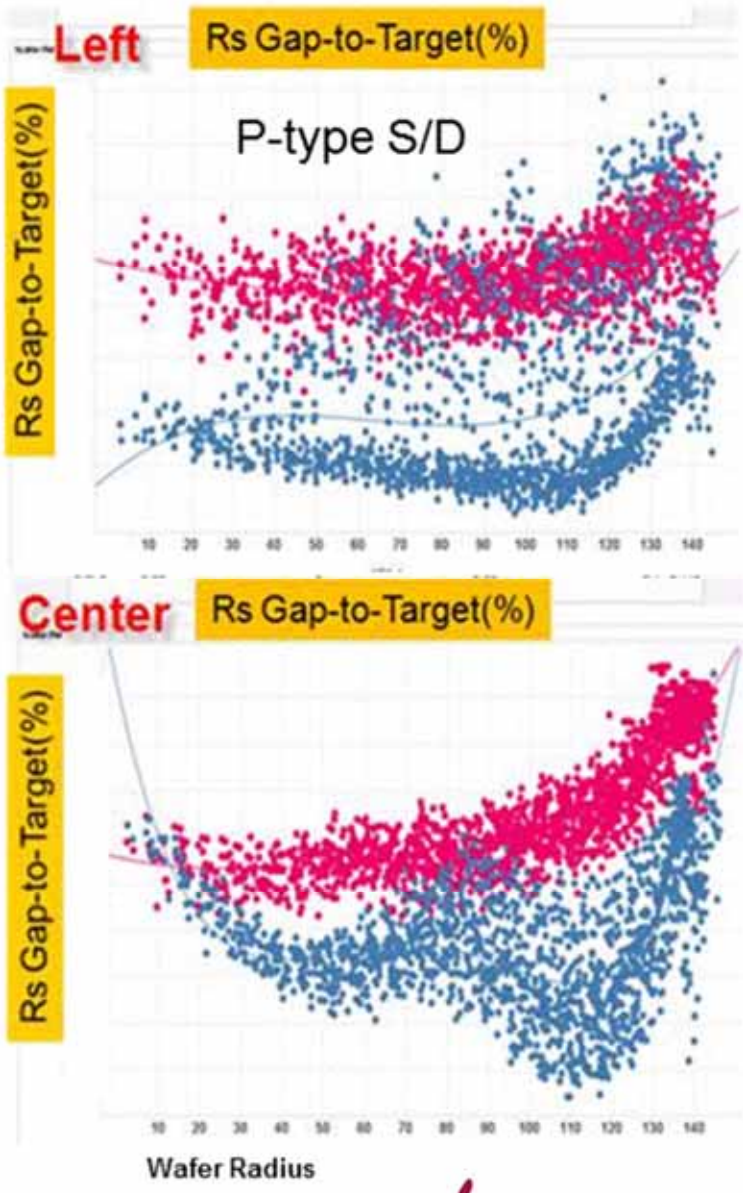
- **S/D silicide Resistance Control in devices inside Product**



- Silicon – to-SPICE check
- Fab matching for Technology Transfer
- Process characterization

Source: PDF Solutions



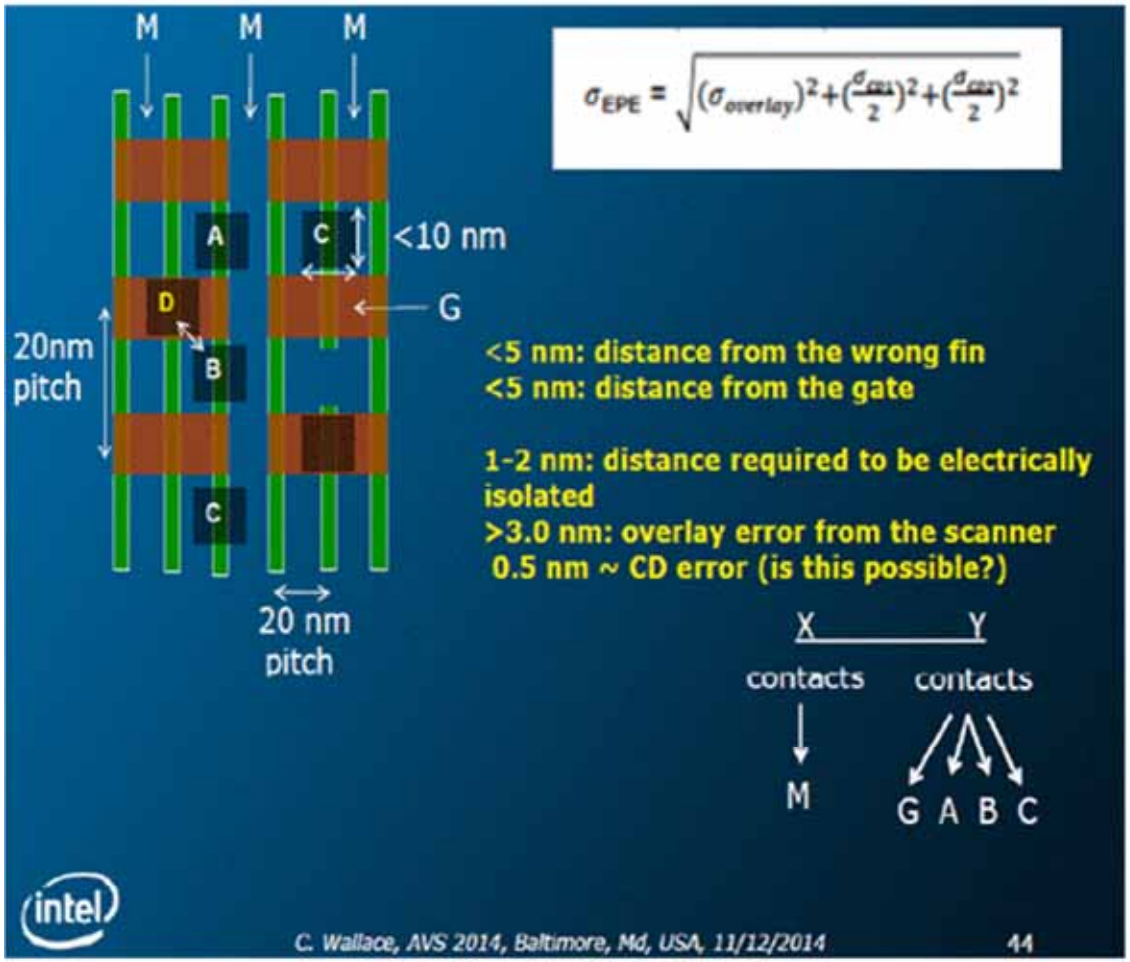


PDF SOLUTIONS

New Sources of Variability in Patterning

EPE - Edge Placement Error

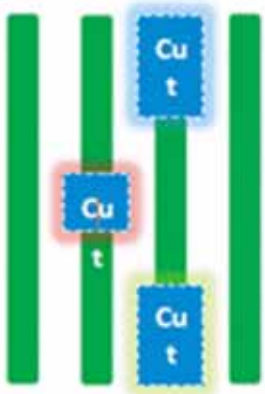
- difference between the actual location of the final pattern versus the intended location specified by the device designer



$$\sigma_{EPE} = \sqrt{(\sigma_{overlay})^2 + (\frac{\sigma_{CD1}}{2})^2 + (\frac{\sigma_{CD2}}{2})^2}$$

Past: Single pattern variation defined by CDU, overlay and LWR

Now: Multiple pattern variation defined by EPE (Edge Placement Error)



$$EPE_{Grid\ +\ cut} = f(CDU_{Grid}, LER_{Grid}, LCDU_{Grid}, OL_{Cut}, CDU_{Cut}, CER_{Cut}, LCDU_{Cut})$$

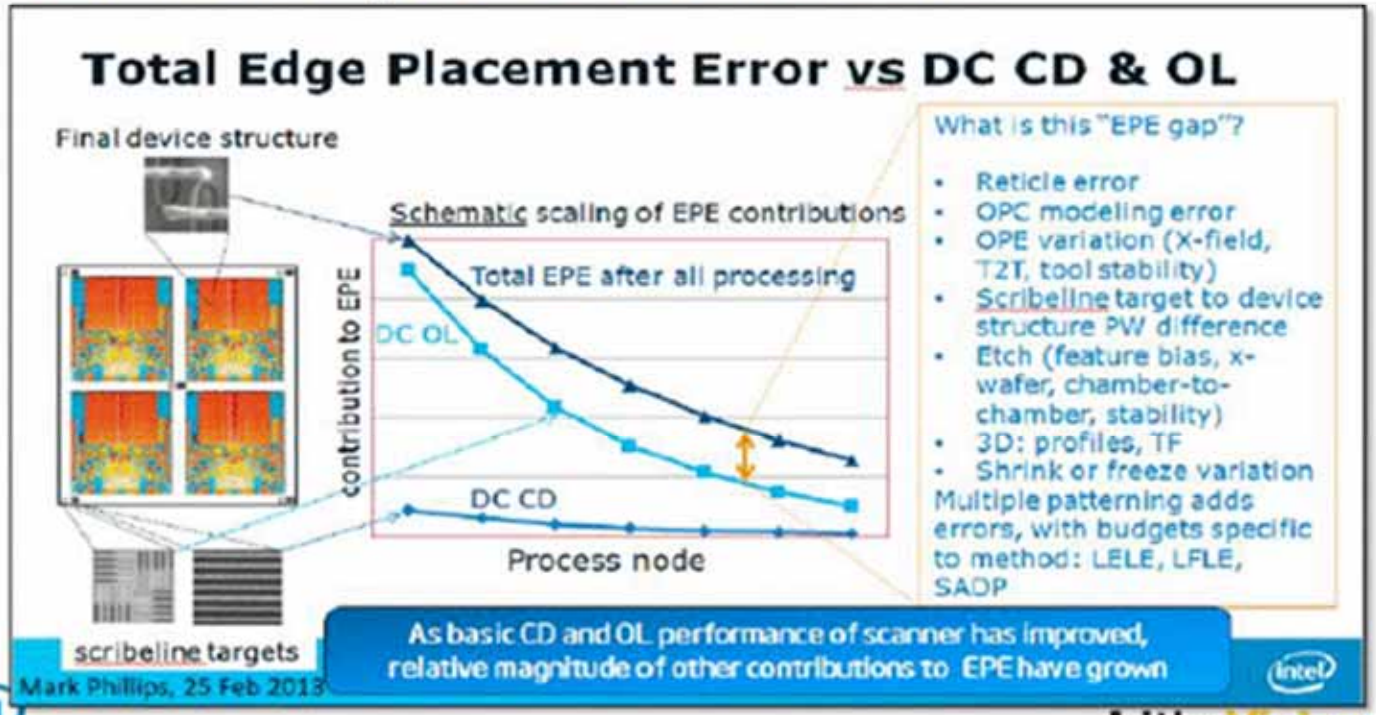
After A. Sekiguchi, Tutorial "Patterning Technology for N5", IEDM'2016

PDF SOLUTIONS

Edge Placement Error – More than CD and Overlay

Resolution isn't the only challenge

- Total Edge Placement Error is the biggest technical challenge to scaling (limiting before device physics)
  - Must reduce EPE contributions from all process steps (not just Litho) in order to take full advantage of resolution benefits of EUVL



Courtesy of Intel

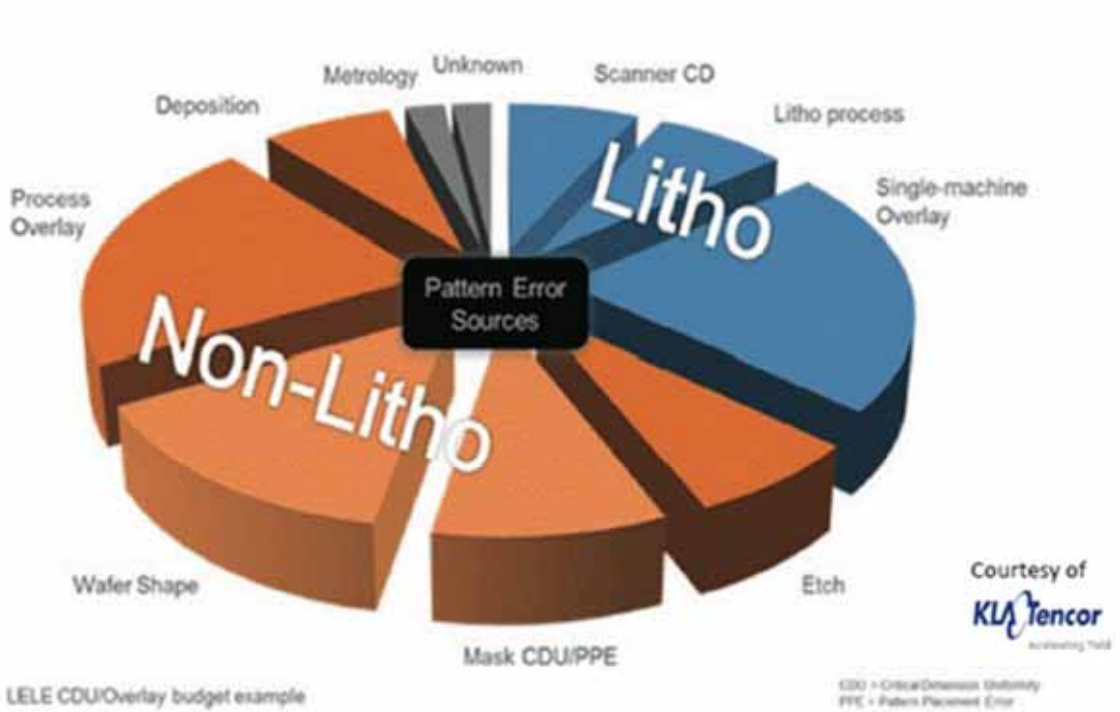
CD and OL alone cannot explain the EPE

After A. Sekiguchi, Tutorial "Patterning Technology for N5", IEDM'2016

PDF SOLUTIONS

Edge Placement Error – Root Causes and Solutions

Non-lithography factors take up more of the EPE budget



LELE CDU/Overlay budget example

Technology Node	28	20	14	10
Overlay budget	9nm	6nm	4.5nm	3.5nm
CD specs	4.5nm	3nm	2nm	1.3nm

After A. Sekiguchi, Tutorial "Patterning Technology for N5", IEDM'2016

- **Reduce the overlay error**
  - Exposure equipment fabricators priority
- **Reduce the number of overlayed shots**
  - Convert from immersion ArF to EUV
- **Optimize the EPE budget across toolsets by controlling the characteristic of processes**
  - Develop self-aligned schemes which behave independently of the overlay problem
- **Change integration schemes to get around current overlay issues:**
  - Self Aligned Contacts
  - Self Aligned Growth

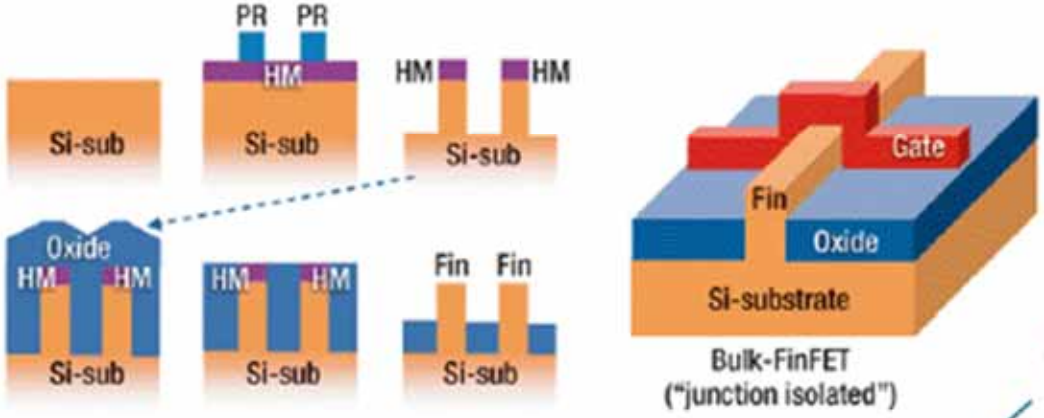
PDF SOLUTIONS

Outline

- Why does it matter – Impact on parametric yield, speed, etc
- Device variability – historical perspective and technology trends
- Sources of Variability and Process dependence
- Local Layout Effects and their Characterization
- Process variability and Characterization
- eMetrology for better process control in advanced nodes

Fin Height & Width Variation Large in Bulk FinFETs

- Additional sources of variation not present in bulk planar structures



35% W variation

18% W variation

Sources of variability	Nominal (nm)	3-sigma tolerance (current)	3-sigma tolerance (future)	
HM oxide	8	0.4	0.2	5% 3-sigma variation for oxide
HM nitride	70	7	3.5	10% 3-sigma variation for deposited nitride
Trench etch	170	8.5	4.25	5% 3-sigma from trench etch based on 32nm data
Oxide recess	100	5	2.5	Oxide dry/wet etch with no etch stop. 100nm oxide etchback for 70nm fin height assumed.
Pad oxide	2	0.1	0.05	
Well anneal	0	3	1.5	3-sigma variability in junction depth from angled implants
Total fin height variability (nm)		12.5	6.2	Root sum-square of all sources of variability
Total fin width variability (nm)		**2.5**	**1.2**	Assumption is that 20% of the vertical variability will translate to CD (Fin width) variability.

http://www.electroiq.com/articles/sst/print/volume-52/issue-11

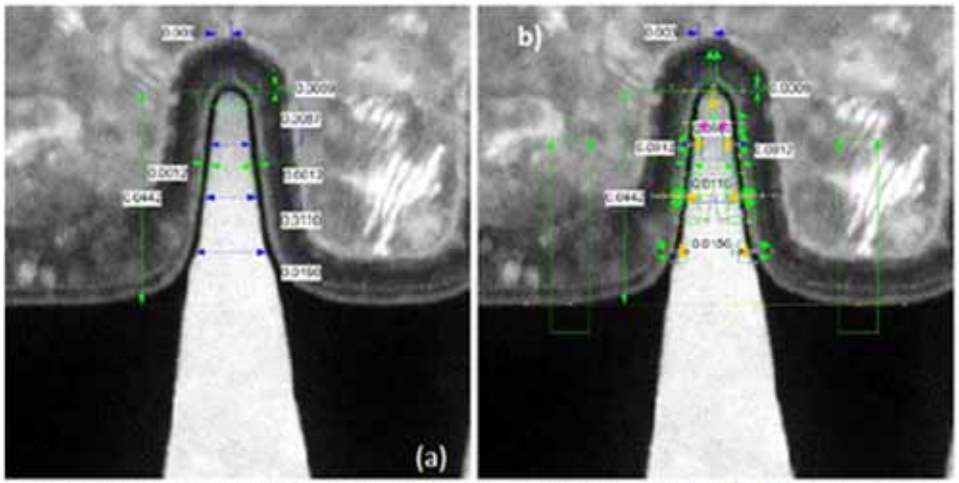
Table 2. Sources of variability for junction-isolated bulk FinFETS.

After S.Thompson, U. Florida, Device Tutorial, IEDM'2015

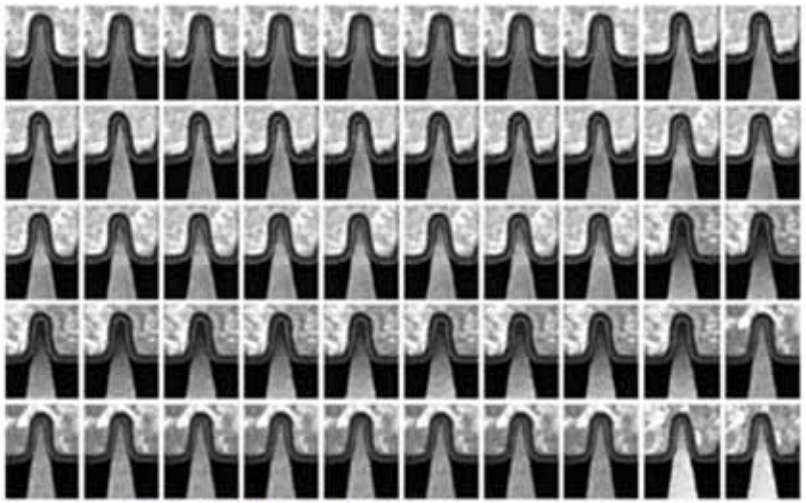
PDF SOLUTIONS

Fin Profile Monitoring with Scanning TEM

- Automated metrology capabilities of STEM demonstrated on SRAM Transistors
- Artifact-Free STEM samples 10-15nm thick prepared for Fin Profile control



Automated HAADF-STEM images are captured and analyzed to extract fin and gate oxide CDs.



A montage of the first 50 NFET images from the automated image acquisition recipe.

Table 1. Fin and gate oxide metrology data for 22nm fi

Feature	(Automated) Average CD (nm)	(Automated) Dynamic Precision (nm 3-σ)
Fin width at 75%	8.48	0.16
Fin width at 50%	10.97	0.14
Fin width at 25%	15.23	0.14
Fin Height	45.10	0.16
Top Gate Oxide	1.19	0.26
Left Gate Oxide	1.41	0.14
Right Gate Oxide	1.22	0.16
Tip Radius	2.50	0.17

CD and dynamic precision values from automated metrology measurements were obtained from a total of 180 images of 18 SRAM inverter transistors (6 each from pFETs and 12 each from nFETs)

3σ precision values were derived from the square root of the average of the variance at each site.

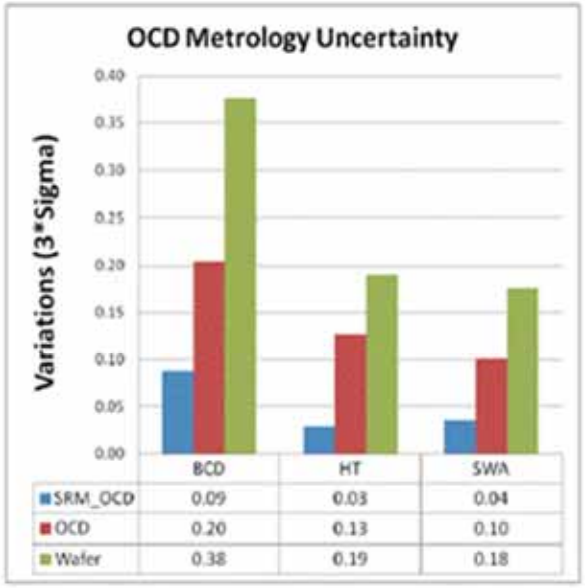
Source: O.Ugurlu, FEI, 22nm FinFET (Intel) SPIE'2013

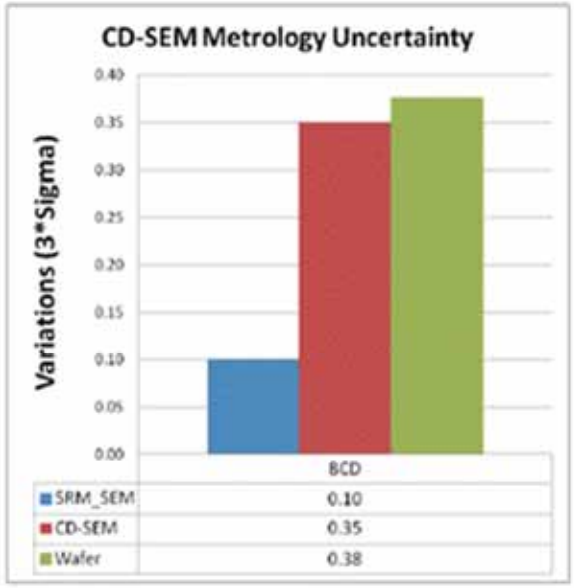
PDF SOLUTIONS

Advanced Metrology

Scatterometry

- OCD (optical CD metrology)
- Gate/Fin CD, Height, Sidewall Angle
- Spacer Thickness
- Cavity Etch, undercut, Epi Growth
- Trench Width, Depth, Sidewall Angle





SRM – Signal Response Metrology

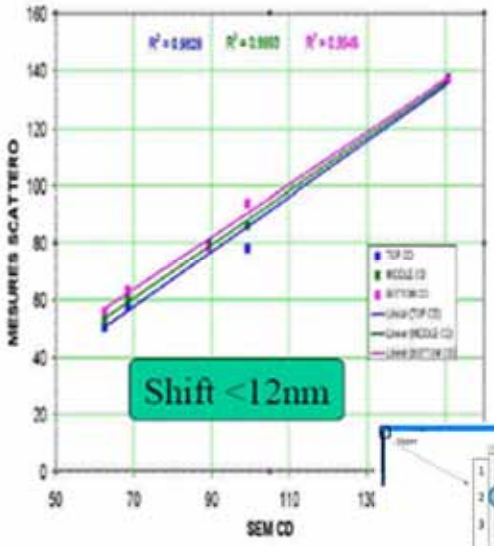
Review of CD Measurement And Scatterometry.

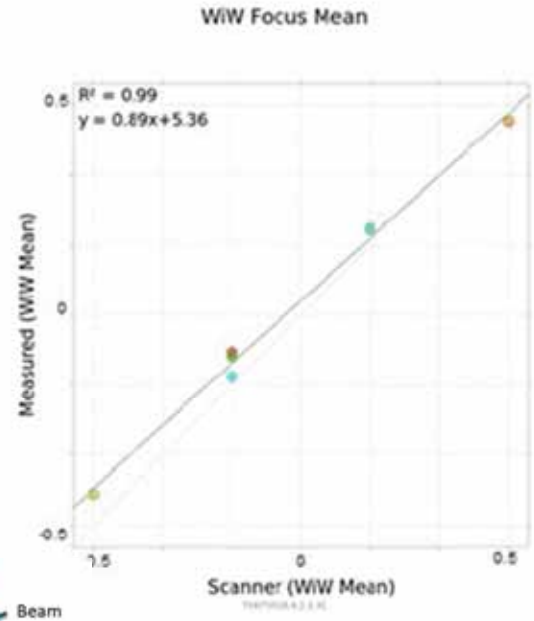
Ph Thony, D. Herisson, D. Henry, Ermes Severgnini, Mauro Vasconi

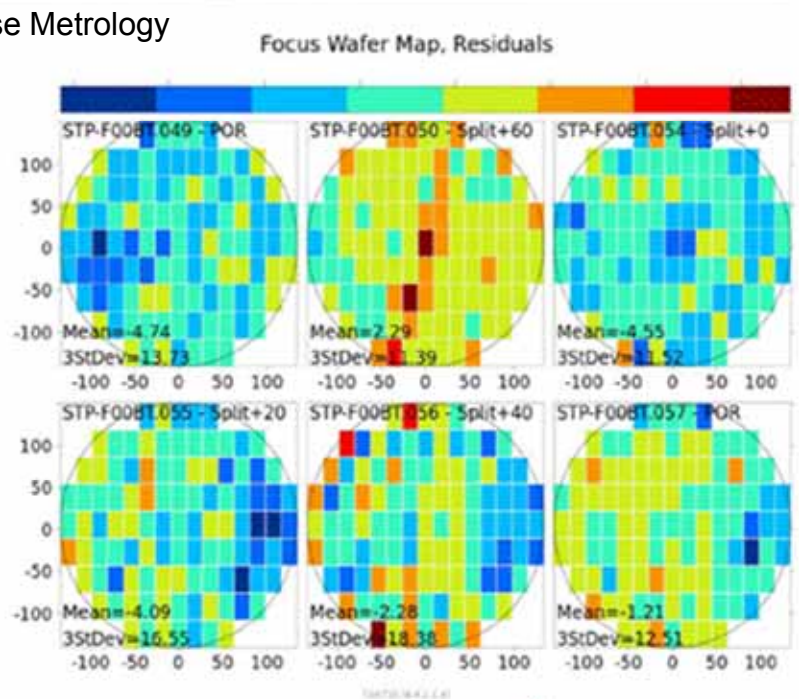
2003 STMicroelectronics – CEA/LETI

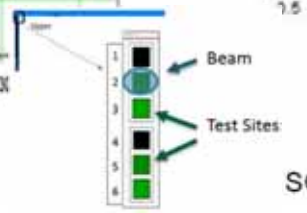
Crolles2 project MOTOROLA PHILIPS

CD-SEM







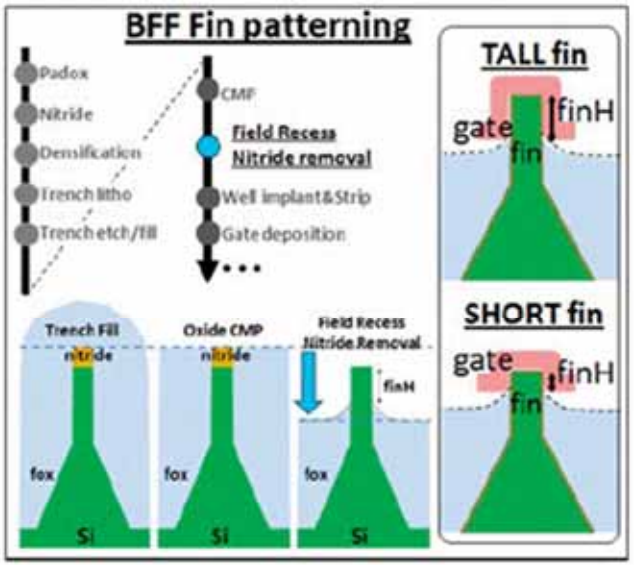


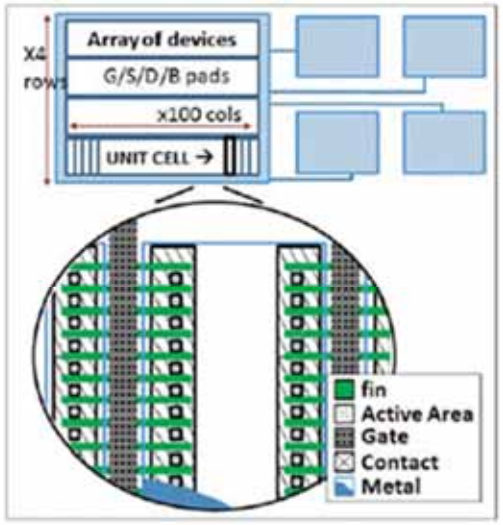
After Fang Fang, GF/KLA, SPIE'2016

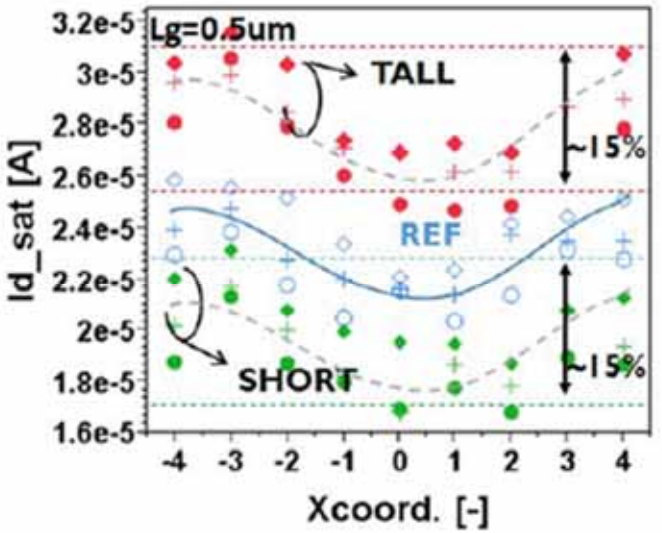
PDF SOLUTIONS

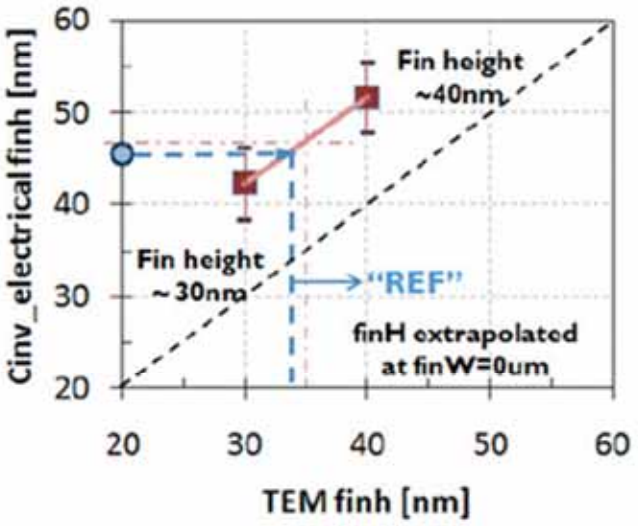
Electrical Metrology for Fin Height

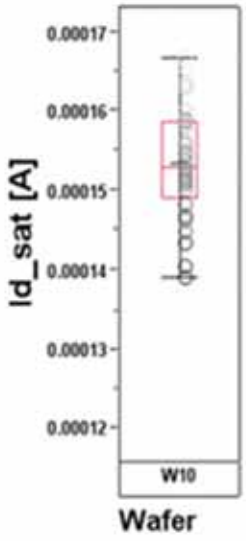
- Fin Height control one of the main sources of FinFET Id variability
- Capacitance measurements of “Fin Array” validated by Current variability

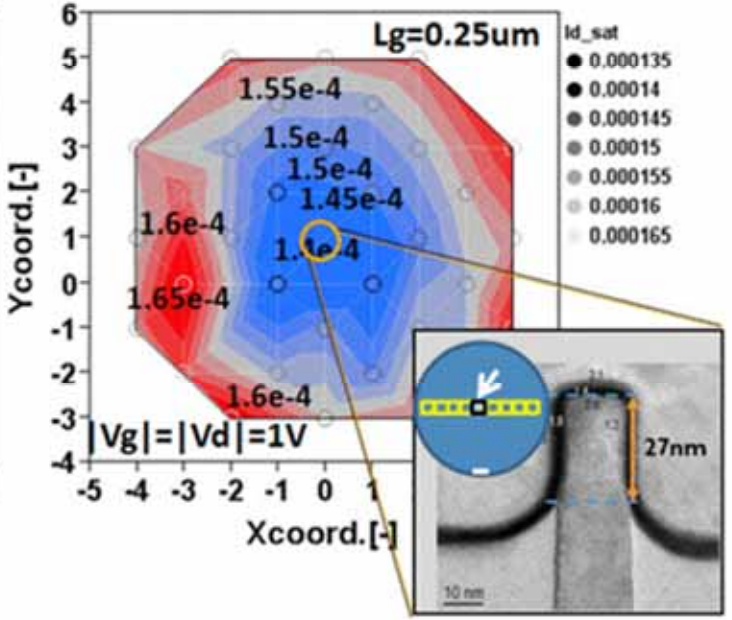












Complete device is built from a 4x100 array of devices from which G/S/D/B pads can be accessed

Source: T.Chiarella, IMEC, ICMTS ‘2011

PDF SOLUTIONS

Electrical Metrology (eMetrology) Objectives

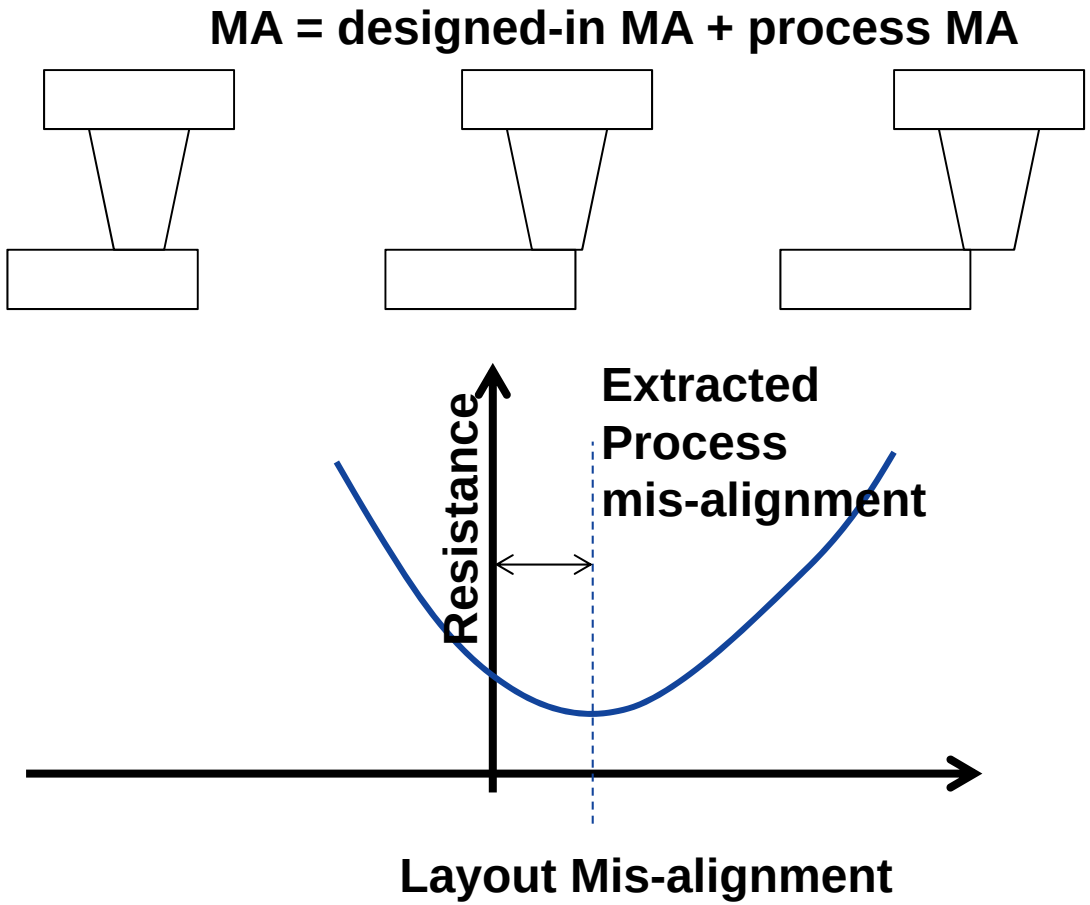
- **Provide infrastructure for high throughput monitoring of technology parameters critical for product performance and variability**
  - Focus is on variability characterization
- **Leverage CV (Characterization Vehicle) infrastructure for compact test structures and fast parallel test**
  - Electrical tests including Resistance and Capacitance
- **Increase areas of application during technology development, yield ramps, and mass production**
  - Device performance diagnosis
  - Yield Process Window
- **Identify new applications**
  - Technology finger-printing for technology transfer and benchmarking
  - Tool level drill down from excursions and drifts

Metrology Target	Typically monitored parameters
FEOL Transistor	• Gate-capacitance (Cgg) • Overlap-capacitance (Cgd) • Tox, ECD, Leff, ueff, WF (long-channel VT) • RSD
Misalignment	• Gate Cut • Contact – to Gate and to Active • Via to Upper/Lower Metal • Contacts and Local Interconnects • Multi-color patetrning (e.g. M1-E1 to M1-E2)
BEOL Metrology	• BEOL RC • Vx bottom CD • Trench Depth • ILD Thickness
FDSOI & DT	•Tsi & Tbox

Source: PDF Solutions

PDF SOLUTIONS

Concept of eMA (Electrical Mis-Alignment)



- **eMA uses a set of DUT structures to extract process mis-alignment.**
- **Additional DOE factors, e.g. horizontal vs. vertical, can be designed per client request.**

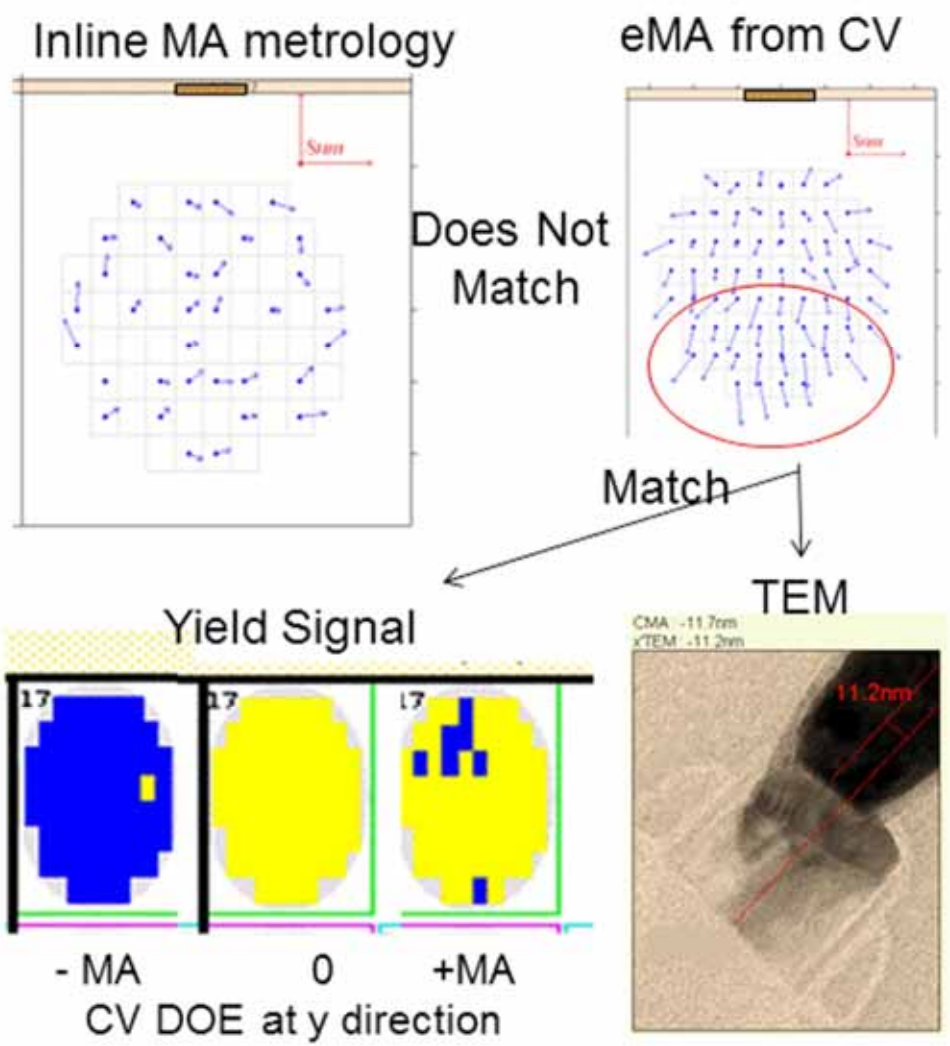
Source: PDF Solutions

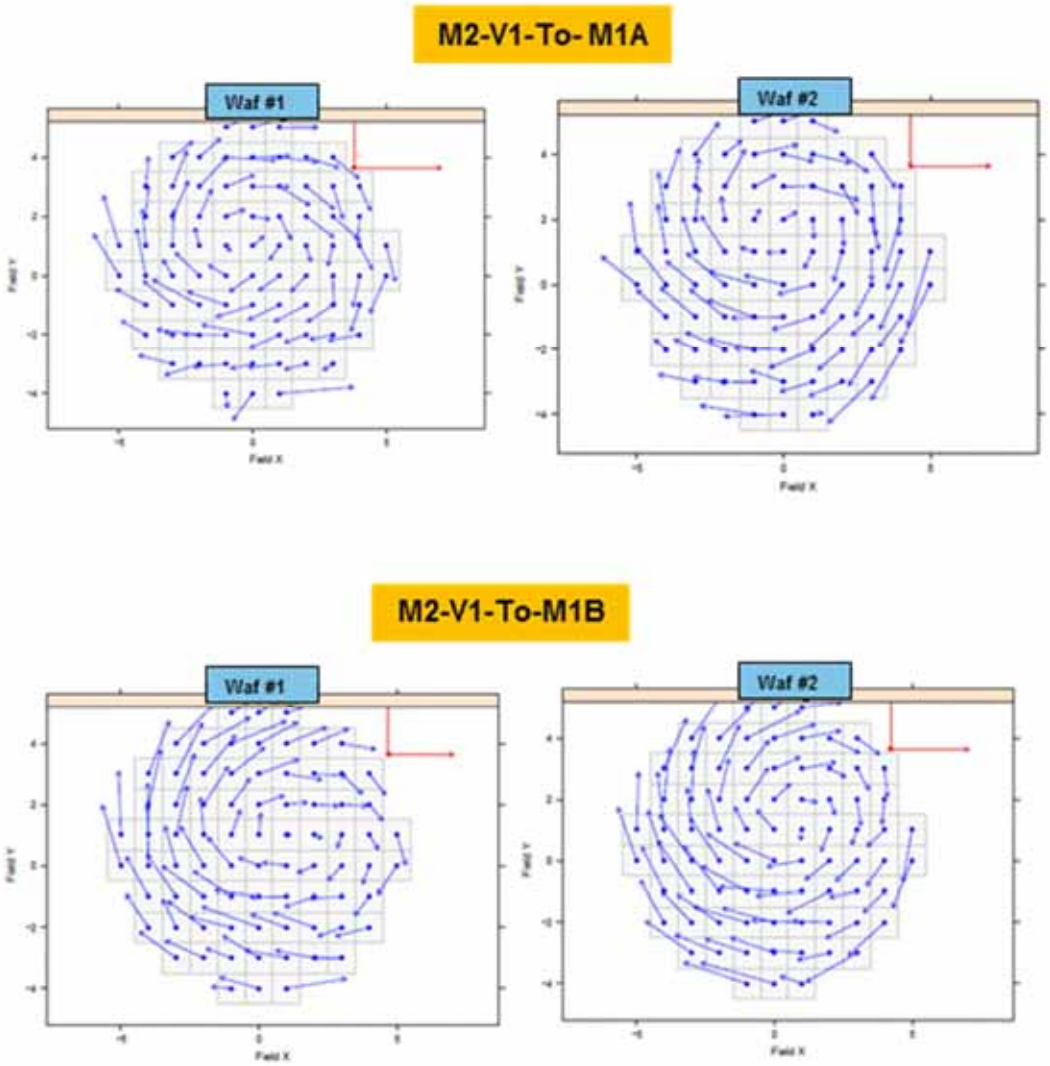
eMA is insensitive to

- Via size : due to same via size change on all structures in the DOE set (assume uniform local variation)
- Upper and lower layer CD : for the same reason above
- Upper and lower border pull back : for the same reason above
- Thickness between layers : for the same reason above
- Defectivity : redundancy and safeguard DUT included
- Wafer tile & rotation on metrology equipment, wafer warpage impact on metrology error (aberrations etc) : no impact

PDF SOLUTIONS

eMetrology Examples: Resistive Method for Misalignment





- **X & Y misalignment across the wafer**

Source: PDF Solutions

Small Capacitance Measurements – CBCM Technique

- CBCM – Charge Based Capacitance Measurements
- Requires special circuitry designed on the Test Chip (with Active Devices)
- Capable of fF level measurements
- Suitable for eMetrology for Process Control in FEOL, MOL, and BEOL

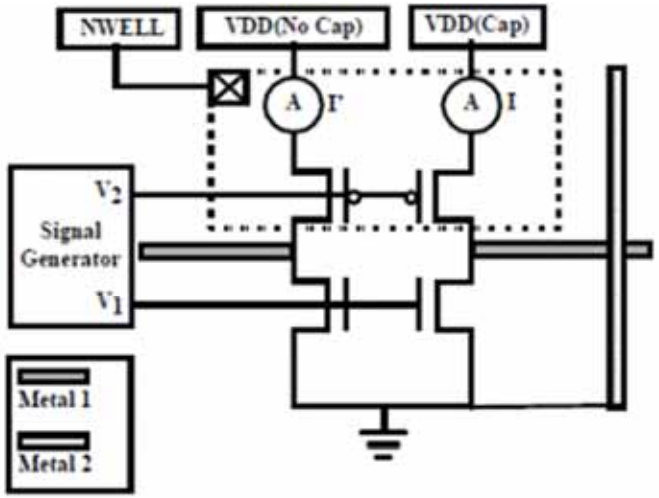
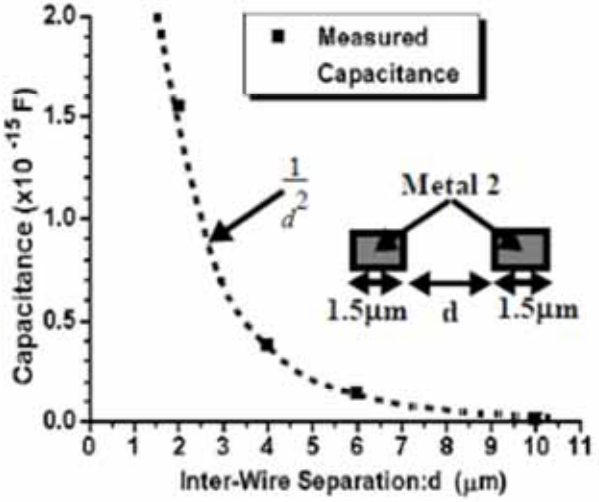
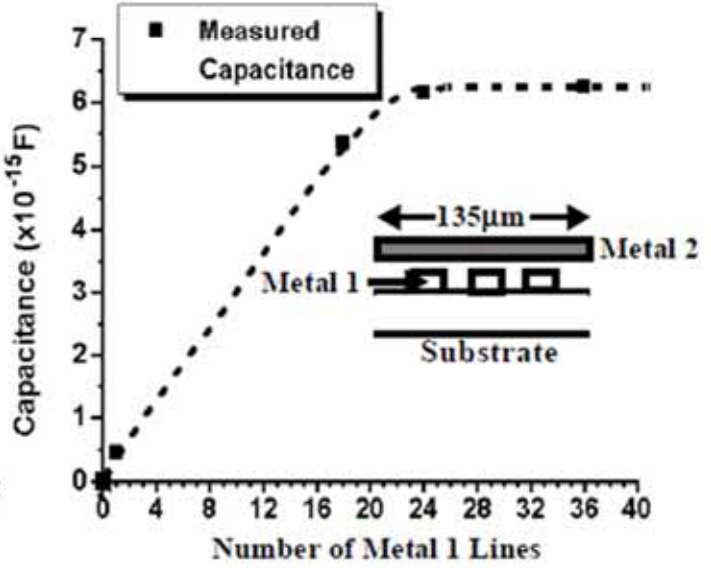


Figure 1. Proposed test structure for interconnect capacitance characterization.

Source: J. C. Chen, UCBerkeley, IEDM'1996



. Measured Metal 2 inter-wire capacitance



Measured Metal 1 to Metal 2 overlap

PDF SOLUTIONS

Summary

- **Variability is not going anywhere**
  - Random Variability will decrease as Gate/Fin LWR control improves and Doping is eliminated
  - Even if we can continue to reduce variability, Vdd reduction for Low Power and IoT will consume all available budget
  - Patterning will contribute to variability significantly during multi-patterning nodes (until temporary EUVL relief)

- **Local layout effects will decrease**
  - Restricted Design Rules will reduce freedom and number of allowable patterns
  - Further scaling will force Fin depopulation and further reduce number of allowable device design variants

- **Test structures and electrical measurements will continue to dominate transistor characterization**
  - Ultimate metric of device performance and variability
  - In-product and in-die measurements will be more important for fast IP design validation and debug

What is needed down the road

- **Better process with better controllability**
  - Self-aligned Patterning
  - Pattern smoothing and healing techniques
  - Better Etch Control - Better selectivity, Atomic Layer Etch
  - More uniform material deposition – Atomic Layer Deposition

- **Variation tolerant designs**
  - Regular designs with low variability, easy to characterize
  - Assist circuitry for Variation tolerant designs

- **Better characterization techniques**
  - Fast and precise In-line metrology
  - eMetrology – faster, denser, with more coverage
  - Complete coverage of physical, material, and geometrical parameters
  - Full wafer data collection with high statistical resolution
  - Big Data for correlation across all databases for Yield, metrology, and e-Test
  - Feedback loop to manufacturing through APC and FDC