The Emerging Ecosystem of Open-Source IC Design

Boris Murmann
Chair, IEEE SSCS TC-OSE
May 23, 2023

Stanford | ENGINEERING
Electrical Engineering

murmann mixed|signal

The Washington Post

TECHNOLOGY

Economic future of U.S. depends on making engineering cool

Purdue University races to expand semiconductor education to fill yawning workforce gap that threatens reshoring effort

By Jeanne Whalen

October 23, 2022 at 7:00 a.m. EDT

SIGN IN The Register

{* SYSTEMS *}

America's chip land has another potential shortage: Electronics engineers

Why screw around writing Verilog when you can earn tons more with Python, Java or Go?

Dylan Martin

Fri 8 Jul 2022 // 18:28 UTC

51

EE Times EUROPE

News Focus Opinion Education Magazine

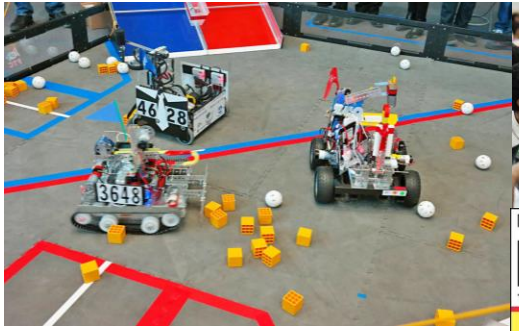
News Trends

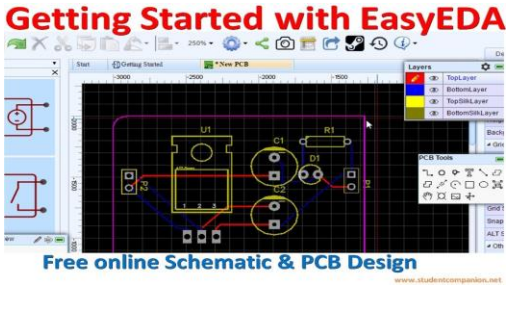
Europe's Semiconductor Talent Gap Widens

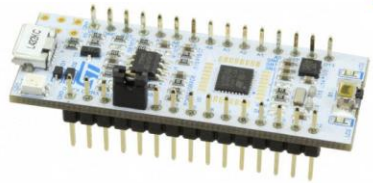
January 4, 2023 Anne-Françoise Pelé

Today's Competition for Talent

- Tech-savvy students at HW/SW intersection thrive on collaborative/maker culture
- Infrastructure enabled by integrated circuits!





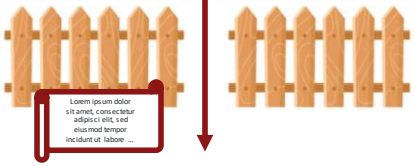


PyTorch

ACM/IEEE TinyML Design Contest at ICCAD

IC Research “Ecosystem”

Proprietary EDA tools



reinforcement learning
continuous integration
silicon compiler
open source

Useful IP

“Your EDA friend”

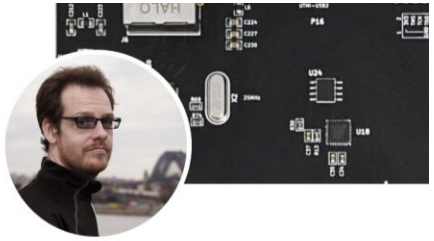
NDA

Manufacturable PDK

Toy PDK

Big-Bang Events: Open-Source PDKs

- First open-source PDK (November 2020)
  - SkyWater 130nm CMOS
  - https://github.com/google/skywater-pdk
- Second open-source PDK (October 2022)
  - GlobalFoundries 180nm MCU
  - https://github.com/google/gf180mcu-pdk
- Third open-source PDK (March 2023)
  - IHP 130nm BiCMOS
  - https://github.com/IHP-GmbH/IHP-Open-PDK
- Permissive Apache 2.0 licensing



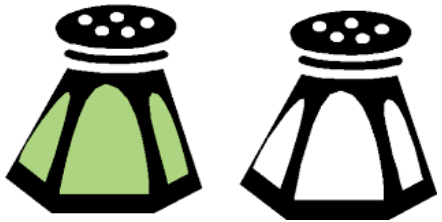
Tim (mithro) Ansell (They/Them) · 1st
Software Engineer at Google

Google + skywater TECHNOLOGY + ihp + GLOBAL FOUNDRIES

Open Source in a Nutshell

- Core principles
  - Open exchange, collaboration, transparency, meritocracy
- Typical benefits (as seen in the software community)
  - Improves productivity, managing complexity
  - Enables community review and steady improvements, re-use
  - Promotes education and tinkering
- Open source does not imply “free”
  - Can make money with open-source products (Red Hat, Ruby on Rails, …)
  - Proper terminology
    - Proprietary vs. open source (NOT: commercial vs. open source)

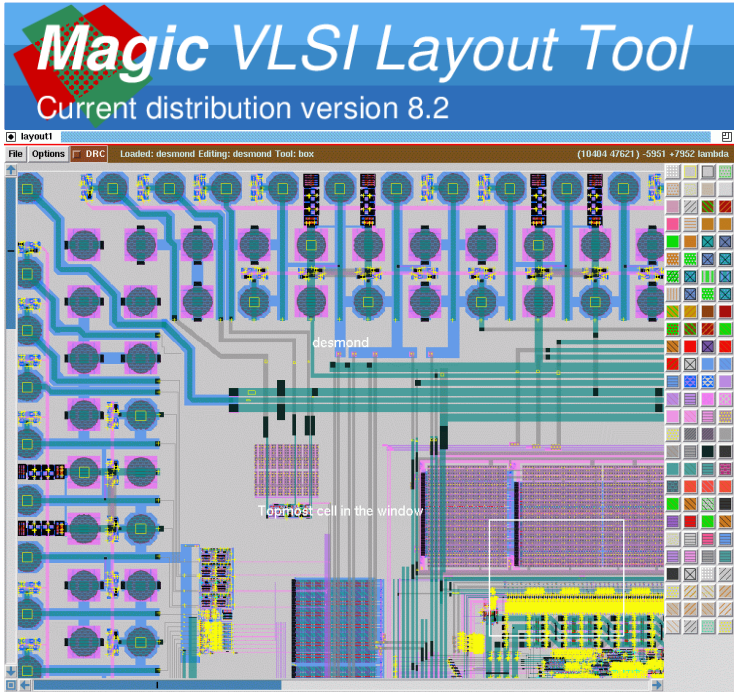
Open Source is in Our DNA!



SPICE (Simulation Program with Integrated Circuit Emphasis)

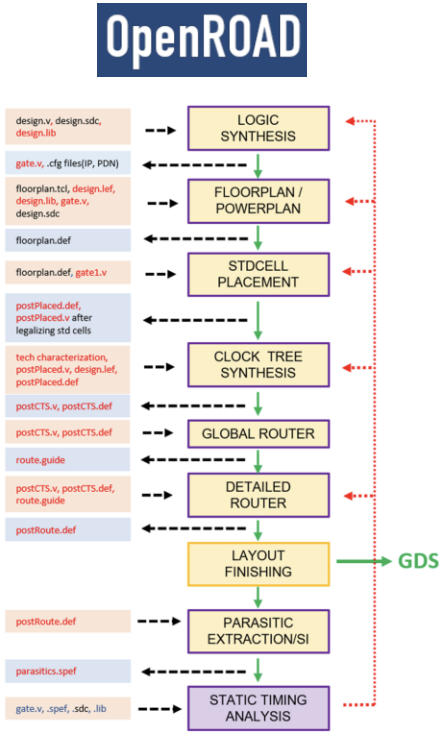
Laurence W. Nagel and D.O. Pederson

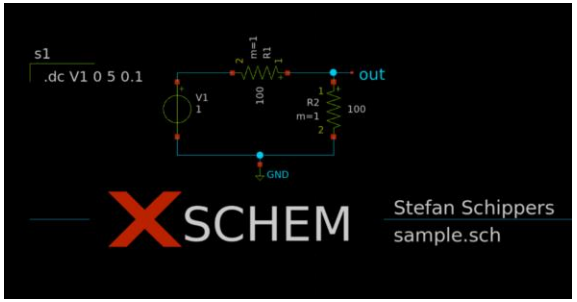
EECS Department
University of California, Berkeley
Technical Report No. UCB/ERL M382
April 1973

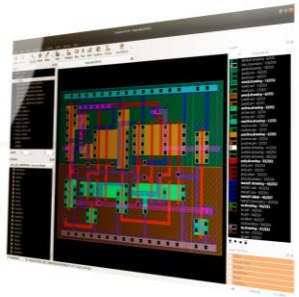


Sources: http://www.omega-enterprises.net, http://opencircuitdesign.com/magic

Examples of Today's Open-Source EDA Tools







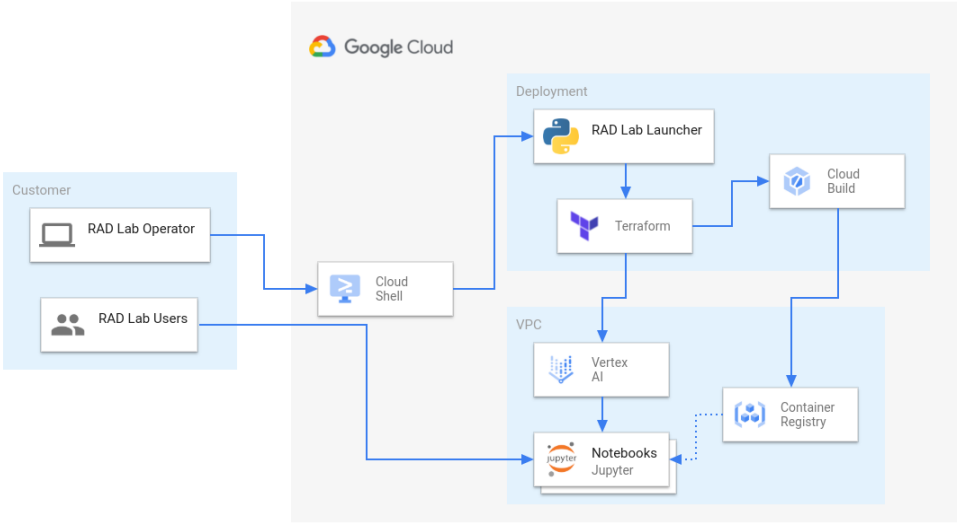
KLayout

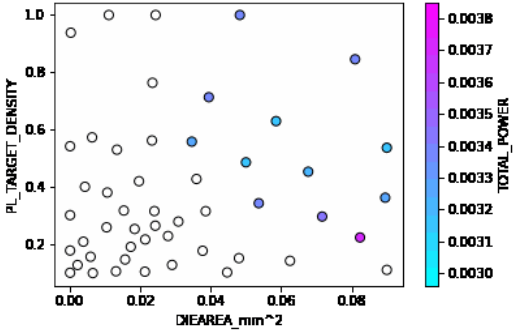
NGSPICE

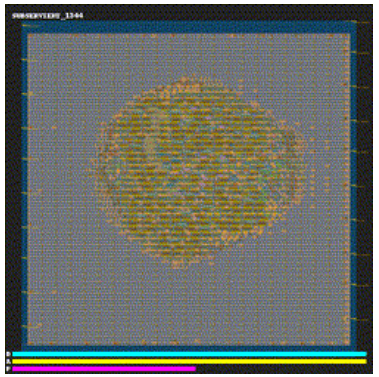
Sandia National Laboratories Xyce
Parallel electronic simulation

GDS_FACTORY

Research: Design Space Exploration in the Cloud

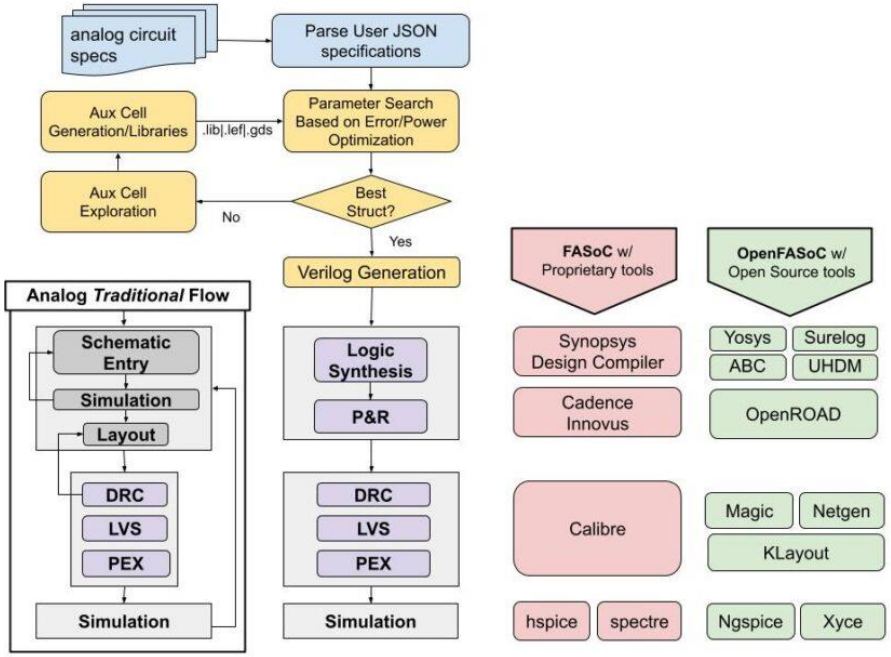






https://bit.ly/jupyter-silicon

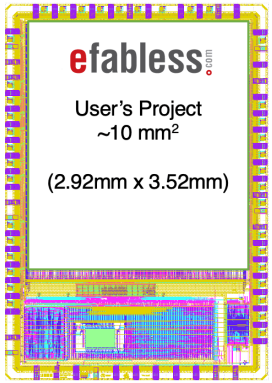
Research: New AMS Design Methodologies



https://github.com/idea-fasoc/OpenFASOC

Mehdi Saligane et al.

Industry: Start-Up Companies



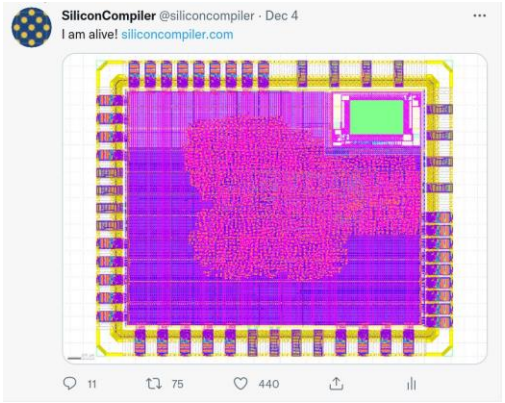
chipIgnite for Startups

Low-cost Development
Access to open-source tools enable low upfront cost for development.

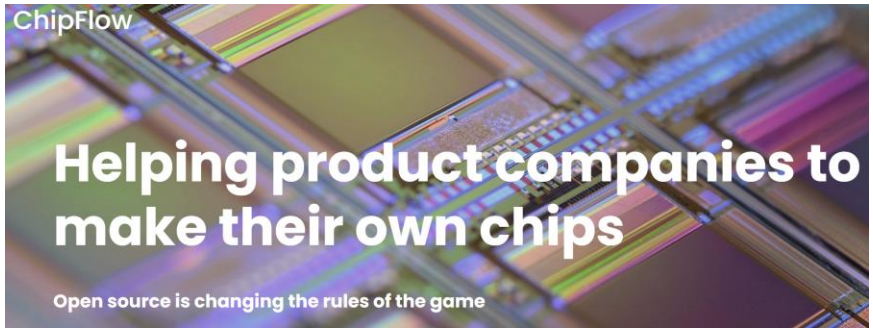
Accelerated Design
Reference designs and automated design flows enable rapid development.

You Don't Need to Be an Expert
Guided and automated flows make design easy for those without IC design experience.

zero



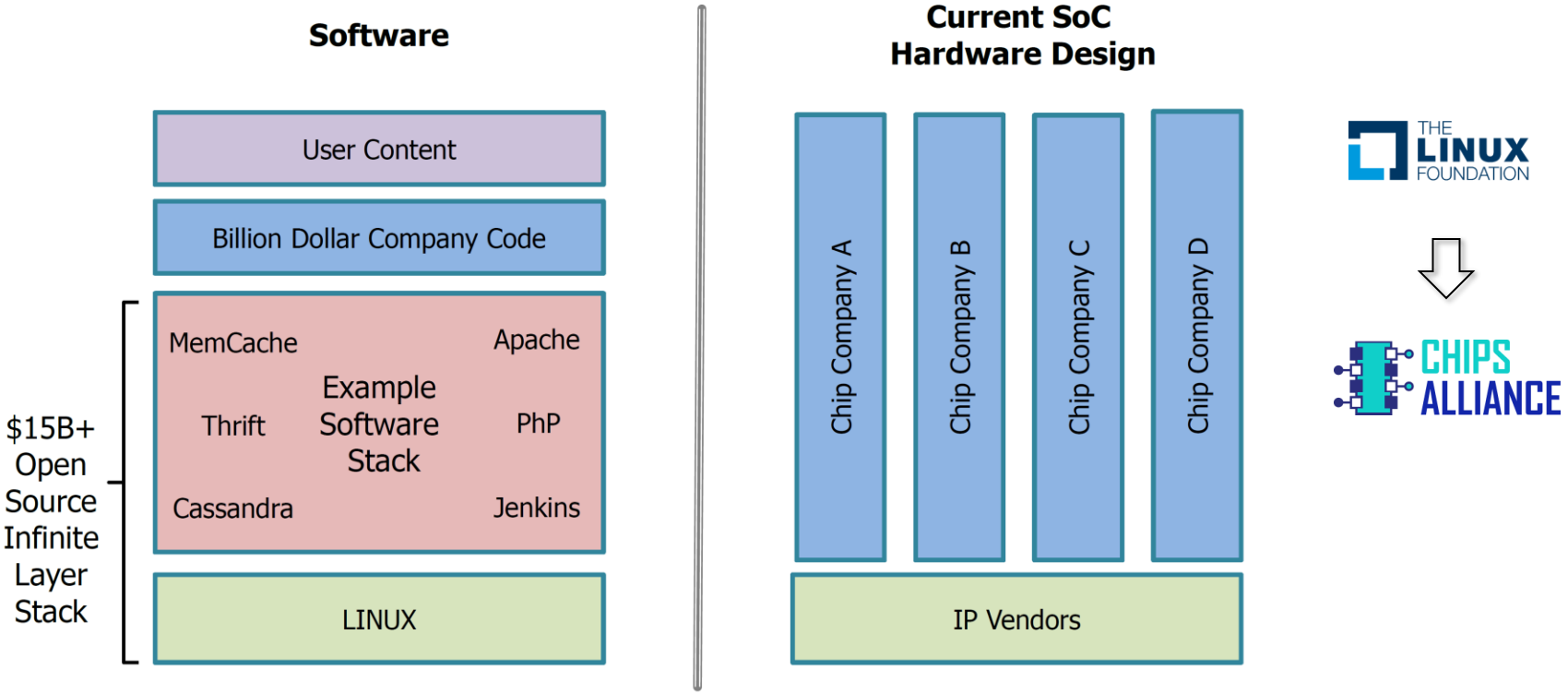
SiliconCompiler



SiliconCompiler is an open-source compiler framework that aims to automate translation from source code to silicon.

The SiliconCompiler project includes a standardized compiler data Schema, a Python object-oriented API, and a distributed systems execution model.
The project philosophy is to "make the complex possible while keeping the simple simple".

Industry: Let's Break the Silos! (Will Take Time…)



Source: Andreas Olofsson (DARPA)

Google-Sponsored (Free) Shuttle Runs

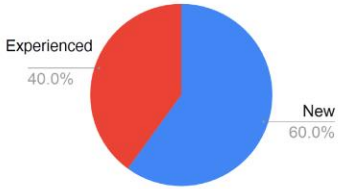
efabless.com

GOOGLE's MPW-ONE

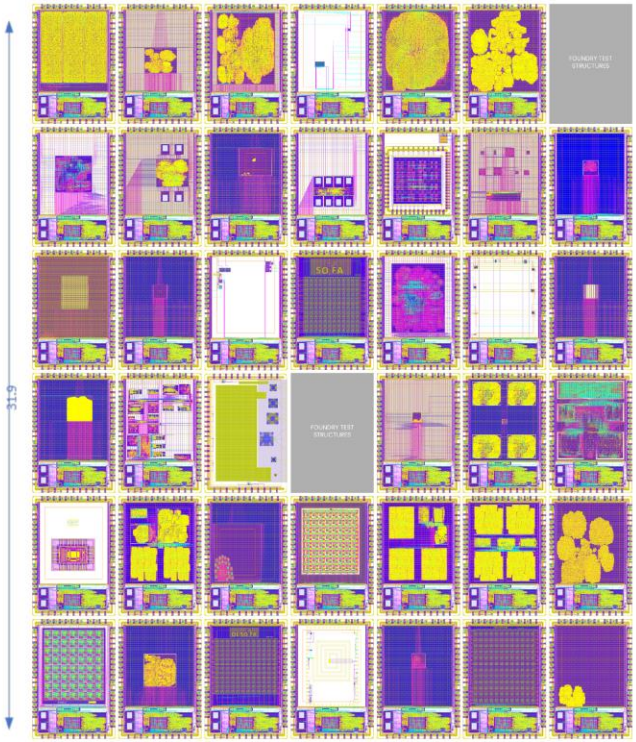
First MPW Overbooked 45/40

45 designs submitted in 30 days!

60% by first time designers!

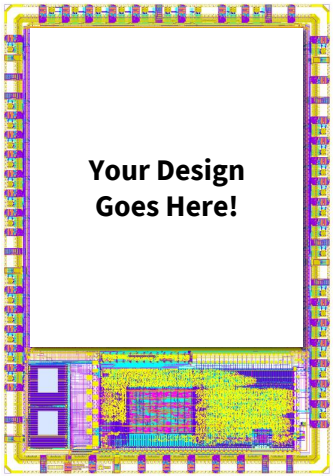


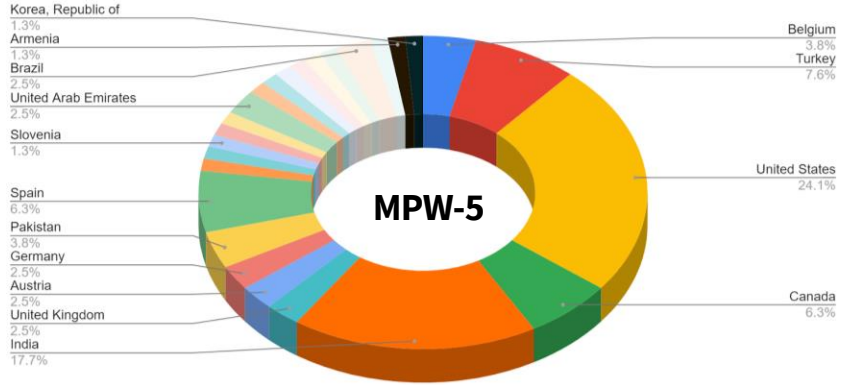
2021 EFABLESS CORPORATION

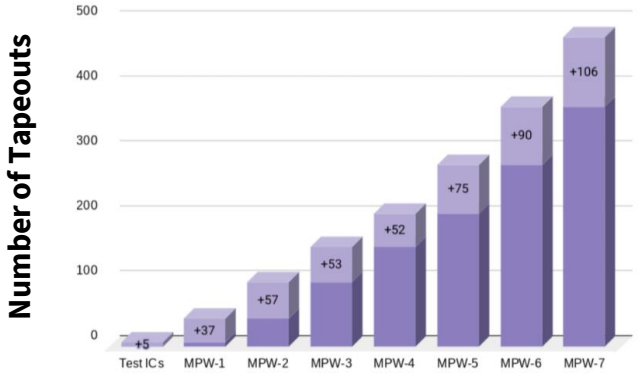


Open-Source IC Design is Taking Off!

Efabless Caravel "Harness" SoC







Monday AM Session @ ISCAS 2023

11:30 – 13:00
Review of the First Silicon Results in the Open Source Ecosystem
Room: San Carlos III (Marriott)
Session Chair(s): Mehdi Saligane, *University of Michigan*
Priyanka Raina, *Stanford University*

11:30
2273: An Open Source Compatible Framework to Fully Autonomous Digital LDO Generation
Yaswanth Kumar Cherivirala, Mehdi Saligane, David Wentzloff
University of Michigan, Ann Arbor, United States

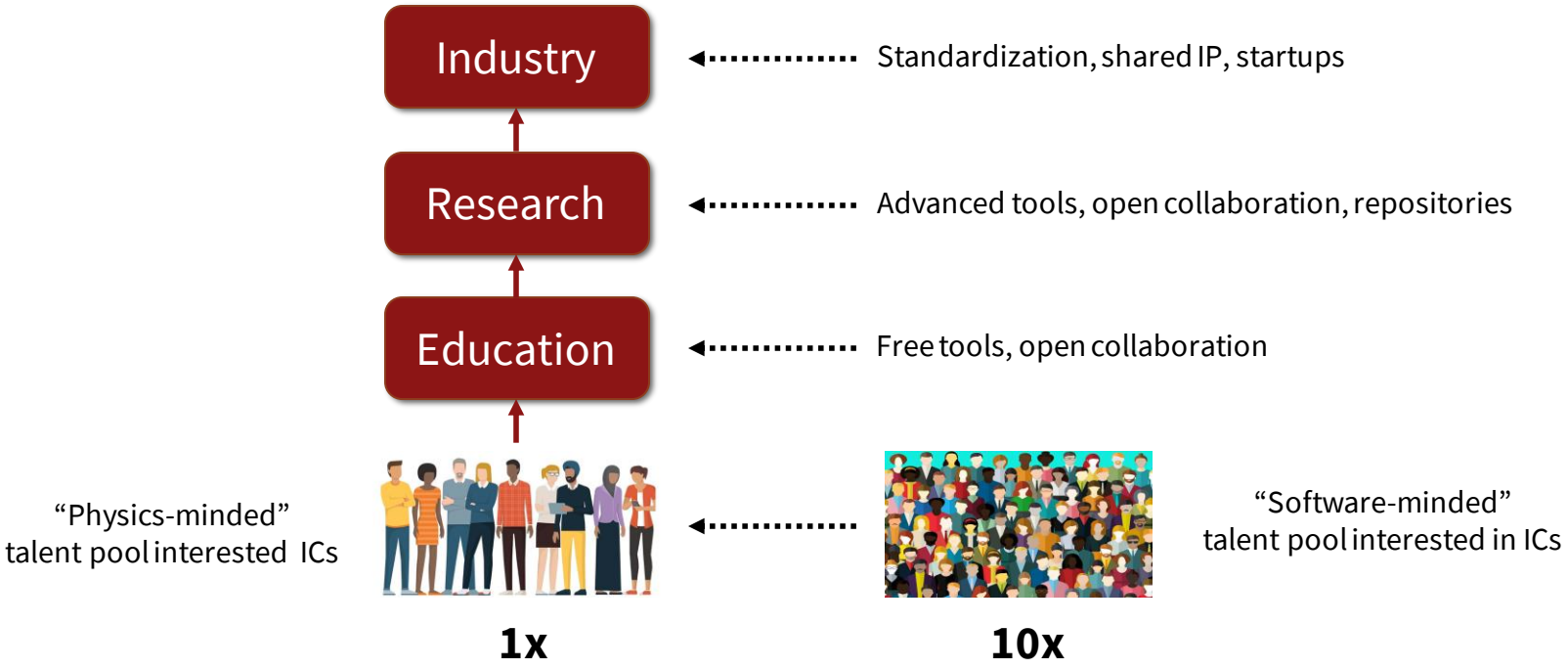
11:48
2290: Design of Cryo-CMOS Analog Circuits Using the Gm/ID Approach
Christian Enz, Hung-Chi Han
École Polytechnique Fédérale de Lausanne, Switzerland

12:06
2314: SRAM Design with OpenRAM in SkyWater 130nm
Jesse Cirimelli-Low{2}, Muhammed Hadir Khan{2}, Samuel Crow{2}, Amogh Lonkar{2}, Bugra Onal{2}, Andrew Zonenberg{1}, Matthew Guthaus{2}
{1}IO Active, United States; {2}University of California, Santa Cruz, United States

11:24
2326: An Open-Source 4x8 Coarse-Grained Reconfigurable Array Using SkyWater 130 nm Technology and Agile Hardware Design Flow
Po-Han Chen, Charles Tsao, Priyanka Raina
Stanford University, United States

12:42
2327: Open-Source, End-to-End Auditable Tapeout of Hardware Cryptography Module
Anish Singhani
Carnegie Mellon University, United States

Ecosystem Stakeholders



IEEE SOLID-STATE CIRCUITS SOCIETY™
IC Innovation

Search IEEE Solid-State Circuits Society | Search | Career Cen

HOME | ABOUT | MEMBERSHIP | EDUCATION | CONFERENCES | PUBLICATIONS | CHAPTERS | DL PROGRAM | WOMEN IN CIRCUITS

Home / Membership / Awards / ISSCC "Code-a-Chip" Travel Grant Awards

ISSCC "Code-a-Chip" Travel Grant Awards

ISSCC "Code-a-Chip" Travel Grant Awards

SUBMISSION DEADLINE: NOVEMBER 21, 2022

The ISSCC 2023 Code-a-Chip Travel Grant Award was created to (1) promote reproducible chip design using open-source tools and notebook-driven design flows and (2) enable up-and-coming talents as well as seasoned open source enthusiasts to travel to the Conference and interact with the leading-edge chip design community. This program is made possible by a donation from the CHIPS Alliance, a non-profit organization hosted by The Linux Foundation.

Program rules

- The program is open to anyone (no restrictions). Membership in the IEEE Solid-State Circuits Society (SSCS) membership is encouraged, but not required. Teaming is encouraged, but each team must identify a single leader who can travel to the ISSCC from February 19-23, 2023, to receive the award.
- Applicants must submit an open-source Jupyter notebook detailing an innovative circuit design using open-source tools (examples: inverter, temperature sensor)
- Each submission must contain a suitable open source license (e.g., Apache 2.0).

Made possible by a donation from the CHIPS Alliance

CHIPS ALLIANCE

https://sscs.ieee.org/membership/awards/ieee-sscs-code-a-chip-travel-grant-awards

Example: Winner of VLSI 2023 Code-a-Chip Contest

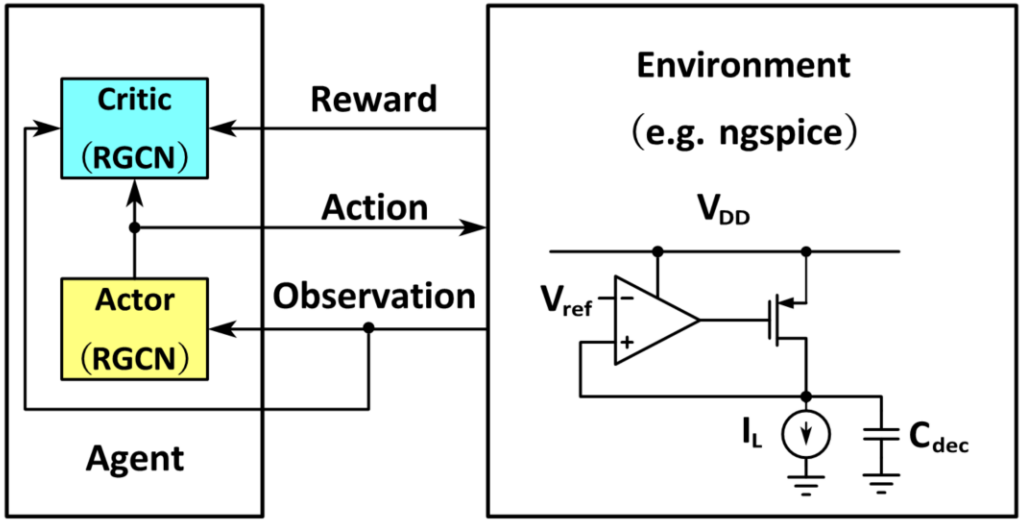
Design and Optimization of Analog LDO with Relational Graph Neural Network and Reinforcement Learning

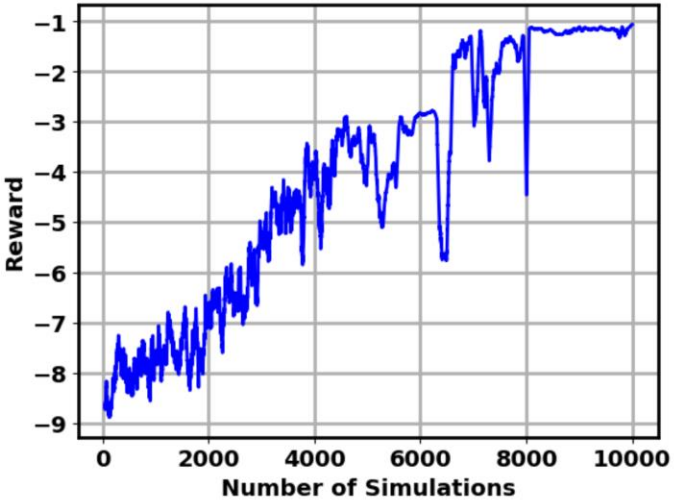
```
Zonghao Li Team, March 2023
SPDX-License-Identifier: Apache-2.0
```

Name	Affiliation	IEEE Member	SSCS Member
Zonghao Li (Lead) Email ID: zonghao.li@isl.utoronto.ca	University of Toronto	Yes	Yes
Anthony Chan Carusone (Advisor) Email ID: tony.chan.carusone@isl.utoronto.ca	University of Toronto	Yes	Yes

https://github.com/sscs-ose/sscs-ose-code-a-chip.github.io/blob/main/VLSI23/accepted_notebooks/ldo_rgcn_rl/ldo_rgcn_rl.ipynb

Example: Winner of VLSI 2023 Code-a-Chip Contest

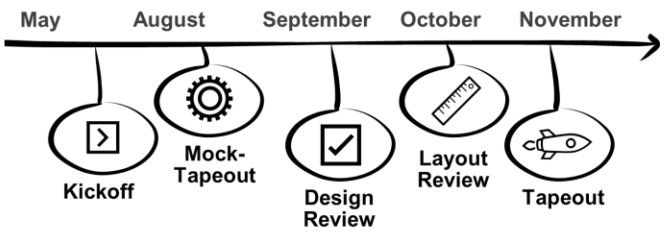


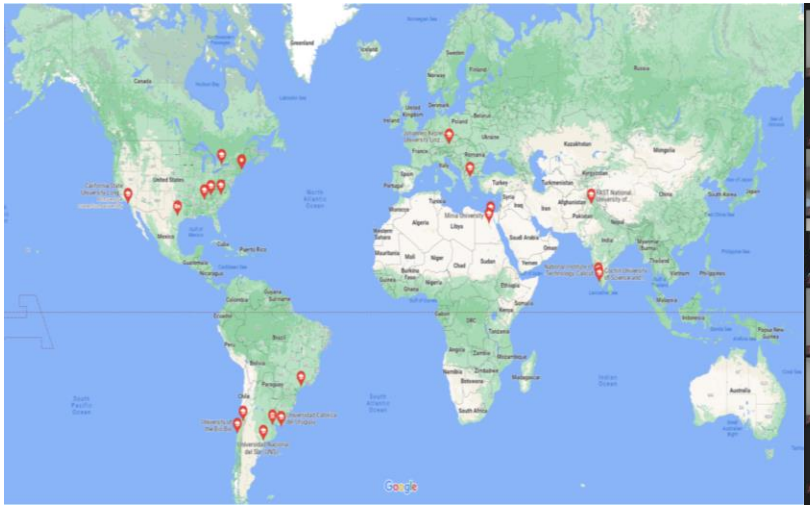


https://github.com/sscs-ose/sscs-ose-code-a-chip.github.io/blob/main/VLSI23/accepted_notebooks/ldo_rgcn_rl/ldo_rgcn_rl.ipynb

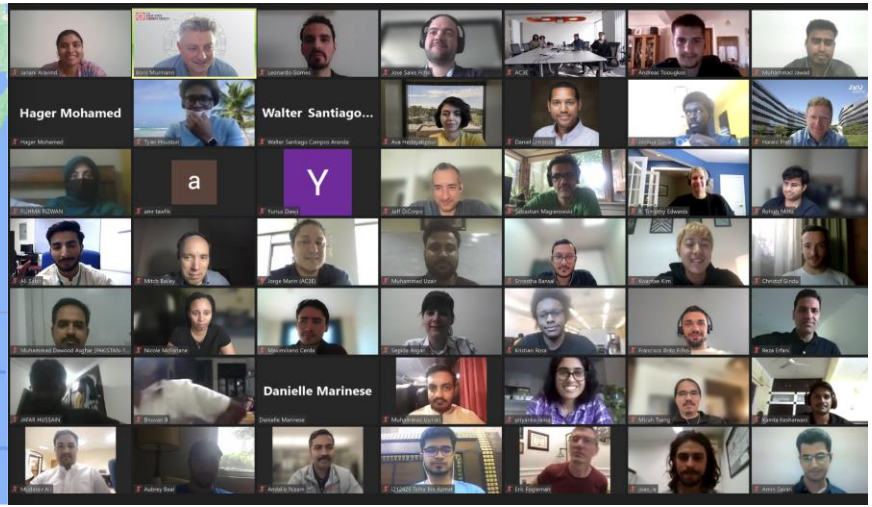
SSCS PICO Chipathon

- 2021: 61 submissions, 18 selected (11 taped out)
- 2022: 54 submissions, 22 selected (14 taped out)



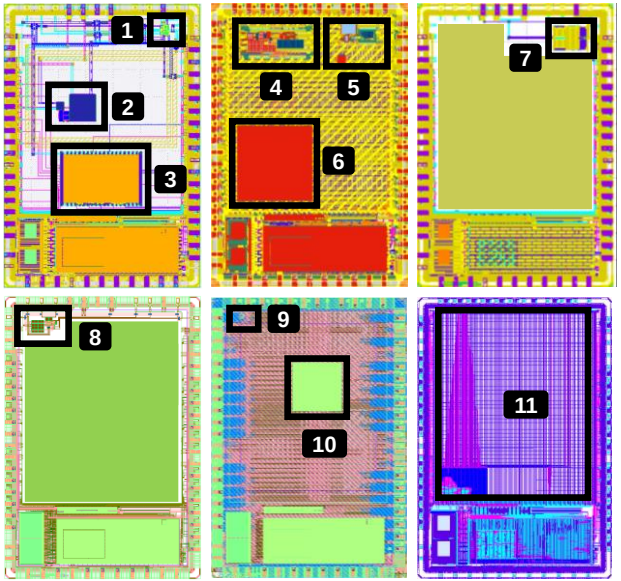


2022 selected teams from 10 countries, 5 continents



June 22, 2022, kick-off meetup with over 100 attendees

2021 Chipathon

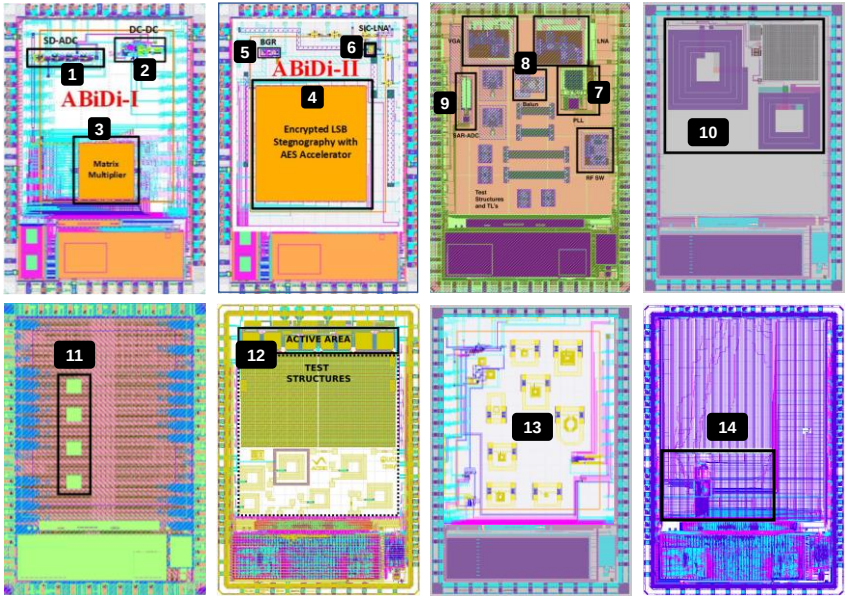


	Function	Team	Chip URL
1	5G bidirectional amplifier	Pakistan3 (FAST National University)	https://efabless.com/projects/560
2	Wireless power transfer unit	Pakistan2 (FAST National University)	
3	Variable precision fused multiply-add unit	Pakistan1 (FAST National University)	
4	Oscillator-based LVDT readout	India2 (Anna University)	https://efabless.com/projects/474
5	Temperature sensor	India1 (Anna University)	
6	GPS baseband engine	India3 (Anna University)	
7	Ultra-low-power analog front-end for bio signals	Brazil2 (U. Federal de Santa Catarina)	https://efabless.com/projects/476
8	TIA for quantum photonics interface	USA4 (University of Virginia)	https://efabless.com/projects/470
9	Bandgap reference	Egypt (Cairo University)	https://efabless.com/projects/473
10	Neural network for sleep apnea detection	USA2 (University of Missouri)	
11	SONAR processing unit	Chile (University of the Bio-Bio)	https://efabless.com/projects/540

- Paid runs via Efabless chipIgnite (130 nm SkyWater)
- All designs are open source

Magazine article: "SSCS PICO Contestants Cross the Finish Line," https://ieeexplore.ieee.org/document/9694491

2022 Chipathon

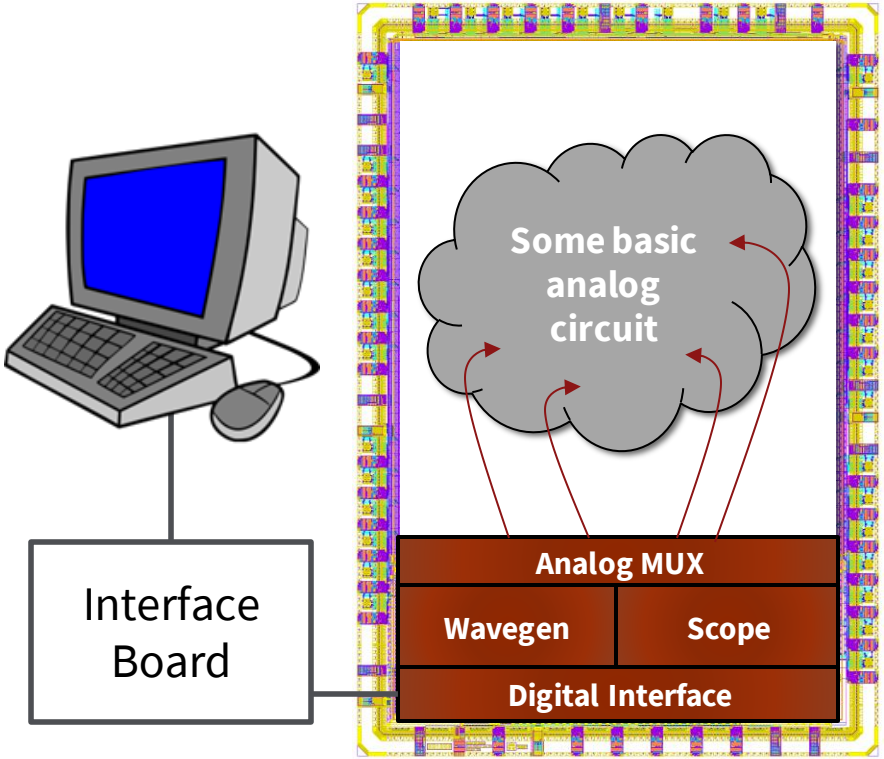


	Function	Team	Chip URL
1	Spatial Sigma-Delta ADC	Pakistan1 (FAST National University)	https://platform.efabless.com/projects/1486
2	On-Chip DCDC Converter with Fast Transient Response	Pakistan4 (FAST National University)	
3	Matrix Multiplier for AI at the Edge	Pakistan7 (FAST National University)	
4	Encrypted LSB Steganography with AES Accelerator	Pakistan2 (FAST National University)	https://platform.efabless.com/projects/1443
5	CMOS Bandgap Reference	Pakistan3 (FAST National University)	
6	Self-Interference Cancellation LNA	Pakistan4 (FAST National University)	
7	Sub-Sampling PLL for SerDes Applications	Austria (Johannes Kepler Univ., Linz)	https://platform.efabless.com/projects/1431
8	60 GHz Demonstrator Chip	Brazil (University of São Paulo)	
9	Low-Power 10-bit SAR ADC	USA1 (University of Alabama & MIT Lincoln Lab)	
10	Boost Converter for Battery-Powered IoT Applications	Greece (Aristotle University of Thessaloniki)	https://platform.efabless.com/projects/1457
11	Radiation-Hardened ALU	USA2 (North Carolina A&T State University)	https://platform.efabless.com/projects/1593
12	DC-DC Buck Converter for CubeSat	Chile[1]/Argentina[2]/Uruguay[3] [1]Universidad Técnica Fed. Santa María [2]Universidad Nacional del Sur & Instituto Nacional de Tecnología Industrial [3]Universidad Católica	https://platform.efabless.com/projects/1427
13	Electrochemical Water Quality Monitoring	USA5 (University of Tennessee)	https://platform.efabless.com/projects/1469
14	Mix-Pix - A Mixed-Signal Circuit for Smart Imaging	Chile (Universidad del Bío-Bío)	https://platform.efabless.com/projects/1494

Magazine article: “Meet the SSCS PICO Chipathletes,” https://ieeexplore.ieee.org/document/9950763

2023 Chipathon (Ongoing)

- Build on-chip waveform generator and “oscilloscope” macros
  - Collection of generally useful IP blocks
- Enable testing of low frequency analog circuits using only a PC
- Tape out first prototypes and improve with community over time



Looking for More Volunteers!

- Possible tasks
  - Evaluate submissions and milestone reports
  - Attend weekly online meet-ups (~June-November)
  - Give a short “how to” presentation during online meetup
  - Provide technical guidance during meet-ups and via Chipathon Slack channel
  - Prepare online tutorials, webinars, chapter talks
  - Help with open-source tool & utility development
- Minimum time commitment of 1-2 hours per week
- Sign up at https://sscs.ieee.org/volunteer-opportunities#SSCD
  - Or send an email to bmurmann@ieee.org

Summary

- There is enormous excitement about collaborative, open-source IC design
  - It will likely change the way we teach & work
  - Fast growing community of ~5000 enthusiasts
- SSCS & CAS Program for Integrated Circuit Outreach (PICO)
  - Engage with broader open-source community and contribute
  - Code-a-chip travel grants, Chipathon, …
  - Volunteering & mentoring opportunities
- Let's all work together to add a new fun factor to IC design!