Reliability and Yield of MOS Devices and Circuits

Prof Gilson Wirth

UFRGS - Porto Alegre, Brazil
Issues in Nano-Scale Technologies

Electrical Behavior / Parameter Variation

Spatial
- Random: RDF, LER, etc
- Systematic: Process Gradients, etc

Temporal
- Aging: NBTI, HCI, Electrom., etc
- Transient: SET/SEU, Noise, etc

There are also environmental sources of variation:
Voltage, Temperature, etc.
Issues in Nano-Scale Technologies

- Average Speed
- Transient Error
- Minimum Acceptable Performance
- Permanent Failure

Performance vs. Time graph
Issues in Nano-Scale Technologies

- Variability
- Transient Error
- Permanent Failure

Minimum Acceptable Speed
Sources & Types of Variations

<table>
<thead>
<tr>
<th>Process</th>
<th>Environment</th>
<th>Temporal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global or Correlated</td>
<td>Operating temperature range, VDD range</td>
<td>&lt;NBTI&gt; and &lt;HCI&gt;</td>
</tr>
<tr>
<td>&lt;Lg&gt; and &lt;W&gt;, &lt;layer thicknesses&gt;, &lt;R&gt;’s, &lt;doping&gt;, &lt;tox&gt;, &lt;Vbody&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Line Edge Roughness (LER), Discrete doping, Discrete oxide thickness, R and Vbody distributions</td>
<td>Self-heating, Hot spots, IR drops</td>
<td>Distribution of NBTI, HCI, Noise, Radiation Eff. (SET/SEU), Oxide breakdown currents</td>
</tr>
</tbody>
</table>
## Sources & Types of Variations

<table>
<thead>
<tr>
<th>Global or Correlated</th>
<th>Process</th>
<th>Environment</th>
<th>Temporal</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$&lt;L_g&gt;$ and $&lt;W&gt;$, $&lt;\text{layer thicknesses}&gt;$, $&lt;R&gt;$’s, $&lt;\text{doping}&gt;$, $&lt;\text{tox}&gt;$, $&lt;V_{\text{body}}&gt;$.</td>
<td>Operating temperature range, VDD range</td>
<td>$&lt;\text{NBTI}&gt;$ and $&lt;\text{HCI}&gt;$.</td>
</tr>
<tr>
<td>Local or Random</td>
<td>Line Edge Roughness (LER), Discrete doping, Discrete oxide thickness, R and Vbody distributions</td>
<td>Self-heating, Hot spots, IR drops</td>
<td>Distribution of NBTI, HCI, Noise, Radiation Eff. (SET/SEU), Oxide breakdown currents</td>
</tr>
</tbody>
</table>

---

6  Gilson Wirth
Different Types of Process Variation

Total Parameter Variation

Systematic
- Layout and Neighborhood Dependent
- Systematic Across Chip

Random
- Intra-Die
- Inter-Die
- Short range Mismatch
- Random Across Chip

After Saxena et al, IEEE-TED 2008
Random Variations

250 180 130 90 65 45 nm

Defect limited yield
Parametric limited yield

σ / μ ≈ (Area)^{-0.5}

hard fails, screenable
soft fails, sensitive to Temp / Vdd / f, difficult to screen
Systematic x Random

130 nm: Systematic

90 nm: More Random

Ring Oscillator Freq Variability
Neuberger, Wirth el al. ESSCIRC 2006.
Systematic Variations

Example of Layout Dependent Systematic Variations: CMP affects dense areas of lines differently than sparsely populated areas of lines.

Design Measure: Regularity and Dummies also in Digital Circuits
Random Process Variations

RDF: Random Dopant Fluctuations
LER: Line Edge Roughness
RDF: Random Dopant Fluctuations

In the past all transistors were similar because of self averaging

Today, Each Transistor is Different

Courtesy Dragica Vasileska
LER: Line Edge Roughness

\[ \sigma_{\text{tot}}^2 = \sigma_{\text{dose}}^2 + \sigma_{\text{pos}}^2 + \sigma_{\text{chem}}^2 \]

45 nm lines/90 nm pitch

Dopants

Substrate
LER: Line Edge Roughness

- Litho Sources of LER:
  - Fluctuations in the total dose due to finite number of quanta
  - Shot noise
  - Fluctuations in the photon absorption positions
  - Nanoscale non-uniformities in the resist composition

- With decreasing feature size, a larger percentage of Lpoly has LER randomness
  - Impact delay and leakage power

Adapted from: D. Frank, VLSI Tech 99
Parameters become Random Variables

[Source: S. Y. Borkar, Intel, 2004]
Power x Timing

Probability

$V_t$

Good chips

Too leaky

Too slow
Aging

NBTI: Negative Bias Temperature Instability
Shifting of PMOS $V_t$ over time, reducing On Current

HCl: Hot Carrier Injection
  Shifting on NMOS $V_t$ over time, reducing On Current

TDDB: Time Dependent Dielectric Breakdown
  Gate Dielectric Breakdown (Gate Leakage Current)

Electromigration
  Increase of Interconnect Resistance (or Rupture)
Collaboration with

Ben Kaczer
Philippe Roussel
Guido Groeseneken
Wear out Mechanisms lead to Aging

- Many failure mechanisms have been shown to be progressive

- Hot carrier injection (HCl)

- Electromigration (EM)

- Negative Bias Temperature Inversion (NBTI)

- Oxide Breakdown (TDDB)

Source: J. Blome
HCl: Hot Carrier Stress

Hot carrier stress generates additional trap states near to the drain:

- Locally shifts $V_{T}$ at the drain side.
- Is also a source of noise.

Noise relevance of traps

Source: R Brederlow, PhD Thesis
NBTI: Negative Bias Temp Instability

- $V_T$ increases over time.
- $I_{ds}$ reduces.

G Wirth et al, IEEE TED 2011
NBTI: Negative Bias Temp Instability

After Bias is removed, Relaxation takes place

Kaczer et al., IEEE-TED 2009
NBTI: Charge Trapping?

Figure 7: Recovery of $V_{TP}$ shifts for several SRAM-sized devices showing the discrete nature of detrapping events. The inset shows that there are no intermediary values between steps in spite of the small measurement step time (shaded area represents the measurement uncertainty (+/- 3σ)).

Huard et al., IRPS 2008
NBTI: Charge Trapping?

Transistor Off

Traps Mostly Empty

Transistor On

Traps Mostly Occupied

After a “Long” Time

$E_F$

$E_F$
BTI x RTS

$V_G$ Positive: PBTI
$V_G$ Negative: NBTI
Model for the Charge Trapping Component

\[ \langle n(t) \rangle \sim \varphi(T, E_F)(A + B \log t) \]

G Wirth et al, IEEE TED 2011
Circuit Activity Dependent

\[ \Delta V_T \ [\text{a.u.}] \]

\[ \text{Duty Cycle} \]
Design Centering Over Product Lifetime

Fig. 2. The impact of $W_p$ (for a fixed $W_n$) on delay varying over time.

HCI and NBTI

• Note that these effects are also history dependent, varying according to total time spent in the 'on' or 'off' state.

• Associated with the average threshold shift, there are also random shifts.

• Even for identical use conditions and devices, there are mismatch shifts due to random variations in the number and spatial distribution of the charges/interface states formed.

• Small gate area devices will experience more random mismatch.
Electromigration

- Particularly likely to affect the thin tightly spaced interconnect lines of deep-submicrometer design.
- Difficult to be prevented by product testing.
- Main cause: generation of stress in the grain boundaries and interfaces.

Common Failure Modes: Grain Boundaries and Interfaces.


Fig. 7. Possible failure modes in CoWP-coated interconnects [14].
Transient Faults

RTS: Random Telegraph Signal

Radiation Effects:
   SET: Single Event Transient
   SEU: Single Event Upset

Signal Integrity Issues (e.g., Noise Coupling, Substrate Noise Coupling, etc).
Transient Faults

**RTS: Random Telegraph Signal**

Radiation Effects:
- SET: Single Event Transient
- SEU: Single Event Upset

Signal Integrity Issues (e.g., Noise Coupling, Substrate Noise Coupling, etc).
Collaboration with

Ralf Brederlow
Roland Thewes

Ralf Brederlow
Purushothaman Srinivasan (SP)
John Krick

Dragica Vasileska
RTS: Random Telegraph Signal

![Diagram of a metal-oxide-semiconductor (MOS) device with labels for $V = V_{GS}$ (gate source), SiO$_2$ (oxide), traps, emission, capture, charge carriers, $V = 0$, and $V = V_{DS}$ (drain source).]
RTS: Random Telegraph Signal

Leads to modulation of the local **mobility** and **number of free carriers** in the channel.
RTS: Random Telegraph Signal

![Graph showing RTS behavior](graph.png)
Evaluating the Noise Power due to One Trap

• Poisson Process

\[ p(0 \to 1)dt = \frac{dt}{\tau_c} \quad \text{(capture)} \]

\[ p(1 \to 0)dt = \frac{dt}{\tau_e} \quad \text{(emission)} \]

average time in state 1 = \( \langle t \rangle_1 = \tau_c = \frac{1}{\tau_c} \int_0^\infty t \exp(-t/\tau_c)dt \)

average time in state 0 = \( \langle t \rangle_0 = \tau_e = \frac{1}{\tau_e} \int_0^\infty t \exp(-t/\tau_e)dt \)
Evaluating the Noise Power due to One Trap

• We calculate the time autocorrelation

\[ A(t) = \langle \sigma_0 \sigma_t \rangle \]

\[ = \sum_{\sigma_i \sigma_j \in \{0,1\}} \sigma_i \sigma_j \Pr(\sigma_t = \sigma_j | \sigma_0 = \sigma_i) \Pr(\sigma_0 = \sigma_i) \]

\[ = \underbrace{\Pr(\sigma_t = 1 | \sigma_s = 1)}_{p_{11}(t)} \underbrace{\Pr(\sigma_0 = 1)}_{\langle t \rangle_1} \]

\[ = \frac{\langle t \rangle_1}{\langle t \rangle_0 + \langle t \rangle_1} = \frac{\tau_c}{\tau_c + \tau_e} \]
Evaluating the Noise Power due to One Trap

• The autocorrelation is given by

\[ A(t) = \frac{\tau_e \tau_c}{(\tau_c + \tau_e)^2} + \left( \frac{\tau_c}{\tau_c + \tau_e} \right)^2 \exp \left[ -\left( \frac{1}{\tau_e} + \frac{1}{\tau_c} \right) t \right] \]

• And the power spectrum density (Fourier Transform) is a Lorentzian

\[ S(\omega) = \frac{\delta^2}{(\tau_c + \tau_e)} \left( \frac{1}{\tau_c} + \frac{1}{\tau_e} \right)^2 + \omega^2 \]

+ Singular term

It is not important
RTS: Random Telegraph Signal

![Graph showing RTS signal with labeled time constants \( \tau_e \) and \( \tau_c \).]
Evaluating the Noise Power due to Many Traps

- Superposition of Lorentzians

\[ S(f, \omega_1, ..., \omega_{N_{tr}}, A_1, ..., A_{N_{tr}}) = \sum_{i=1}^{N_{tr}} S_i(\omega) = \sum_{i=1}^{N_{tr}} A_i^2 \frac{1}{\omega_i} \frac{1}{1 + \left(\frac{\omega}{\omega_i}\right)^2} \]

- Averaging on many variability sources

\[ \langle S \rangle = \ln^{-1}\left(\frac{\omega_{\text{max}}}{\omega_{\text{min}}}\right) \sum_{N_{tr}=0}^{\infty} \frac{N^{N_{tr}}}{N_{tr}!} e^{-N} \sum_{i=1}^{N_{tr}} \langle A_i^2 \rangle \int_{\omega_{\text{min}}}^{\omega_{\text{max}}} \frac{1}{\omega_i^2} \frac{1}{1 + \left(\frac{\omega}{\omega_i}\right)^2} df_i \]

\[ p(\tau_i) \propto \tau_i^{-1} \]

\[ p(\omega_i) = \ln^{-1}\left(\frac{\omega_{\text{max}}}{\omega_{\text{min}}}\right) \omega_i^{-1} \]
Evaluating the Noise Power due to Many Traps

- **Average Value**

\[
\langle S (f) \rangle = \frac{\langle A^2 \rangle N_{\text{dec}} \text{ WL}}{f} \frac{\pi}{2}
\]

- **Standard Deviation**

\[
\frac{\sigma S(f)}{\langle S (f) \rangle} = \frac{\sqrt{2}}{\pi} \sqrt{N_{\text{dec}} \text{ WL}} \sqrt{\frac{\langle A^4 \rangle}{\langle A^2 \rangle^2}}
\]
Evaluating the Noise Power due to Many Traps

\[
S(f) = \sum_{i=1}^{N_{tr}} A_i^2 \frac{1}{f_i} \frac{1}{1 + \left(\frac{f}{f_i}\right)^2}
\]
Average Noise

\[ < S(f) > = \frac{< A^2 > N_{\text{dec}} \cdot WL}{f} \cdot \frac{\pi}{2} \]

1/f noise

Thermal noise
Noise of Large Area Device: 1/f

C11n  W=10um  L=10um
Vg=0.85  Vd=1.30

Drainrauschstrom/Hz^-2

Frequenz (Hz)
Noise of Small Area Device: Lorentzian

C11n 0,16x0,12 Vg=0.85, Vd=1.0

Frequenz (Hz)
Rauschstrom / Hz^-2
Average Value and Variability

\[ \text{Gate referred voltage noise} \]

\[ [\text{VHz}^{-1/2}] \]

- n-MOS, \( W / L = 25\mu\text{m} / 0.25\mu\text{m} \)
- \( V_d = 1.0\text{V}, \ V_{g,\text{eff}} = 0.5\text{V} \)
Average Value and Variability

n-MOS, W / L = 2.5µm / 0.25µm

\[ V_d = 1.0V, \ V_{g,\text{eff}} = 0.5V \]
Average Value and Variability

n-MOS, $W/L = 0.25\mu m / 0.25\mu m$

$V_d = 1.0V$, $V_{g,\text{eff}} = 0.5V$
Noise Scaling

Noise corner frequency [Hz]

Technology node [nm]

Data based on ITRS 2004
valid for minimum sized devices

device operating in saturation, $V_{\text{geff}} \sim 250\,\text{mV}$

M. Fadlallah et al.
Variability Scaling

Triangles: Measurement
Dots: Monte Carlo Simulation
Line: Model

G Wirth et al. IEEE Trans Electron Dev, 2005
Switched Bias: Modulation Theory

we can expect for 50% duty cycle, as the switching operation can be represented as a multiplication of the $1/f$ noise current with a square-wave signal with 50% duty cycle, $m(t)$, as follows:

$$m(t) = \frac{1}{2} + \frac{2}{\pi} \sin \omega_{sw} t + \frac{2}{3\pi} \sin 3\omega_{sw} t + \frac{2}{5\pi} \sin 5\omega_{sw} t + \cdots .$$

(1)

In the frequency domain this corresponds to a convolution of the PSD of the $1/f$ noise with a spectrum with delta functions at dc, $\omega_{sw}$, $3\omega_{sw}$, $5\omega_{sw}$, etc. The dc-term determines the resulting noise power in baseband, which is $(1/2)^2$ (or $-6$ dB) compared to the original $1/f$ noise power.

Klumperink et al., IEEE J. SOLID-STATE CIRC, VOL. 35, NO. 7, 2000
Statistical Model for MOSFET Low-Frequency Noise under Cyclo-Stationary Conditions

Gilson Wirth\(^1\), Roberto da Silva\(^2\), Purushothaman Srinivasan\(^3\), John Krick\(^3\) and Ralf Brederlow\(^4\)

\(^1\)Electrical Engineering, \(^2\)Informatics Institute
\(^1,2\)UFRGS, Porto Alegre, Brazil, \(^1\)Email: wirth@inf.ufrgs.br
\(^3,4\)Texas Instruments, \(^3\)Dallas, US, \(^4\)Freising, Germany
Outline

• Analytical Model for Cyclostationary Noise
  – Mean Value
  – Standard Deviation

• Experimental Results of Cyclostationary Noise
  – Mean Value
  – Standard Deviation

• Conclusions
Noise Produced by Interface States

• LF-noise of MOSFETs is generated by trap-states at the Si/SiO$_2$ interface which are randomly charged and discharged in time.

• This leads to modulation of both local mobility and number of free carriers in the channel.

• Probability of a trap state to switch its occupation level depends on the energetic position of the local Fermi level.
Trap State and Fermi Level at $V_{gs,\text{on}}$

Gate voltage applied to the device

$V_{gs,\text{on}}$  $V_{gs,\text{off}}$

The Energy difference between the Fermi Level and the Trap Level depend on bias
Trap State and Fermi Level at $V_{gs,off}$

Gate voltage applied to the device

The Energy difference between the Fermi Level and the Trap Level depend on bias
Trap State at Switched Bias Operation

Gate voltage applied to the device

\[ V_{gs,on} \]
\[ V_{gs,off} \]

\[ E_T \]
\[ E_f \]

Gate Oxide Substrate

\( g_t(E) \)
Noise Spectra for a Single Trap under Cyclo-Stationary Excitation

\[
S_i = \frac{\delta^2}{\pi} \cdot \frac{\beta_{eq}}{(1 + \beta_{eq})^2} \cdot \frac{1}{\omega_i} \cdot \frac{1}{1 + (\omega / \omega_i)^2}
\]

where

\[
\beta_{eq} = \frac{<1/\tau_e>}{<1/\tau_c>}, \text{ with } <\bullet> = (1/T) \int_0^T \bullet \, dt
\]

\[
\omega_i = <1/\tau_e> + <1/\tau_c>
\]

For Switching Frequency $\gg \omega_i$
Uniform Trap Density

• No noise reduction was observed in Analytical Analysis and Monte Carlo Simulation.
Parabolic U-shape

\[ g(E_T) = aE_T^2 - a(E_c - E_v)E_t + k \]
Switched Bias: Noise Mean Value Decreases

Noise power as a function of the Fermi level in the off phase

\[ \langle S \rangle \text{[a.u.]} \]

Ev \quad (Ec+Ev)/2 \quad Ec

0.005
0.01
0.015
0.02
0.025

E_{\text{Foff}}
Noise Measurements

- Noise measurement under both DC and cyclo-stationary conditions for constant $V_{DS}$ and various $V_{GS,ON/OFF}$ bias.
- Cyclo-stationary noise frequencies of 1 kHz, 10 kHz and 100 kHz.
- 45 nm Technology
Noise Reduction under Cyclo-Operation

- Modulation theory predicts four times noise reduction for CS operation.
- Noise reduction is larger and in good agreement to the proposed model.
Conclusions

• A microscopic model for LF-noise under cyclo stationary excitation has been introduced.
• It is capable of modeling the average noise behavior and its standard deviation.
• Model is in good agreement to experiment.
• Under cyclo-stationary operation the average noise power decreases but the variability increases.
RTS in **Time Domain**

**V_T Fluctuations**
### Possible Simulation Methodologies

<table>
<thead>
<tr>
<th>Static</th>
<th>Dynamic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Change $dV_t$ at instantiation</td>
<td>Change transistor Model equations</td>
</tr>
</tbody>
</table>

Verilog-A wrapper to Trans. model

$$\Delta V_T$$  

$$\Delta V_T$$

$$\text{Ids} = \ldots + f(d\text{elvto}(t))$$
$V_T$ Fluctuates Over Time

$\Delta V_T(t)$

$V_T$ Fluctuation (V)

Time (s)

2.0x$10^{-7}$

3.0x$10^{-7}$

4.0x$10^{-7}$
Ring Oscillator

\[ V_0 \rightarrow V_1 \rightarrow V_2 \rightarrow V_0 \]
Period Jitter

- Period Jitter is the difference between a clock period and the ideal clock period (it can occur after or before the ideal transition).
Statistical Simulation Results

Minimum: 3.6784E-11
Máximum: 3.8338E-11
Mean: 3.7370E-11
Std Deviation: 2.06329E-13

Distribution is skewed (not Gaussian)
Phase Noise: Upconverted 1/f Noise

Source: Texas Instruments
Vmin on some SRAM arrays varied from one measurement to the next.

Source: M Agostinelli et al. (Intel), IEDM 05
Issues for Test

- Traditional Go-Don’t Go Test (usually intended to screen hard failures, not Adequate
- Burn-In and Iddq Test Challenged by Leakage Currents
- Complex Aging Mechanisms
Transient Faults

RTS: Random Telegraph Signal

Radiation Effects:
  SET: Single Event Transient
  SEU: Single Event Upset

Signal Integrity Issues (e.g., Noise Coupling, Substrate Noise Coupling, etc).
Radiation Effects

Please click on Fig to run movie
Radiation Effects

Charge Collection Mechanism
SET in Combinational Logic

Particle strike
SEU in Sequential Logic

BIT-FLIP

\[ Q_{\text{crit}} \sim C_{\text{node}} V_{\text{node}} + I_{\text{restore}} \tau_{\text{flip}} \]
Sequence of Events from Ionization to Failure

- **Fault latency**
- **Error latency**

1. **Ionization**
2. **Transient current (injected or extracted from the junction)**
3. **Transient voltage pulse (capacitor node)**
4. **Fault**
5. **Fault effect**
6. **Error**
7. **Failure**

- **Fault tolerant techniques**
- **Sensors (detection)**
- **Time redundancy (detection, mitigation)**
- **Hardware redundancy**
- **Error correcting codes (detection and mitigation)**
- **Self-checking mechanisms with recovery**
- **Recomputation (detection and mitigation)**
- **Redundancy / Spare components**

80 Gilson Wirth
Bulk-BICS

Wirth et al., IEEE Micro, 2007

\[ \alpha \text{ particles, protons, heavy ions} \]
Transient Faults

RTS: Random Telegraph Signal

Radiation Effects:
  SET: Single Event Transient
  SEU: Single Event Upset

Signal Integrity Issues (e.g., Noise Coupling, Substrate Noise Coupling, etc).
Signal Integrity

fringing

parallel
Signal Integrity

Noise can be interpreted as logic switching!
Simulation Methodologies

Circuit Level
   Corner Based
   Monte Carlo
   Error Propagation

Logic-Gate Level
   Statistical Static Timing Analysis
Corner Based

Traditional method:

- Design Circuits so as to guarantee functionality at all worst case corners.
- Values of parameters are considered deterministic.
- No probability is taken into consideration.

Problem:

- Makes sense only if sources of variations are strongly correlated (worst case occurs for all parameters).
- Too pessimistic for nano-scale CMOS.
Corner Based

\[ I_D = \frac{K'}{2} \frac{W}{L} \left[ (V_{GS} - V_T) - \frac{V_{DS}}{2} \right] V_{DS} \]

Variation of \( K' \) and \( V_T \) across the commonly modeled process corners. “Hst” and “Lst” are highest and lowest values for \( K' \) and \( V_T \).

<table>
<thead>
<tr>
<th>Corner</th>
<th>( K'_N )</th>
<th>( V_{TN} )</th>
<th>( K'_P )</th>
<th>( V_{TP} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>Hst</td>
<td>Lst</td>
<td>Hst</td>
<td>Lst</td>
</tr>
<tr>
<td>SS</td>
<td>Lst</td>
<td>Hst</td>
<td>Lst</td>
<td>Hst</td>
</tr>
<tr>
<td>SF</td>
<td>Lst</td>
<td>Hst</td>
<td>Hst</td>
<td>Lst</td>
</tr>
<tr>
<td>FS</td>
<td>Hst</td>
<td>Lst</td>
<td>Lst</td>
<td>Hst</td>
</tr>
</tbody>
</table>
Monte Carlo (MC)

- Netlist
- Distribution dVt/dBeta of transistors

Flowchart:
1. Electrical simulation \( h(v_{t1}, b_1, \ldots, v_{tn}, b_n) \)
2. Check if \( i < N \)
3. Increment \( i \)

Complexity:
- Arbitrary \( N \)
  - independent of number of devices \( n \)
  - rule of thumb: 100-100,000
- Error \( \approx \frac{\text{var}(f)}{\sqrt{N}} \)
- Error \( \approx O(\frac{1}{\sqrt{N}}) \)

Compute statistical information
Fit Probability Density Function
Error Propagation (EP)

1. Distribution \( dV_t/d\beta \) of transistors
2. Netlist, Measures
3. Generate data file (points around the average)
4. Set of runs (data file)
5. Electrical Simulations
6. Compute sensitivities (numerically)
7. Compute Error Propagation
8. Mean, Standard Deviate

\[
\begin{align*}
\mu_p & \approx \bar{f} \\
\sigma_p^2 & \approx \sum_{i=1}^{n} \left[ (s_{Vt_i} \sigma_{Vt_i})^2 + (s_{\beta_i} \sigma_{\beta_i})^2 \right]
\end{align*}
\]

Complexity \( n + 1 \)
**EP x MC: FF setup time**

The diagram shows a comparison of sample quantiles against theoretical quantiles. The data points for MC (points), MC (line), and EP (line) are plotted against the theoretical quantiles. The histogram inset provides a visual representation of the data distribution.
EP x MC: FF hold time

Histogram
**EP x MC:** FF clock-to-q delay

![Graph showing FF clock-to-q delay](image)
Static Timing Analysis (STA): Deterministic

No process variability
Nominal (corner) values

<table>
<thead>
<tr>
<th>Load [fF]</th>
<th>1</th>
<th>4</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew [ps]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>0.021</td>
<td>0.037</td>
<td>0.102</td>
</tr>
<tr>
<td>60</td>
<td>0.039</td>
<td>0.055</td>
<td>0.115</td>
</tr>
<tr>
<td>240</td>
<td>0.078</td>
<td>0.117</td>
<td>0.182</td>
</tr>
</tbody>
</table>

Cell Delay

9x1 electrical simulations

240
Statistical Static Timing Analysis (SSTA)

Variability Info

<table>
<thead>
<tr>
<th>Load [fF]</th>
<th>1</th>
<th>4</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew [ps]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>0.021</td>
<td>0.037</td>
<td>0.102</td>
</tr>
<tr>
<td>60</td>
<td>0.039</td>
<td>0.055</td>
<td>0.115</td>
</tr>
<tr>
<td>240</td>
<td>0.078</td>
<td>0.117</td>
<td>0.182</td>
</tr>
</tbody>
</table>

Cell Delay

Library Characterization

- Load (fF): 1, 4, 16
- Slew (ps): 15, 4, 16
- Values:
  - Load [fF]: 1, 4, 16
  - Slew [ps]: 15, 4, 16
  - Values: 0.021, 0.037, 0.102; 0.039, 0.055, 0.115; 0.078, 0.117, 0.182
Could Variability & Reliability Cost Become a Show Stopper?

High-cost reliability solutions (increased design cost, increased silicon area, etc) and service may lead to unacceptable costs.

Based on T Austin et al., IEEE D&T of Comp., 2008.
Could Variability & Reliab. Cost Become Show Stopper?

Need for New Low-Cost, Resilient Design Methodologies

Based on T Austin et al., IEEE D&T of Comp., 2008.
# HW & SW Techniques for Enhancing Reliability

<table>
<thead>
<tr>
<th>SW</th>
<th>Application</th>
<th>Check-point and Roll Back, Application Replication &amp; SW Voting, Robust Data Structures, Memory Management, etc.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BIOS</td>
<td></td>
</tr>
<tr>
<td>HW</td>
<td>Intercon. &amp; I/O</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Memory</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Logic</td>
<td></td>
</tr>
</tbody>
</table>
Conclusion

- Process parameter variations and variations of parameters over time (both aging and transient) are very important in Nano-scale technologies.
- Tools for automated estimation of yield and reliability are mandatory.
- New design methodologies to assure yield and reliability are required.
- New test methodologies to cope with parametric and transient failures needed.
- It is needed to simultaneously address power, speed and reliability constraints.
- Proper process eng., modeling, simulation and design can lead to high yield and reliability.