System Co-design and optimization for high performance and low power SoC’s

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Agenda

• What is Co-Design
• Why Co-Design
• Co-Design Flow
• Practical Case Studies
• Summary
What is System Co-Design?

• System Co-Design is the process of designing die, package and board in conjunction for meeting all the design and system goals in an optimal manner

• Complexity introduced due to scaling and miniaturization trends have brought a need for a systematic co-design
  – Increasing interference of package electrical behavior at higher frequencies
  – Higher routing density and miniaturization trends driving routes getting closer and closer
  – System level Packaging & associated challenges
What is System Co-Design?

SoC Design → Package Design → PCB Design → End Product

PAST

Co-Design

SoC Design

Package Design

PCB Design

End Product

CURRENT
Why System Co-Design?

- **Performance**
  - Signal Integrity of Critical nets with ever increasing interface speeds
  - Power Integrity with reduced voltage margins at all interface levels of Die, Package, PCB

- **Cost**
  - Co-Design helps with clear idea and quantification of various factors impacting cost
  - Helps not only reduce SoC cost but optimize system cost too
  - Trade off analysis vs. system considerations; some of the board solutions are very expensive like thermal management

- **DFM/DFY**
  - Maintain better manufacturing through validated and tested design approaches
  - Better yield/manufacturing practices vs. electrical impact
Co-Design Flow

Co-design

Electrical
- Die Model
- Package Model
- Board Model
- Power Integrity
- Signal Integrity

Physical
- IO/Bump planning
- Pkg Design
- Board Design

Others
- Thermal Analysis
- Reliability Analysis
Factors affecting minimum bump pitch –

- There are limitations on minimum bump pitch from bumping process that can be manufactured.
- In package minimum bump pitch that can be achieved depends on the via pad size and line width/spacing used for escape routing.

- Signal escapes are assumed to be on layer2 -
  - Via pad diameter = 90um
  - Line width/spacing = 15um
  - Bump pitch = ((number of escape routes) * Line width) + ((number of escape routes+ 1) * line space) + via pad size
Co-Design : Die Planning Case Study

- Option 1: Higher column pitch
  - Standard Row-Row pitch
  - Effective signal pitch = high

- Option 2: Medium column pitch
  - Standard Row-Row pitch
  - Effective signal pitch = medium

- Option 3: Lower column pitch
  - Standard Row-Row pitch
  - Effective signal pitch = low

Bump placement / Assignment can significantly impact the effective signal pitch using same packaging rules – Enables more IO placement in a given periphery

Which is the best option?
Co-Design : Power Integrity

Dynamic IR Plot without Package

Dynamic IR Plot with Distributed Package Model

Notice how the hot spots change with the detailed package model
Co-Design : Power Integrity

2-2-2 stack up provides better PDN impedance by just optimizing # VIA’s
Reduced substrate cost by using 2-2-2 stack up

Blue  – 3-2-3 stack up
Red   – 2-2-2 stack up
Green – 2-2-2 stack up
Co-Design : Package Decap Planning

• Useful for maintaining Power integrity
• More effective than board decaps at higher frequencies, especially if low inductance IDC’s are used
• Can eliminate some board decaps which helps board design

**Case1:** Baseline without any package decaps

**Case2:** 60 decaps (20x0.1uF, 20x0.01uF, 20x560pF) removed from baseline board
4x2.2uF, ESL=100pH
Murata LLA decaps added to package

<table>
<thead>
<tr>
<th>Case</th>
<th>Peak Voltage Swing (mV)</th>
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<tbody>
<tr>
<td>Case 1 (Baseline)</td>
<td>38 mV</td>
</tr>
<tr>
<td>Case 2 (Baseline minus 60 board decaps plus 4 package decaps)</td>
<td>27 mV</td>
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Co-Design: Die / Package / Board

- **SOC**
  - VDD/VSS Pad-Frame Resist. Per pin
  - Decoupling ESR
  - WC Signal
  - Decoupling Per pin
  - SOC VSS and Substrate Network Model

- **Driver**
  - PVT + Load + Slew Control assumptions
  - Pad-Frame Model
  - Wc Crosstalk Signal

- **Package Model**
  - RLC
  - Or, S-para

- **PCB Model**
  - Range: Line Length & $Z_0$
  - PCB Supply Model

- **Receiver**
  - PVT Spice Model + IBIS

- **SOC VSS and Substrate Network Model**
  - Ensure Pin “Waveform Spec” Compliance (e.g. JEDEC)
  - Margins and Timing De-Rating Assumptions

- **Memory/other**
  - Ensure Functional Compliance Of Rx signal
  - Load Model
Co-Design: Die / Package / Board

Full System level view is required to arrive at the optimal settings on the Tx and the Rx.
Co-Design: Analysis Completeness

Conventional Clocking

DDR Read Clocking
Co-Design : Analysis Completeness

Choice of Switching pattern is very important to model all SI effects
Co-Design : Package Thermal

- Impact of Thermal Balls (CSP)
  - Includes solid Cu land under die
  - Thermal vias to 1st buried plane
    - thermal via modeled as Cu column
    - Cu column area is the equivalent area of 1oz. Cu plated in a 0.3mm diameter hole
Co-Design : Package Variations

- Variation exists due to manufacturing tolerances
- Electrical impact more prominent due to tighter densities – cannot ignore
- No systematic approach, methodology exists in most EDA tools
Summary

• System Co-Design is an emerging field and is a multi disciplinary function. Overlap Die, Package, Board analysis requirements.

• System Co-Design is not an option – it is a MUST for optimizing performance, cost and yield with the current design trends

• Innovations in Packaging are going to drive the future devices. Co-Design is going to be a key enabler
Acknowledgements:

TI India Processor Co-Design Team
TI Dallas Processor Co-Design Team