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Multi-source phonocardiography for the home prevention of heart failure

Ms. Noemi Giordano, PhD Candidate, DET.

Auscultation is a traditional routine screening tool in the clinical practice for cardiovascular diseases, the first world cause of death according to the World Health Organization. Phonocardiography is its digital counterpart and is growing in importance because it allows, for example, for the assessment of the electromechanical coupling of the heart. A delay in the closure of heart valves, which originates heart sounds, with respect to the ventricular depolarization in the simultaneous electrocardiogram was found to correlate with heart failure. This talk will explore how the design of a noninvasive device for the recording of phonocardiographic (PCG) and electrocardiographic (ECG) signals can help in the prevention of acute episodes of heart failure. The issues regarding the positioning of the digital stethoscope, limiting its applicability in a real-life homecare context, will be investigated along with the potentiality of multi-source phonocardiography as a possible solution.

Relaxation DAC: a new-in-concept interface for the Internet-of-Things

Mr. Roberto Rubino, PhD Candidate, DET.

Technology scaling has been leading the market of integrated circuits (IC) production of the last decades, to get aster and more efficient digital circuits. Meanwhile, transistor variability has increased the challenges in the design of analog blocks, especially where low area and low power embedded systems are required. This is the case for the Internet of Things (IoT) sensor nodes, where analog interfaces are needed as acting, sensing and communicating blocks in systems which need little to no maintenance, possibly harvesting energy from the environment. The strategy to re-think analog interfaces to be intrinsically mostly-digital, matching-insensitive and able to work at very low supply voltages is proving to be a promising solution. The new-in-concept Relaxation Digital-to-Analog converter (ReDAC) which is going to be presented in the talk, is targeting all these challenges as an ultra low power, bitstream based, easily scalable converter.

Logic-in-Memory computing: an architectural solution to solve the von Neumann bottleneck

Mr. Andrea Coluccio, PhD Candidate, DET.

Nowadays, computer architectures are widely studied in the literature. The von Neumann scheme, which is essentially composed of CPU and memory, is the most adopted structure. Both elements have made significant improvements in terms of performance: CPUs are becoming faster and more efficient over the years, achieving high clock frequencies and multitasking capabilities. However, memory cannot follow the trend of the CPU in terms of computational speed, so the communication between these two elements represents a bottleneck: a lot of power, energy, and execution time are wasted only to wait for the data from memory. This phenomenon is called the von Neumann bottleneck. What could we do to reduce this drawback? Logic-in-Memory (LiM) could be a solution: it merges storage and computation, so instead of moving data back and forth in the memory hierarchy, calculations are performed directly inside the memory array, reducing the data traffic and improving the performance.

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