High-Density 3D Power Packaging with Heterogeneous Passive-Active Integration

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Heterogeneous Integration with Nanopackaging

• Power delivery in computing systems
  • Integrated voltage regulator
  • Capacitors and Inductors

• Medium-power packaging
  • Embedded-die packaging with die-attach materials
  • High-temperature organic packaging

• High-Power packaging:
  • Doubleside cooling
  • High-voltage passives
3D Heterogeneous Package Integration

Pre-packaged and molded devices

Large power components and RF interfaces

2D Surface assembly

Traditional PCB processes

2.5D or 3D integration: logic-memory, transceiver-Antenna, High-bandwidth interconnects with interposers and fan-out packages Passive integration with actives Integrated EMI, heat-spreaders, encapsulation
Power Delivery for Processors

IPECs may be partitioned and integrated in multiple ways, each potentially serving different parts of hybrid topologies.

**Inside SiP**
- **Focus of this presentation**
- **Outside SiP**
  - **A parallel initiative**

### A) In load (IP, HBM, PIC)
- Monolithic integration
- Hybrid bonding

### B) In interposer
- On top side
- Integrated in active interposer
- Embedded in organic interposer

### C) In substrate
- On top side
- On land side

**IEEE HIR TWG, Power Electronics**
How to Partition the Power Components Around the Load?

Apple iPhone 8 Application Processor/Memory in Fanout (Info) Package

- 13.9 x 14.8 mm InFO PoP Package
  - 8% smaller than A10
  - 790μm package height
- Memory package with SxS die
  - Die Thickness: 140μm
  - 140μm EMC thickness over die
  - 3L substrate; 90μm thick
  - Underfill between packages
- Processor: ~10 x 8.7mm
  - 30% smaller than A10
  - 150μm thick, 15μm “top coat”
  - 50μm thick, four-metal-layer RDL

1 A11 Die
2 RDL
3 Vertical Connection
4 Memory
5 Capacitor
**Medical Device Application**

**System Description**

- **Neural recording system:**
  - Piezomagnetic antenna to turn on the diode

- **Neural stimulation system**
  - Piezomagnetic power telemetry to charge the storage capacitor

- **Biophotonic system**
  - Piezomagnetic power and data telemetry to power the photonics, drivers and RF interface
Power Telemetry – Wearable and Implantable

**Two-Coil Inductive Link**
- Receiving coil should be large enough
  - $0.1 - 1 \text{ mW/mm}^2$
- Efficiency can be increased with larger separation distance
  - $1 - 5 \text{ mW/mm}^2$

**Multiple-Coil Inductive Link**
- Efficiency can be increased with larger separation distance
  - $1 - 5 \text{ mW/mm}^2$

**Piezoelectric power telemetry**
- Receiving link can be reduced to $< 1 \text{ mm}$
  - $0.1 - 1 \text{ mW/mm}^3$

**Piezo-magnetostrictive power**
- Higher power density can be achieved with smaller sub-mm receivers
  - $1 - 20 \text{ mW/mm}^3$

---

**Inductive link**

**Piezo-magneto**

Device assembly

*Bioelectronics on the front side*
- Metglas®/PvDF/Metglas® Stack on the backside

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![Graph](chart.png)

- **Active Range (mm)**
- **Efficiency (%)**

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<thead>
<tr>
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<tbody>
<tr>
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</tbody>
</table>
Nanopackaging Drives Future Hardware

- **Power**: Nanocapcitators and inductors
- **Thermal**: Cu-Graphene heat-spreaders
- **Reliability**: ALD Inorganic films
  - Humidity barriers
- **RF**: Nanodielectrics and additive interconnects for 5G and wireless sensors

**Multimodal Sensing**

**Broadband Wireless Communication**

**Bioelectronics**

- Electrodes
- Power and data telemetry
- Storage capacitors
- Remateable connectors

https://ieeenano.org/nanopackaging-tc
Power Delivery

Minimize the stages of power conversion;

Perform power conversion right near the load;

Utilize Advances in:
- GaN
- CMOS integration
- Topologies
- Passive components

Figures from EPC (Alex Lidow) and IBM Zurich (Arvind Sridhar)
Role of PMIC in Power Delivery

Enabled by advances in magnetics

Higher freq DC/DC

Integrated PMIC

(Adapted from Indumuni Ranmuthu, PwrSOC 2016 [1])

High-frequency power MOSFETS

Advanced Topologies

High-density integrated passives
## R&D Needs

<table>
<thead>
<tr>
<th>Capacitors</th>
<th>Density</th>
<th>High K dielectrics; Enhance electrode surface area; New dielectrics and deposition processes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Frequency stability</td>
<td>Electrodes and connectivity with lower parasitics</td>
</tr>
<tr>
<td></td>
<td>Integration</td>
<td>Thinner form-factors; Substrate or wafer or fan-out embedding</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Inductors</th>
<th>Density</th>
<th>Higher permeability with saturation field and high resistivity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Efficiency</td>
<td>Low coil DC losses; Low core losses with low coercivity and eddy currents</td>
</tr>
<tr>
<td></td>
<td>Integration</td>
<td>Substrate- or wafer-compatible process</td>
</tr>
<tr>
<td></td>
<td>Current-handling</td>
<td>Design innovations; Scalability in thickness to handle higher current</td>
</tr>
</tbody>
</table>
**Embedded Capacitors Roadmap**

- **Embedded polymer laminate and dielectrics**
  - 2000:
    - 0.1 nF/mm² Polymer laminate dielectrics
  - 2008:
    - 0.5 nF/mm² Polymer film dielectrics
  - 2016:
    - 2-3 nF/mm² Thin oxides
  - 2020:
    - 20-30 nF/mm² BaTiO₃ film
  - 2025:
    - 30-50 nF/mm² enabled by new multicomponent oxides

- **Embedded ceramic film**
  - 0.08 µF/mm² Silicon capacitors Deep trench
  - 0.25 µF/mm² 0.5 µF/mm²
  - 20-30 nF/mm² BaTiO₃ film

- **Wafer-integrated capacitors**
  - Board or package embedding; I/O decoupling; 100 MHz
  - Core and I/O decoupling; 100-500 MHz

- **Embedded capacitors Panel**
  - Multilayered dielectrics on deep trench
  - IVR; Embedded PoL 1-20 MHz
  - Adv. Nanotech. >3 µF/mm²
Deep Trench Land-Side Inserted Si Capacitors (TSMC)

*Land-side on-Si capacitors for integrated fan-out packaging*

- Up to >500 nF/mm² density
- Superior VCC and TCC
- Comparable ESR to MLCCs
- Thickness as low as 100 µm

<table>
<thead>
<tr>
<th>Density, nF/mm²</th>
<th>Breakdown Voltage, V</th>
<th>TDDB, V</th>
<th>Max Voltage rating, V</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>16.1</td>
<td>7.0</td>
<td>4.5</td>
</tr>
<tr>
<td>250</td>
<td>14.3</td>
<td>6.8</td>
<td>4.2</td>
</tr>
<tr>
<td>500</td>
<td>6.5</td>
<td>4.5</td>
<td>3.2</td>
</tr>
<tr>
<td>600-700</td>
<td>4.0</td>
<td>3.8</td>
<td>2.5-1.2</td>
</tr>
</tbody>
</table>

1 × 0.5 mm footprint
Located underneath info-POP supported by extra PCB layer
High-Density Capacitors for Integrated Voltage Regulators

Objectives

- Ultra-high density capacitors:
  - >1 μF/mm² at 1 MHz, 3-48 V, & 50 mΩ ESR
  - 1 nA/μF leakage current
  - Simpler processing on wafer or package
  - 100 μm thickness
  - >105°C stability

Prior Art

<table>
<thead>
<tr>
<th>MLCC</th>
<th>Trench Caps</th>
<th>Ta Chip</th>
<th>Emerging Need</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volumetric Density</td>
<td>20 μF/mm³</td>
<td>1 μF/mm³</td>
<td>~10 μF/mm³</td>
</tr>
<tr>
<td>Thickness</td>
<td>100 μm</td>
<td>100 μm</td>
<td>600 μm</td>
</tr>
<tr>
<td>Freq. Stability</td>
<td>10-100 MHz</td>
<td>&gt;1-10 MHz</td>
<td>0.2-1 MHz</td>
</tr>
<tr>
<td>ESR</td>
<td>~10 mΩ</td>
<td>50 mΩ x mF</td>
<td>&gt;100 mΩ x mF</td>
</tr>
<tr>
<td>% AC/V</td>
<td>-13 % to -70%</td>
<td>~ 0 %</td>
<td>~ 0 %</td>
</tr>
<tr>
<td>Max. Temp</td>
<td>85°C</td>
<td>150°C</td>
<td>125°C</td>
</tr>
</tbody>
</table>

Unique Approach

- High-surface area at ultra-thin form-factor
- Scalable to any design need
- Printed Tantalum Nanoparticles Anode
  - High-surface area at ultra-thin form-factor
  - Scalable to any design need

- Nanoscale Ta₂O₅ Dielectric
  - Paraelectic for DC bias and temperature stability
  - Amorphous for low leakage current

- Conformal Conducting Polymer Cathode
  - Low-resistivity and thick coating for low ESR
  - Self-healing for low leakage current

- Foil-transfer integration
  - Thin-film lamination
  - Ultra-short copper interconnections for reduced impedance
  - Low-cost, panel-scale, 3D approach

Major Accomplishments

- >1μF/mm² up to 1 MHz at 5 V with low ESR, low leakage current, and 100 μm component thickness
Integrated Power Delivery in the Package
Key for High-Performance in Computing

Previously Voltage regulator is designed on the PCB
Few filter capacitors in package

Now, Voltage regulator is moving into the package
More filter capacitors moving into the package

Intel, ECTC 2020
# Inductor Technologies

<table>
<thead>
<tr>
<th></th>
<th>Discrete (Ferrite or Metal powder)</th>
<th>Magnetic composites –substrate-embedding</th>
<th>Nanomagnetic films: On-chip</th>
<th>Need</th>
</tr>
</thead>
<tbody>
<tr>
<td>L/Rdc nH/milliohm</td>
<td>15-25</td>
<td>5-10</td>
<td>0.1-0.2</td>
<td>&gt;&gt;10</td>
</tr>
<tr>
<td>Q</td>
<td>&gt;20</td>
<td>&lt;10</td>
<td>5</td>
<td>&gt;20</td>
</tr>
<tr>
<td>Current-handling A/mm²</td>
<td>0.01 – 0.1</td>
<td>0.1 – 1</td>
<td>5-10 A/mm²</td>
<td>5-10</td>
</tr>
<tr>
<td>Thickness</td>
<td>200- 500 microns</td>
<td>50 - 200 microns</td>
<td>25 microns</td>
<td></td>
</tr>
<tr>
<td>Cost</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
</tr>
</tbody>
</table>

- **Discrete** (Ex. 0.5 x 0.1 x 0.5 mm)
- **KEMET-Tokin**
- **Nitto Denko**
- **Substrate-embedded inductors**
- **Magnetic Core (0.5 - 0.6 mm)**
- **Intel and Ferric**
Prior Art - Inductor Integration

**On-Chip IVR**

**Monolithic integration**
- Magnetic-core inductor
  - CoZrTaB
  - Ms: 1.5 T
  - Hc: 0.39 Oe

**Switching frequency**
- 80 to 100 MHz

**Inductance**
- 300 nH/mm²

- Peak Q Factor > 20 @ ~100MHz
- Peak Inductance Density ~300nH/mm²
- L/RDC >200nH/Ω for L > 100nH
- L/RDC of 120nH/Ω for L ~ 10nH
- Current Density exceeding 12A/mm² for coupled inductors
- Saturation Current exceeding 1.5A for single inductors
- Cross wafer inductance variability σ < 3%
- Other Devices in development:
  - Transformers, improved inductor designs

**On-Chip**

**Monolithic integration**
- Magnetic-core inductor
  - Ni_{45}Fe_{55}
  - Ms: 1.6 T
  - Hc: 0.2 Oe

**Switching frequency**
- 50 to 200 MHz

**Inductance**
- 130 nH/mm²

- Material sample thickness = >40um
- High deposition rate – high throughput and low cost
- IC or glass substrate-compatible
- Deposition thickness capability up to 50um
- \( \mu_r = 200 \), \( B_{sat} = 1.3 \) T, \( Q @ 5 \) MHz>90, \( Q@ 20 \) MHz=30
- 0.5 microhenries; Isat of 2 Amp on 6 inch;
- Toroid and solenoid inductors

**Relative Permeability**

- Frequency (MHz)

**Graphs**
- Various permeability curves and Q factor vs frequency graphs
- Inductance density vs frequency graphs
Magnetic Components: Integration

- Planar transformers with windings implemented on PCB are gaining momentum in R&D and production

<table>
<thead>
<tr>
<th>Component</th>
<th>Conventional Wire-wound</th>
<th>Wire-wound integrated</th>
<th>PCB winding planar core</th>
</tr>
</thead>
<tbody>
<tr>
<td>Method</td>
<td>Wire-wound</td>
<td>Wire-wound integrated</td>
<td>PCB winding planar core</td>
</tr>
<tr>
<td>Structure</td>
<td><img src="image1" alt="Image 1" /></td>
<td><img src="image2" alt="Image 2" /></td>
<td><img src="image3" alt="Image 3" /></td>
</tr>
<tr>
<td>Power</td>
<td>3.3kW</td>
<td>192W</td>
<td>5 kW</td>
</tr>
<tr>
<td>Profile</td>
<td>&gt; 45 mm</td>
<td>&gt; 30 mm</td>
<td>20 mm</td>
</tr>
<tr>
<td>Leakage inductor</td>
<td>Discrete</td>
<td>Integrated</td>
<td>Integrated</td>
</tr>
<tr>
<td>Process</td>
<td>Manual (Litz wire)</td>
<td>Manual (Litz wire)</td>
<td>Thick Cu PCB</td>
</tr>
<tr>
<td>Repeatability</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

- Monolithic integration of transformer and inductors on single core to minimize part count

Haksun Lee, GT

Source: Virginia Tech, APEC 2015
Source: NUI Galway
Medium Frequency – Medium Power: Inductor Advances

**PSI2: Inductor in package molding**

Better thermal, shielding,
High current-handling and efficiency

2.8% increase in efficiency with 3-5 Amp current

**Virginia Tech: Inductor in PCB Substrate**

Inductors integrated in substrates
- Air-core inductors
- Multiple domains
  - High-current: >20 A
  - Medium-current: 5-20 A
  - Low-current: <5 A
- Switching frequency: 140 MHz

**Inductor in package**

4X increase in current-handling with metal compacts compared to ferrites
High-Density Embedded Inductors for Integrated Voltage Regulators

Objectives

- Embedded inductors for power converters:
  
  Target
  
  20 nH/milliohm

  2 A/mm²

  20-50 microns

Unique Approach

1. Substrate-compatible magnetic composites with high permeability
   - High permeability for high-inductance density
2. Embedded solenoid inductors
   - Embedding for miniaturization
   - Design for high-current density
3. Substrate design rules to fabricate thick copper
   - Low resistance

Major Accomplishments

- Embedding of high current density and high-efficiency inductors embedded in organic substrates. Current status:
  
  - Thickness: 500 μm
  - Inductance: 8nH/mm²
  - Current: Projected to 1 A/mm²
  - Resistance: projected to <10 mΩ
3D Power Packaging

- Multiphysics converter design (topology & hardware co-design)
- Advanced GaN devices & high-temp passives

Infineon

- Structure and process innovations
- Doubleside wafer plating
- Panel-scale embedding of power devices
- High-temperature materials with enhanced interfaces for Hi-Rel

Schweizer

- Sintered copper interconnections between devices, IMS or leadframe and PCB
- Barriers for oxygen and moisture
- Advanced encapsulants

AT&S

- Advanced cooling loop with temp uniformity
- System-level thermomechanical and electrical reliability:
Improvement trends* for different system components

- Signal and power connections in one device
- Integration of water pipes
- Higher operating temperature
- Improved accuracy
- Small and compact designs

- High operating temperature and high voltages
- Faster response time
- Higher operating temperature
- Direct liquid systems

- Coreless transformer isolation
- Capacitive coupling isolation

- Faster response time
- Higher operating temperature
- Direct liquid systems

Laminated busbars

DC link capacitors

Fuses, over voltage protections, etc.

Current sensors

Cooling systems

Discrete devices

Power modules/IPM

Switching drivers

*Non-exhaustive list

New substrate materials
- Bond-free interconnections
- New encapsulation materials

Wide Band Gap
- High temperature packaging
- Advanced packaging in power

Yole
# Evolution of Die-Attach Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Pressureless assembly capability</th>
<th>Electrical and thermomechanical reliability performance</th>
<th>Safety</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-lead solders</td>
<td>Pressureless</td>
<td>Moderate with low homologous temperature</td>
<td>Lead-based</td>
<td>High</td>
</tr>
<tr>
<td>Transient Liquid Phase Sintering</td>
<td>Requires pressure</td>
<td>Moderate with kirkendall voids</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nanosilver</td>
<td>Requires more pressure</td>
<td>Microstructural instabilities and diffusion</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nanocopper</td>
<td>Pressureless with reactive nanosurfaces</td>
<td>Die shear strength is low with smooth backside metallization</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nanocopper-microwire-graphene multilayers</td>
<td></td>
<td></td>
<td></td>
<td>Low, because of design and process flexibility</td>
</tr>
</tbody>
</table>

- **High-lead solders**: Koduri, Texas Instruments. Current is not needed for lateral GaN die-attach.
- **Transient Liquid Phase Sintering**: Infineon. Jiang Li (TI, Virginia Tech).
- **Nanocopper**: Infineon. Jiang Li (TI, Virginia Tech).
- **Nanocopper-microwire-graphene multilayers**: Vanessa Smet, Georgia Tech.
Low Power (Consumer Electronics) to High Power

- 1.2W, 900W/in^3
- 10W, 350W/in^3
- 500W, 308W/in^3
- 30kW, 81W/in^3

- Higher frequencies
- Higher power densities
- More integration
- Single package solutions

Micro power module at 2MHz
Step down converter at 780kHz
GaN DC-DC converter
30kW all SiC inverter

Haksun Lee, GT
## High-Power Packages – Leading-edge Products

<table>
<thead>
<tr>
<th>Package structure</th>
<th>Standard wire bond package</th>
<th>Cu pin interconnect w/ thick Cu DBC</th>
<th>Double-sided liquid cooling</th>
<th>Cu traces on flexible foil w/ sintered joints</th>
<th>Planar interconnect using Cu plating</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Conventional</td>
<td>Fuji Electric</td>
<td>Denso</td>
<td>Semikron SKiN</td>
<td>Siemens SiPLIT</td>
</tr>
</tbody>
</table>

### Package structure

- **Cross-section**

### Parasitic inductance

- Not Available

### Thermo-mechanical

- Very bad

### Note

- Wire bond
- Solder die attach
- Cu pin joints
- Gel replaced with epoxy
- Double sided cooling
- Double DBC
- FPCB Gate drive integrated
- Ag sintered joints
- Area joints by Cu electroplating

---

*Sources*:

- Haksun Lee, GT
Traditional to 3D Power Packaging

- Reliability challenges with nanocopper and nanosilver
- Thick packages
- Large electrical inductance and high thermal resistance

Leadframe Fan-Out Packaging
- No reliability challenges with nanocopper
- (Bonding layers are in compression)
- Thin packages
- Lower electrical inductance and thermal resistance

Heat generation: 100 W
Heat transfer coefficient: 10,000~50,000 W/m²K
Traditional to 3D Power Packaging

- **Reliability challenges with nanocopper and nanosilver**
- **Thick packages**
- **Large electrical inductance and high thermal resistance**

**Leadframe Fan-Out Packaging**

- **No reliability challenges with nanocopper**
- **(Bonding layers are in compression)**
- **Thin packages**
- **Lower electrical inductance and thermal resistance**

![Diagram of a converter system](image)

- Bypass capacitor
- SiC MOSFET
- Cross-section
- Current sensor
- Gate driver
- Components embedded in substrate
- Reactor
- One block of converter
- Full converter

**Heat generation**: 100 W

**Heat transfer coefficient**: 10,000~50,000 W/m²K

Mitsubishi Electric
3D Power Packaging: AT&S and GaN Systems

AT&S

- Planar Surface-embedded components (PARSEC)
- 250-450 V; 200 A: 50 kW inverter
- IMS PCB with thermal-conducting prepregs
- Better partitioning, faster switching, reduced switching losses
3D Power Packaging - Schweizer

- Thick lead-frame heat-spreader with cavity for die placement
- Laser-drilled and plated-vias for top interconnect on top side (logic integration possible)
- Power embedded PCB offers improved electrical, thermal performance with increased power density

P2Pack Half-bridge with embedded shunt:
- No die-attach reliability concerns
- Laminate temp: 175-220 C
- 38% reduction in losses for power PCB
  - Over 100-500 Amp

- Improved switching behavior
- Reduced losses
- Optimized heat dissipation
- Control & power co-integration

Kearney et al., ABB Corporate research

- 50% improvement in performance
- 4.5-9W ; 3-5 K rise in temperature;
- 0.05 -0.1 milliohm resistance
Reliability Challenges

- Cracking of thick vias
- Dielectric cracking at stress-intensive points

- Partial discharge:
  - 41-50 kVrms/mm before aging
  - 32-36 kVrms/mm after aging
  
  Lifetime = \( C/E^n \)
  
  - \( n = 10-11 \)
  - \( n = 14-16 \)

ABB/Schweizer
Example of electrical breakdown at high fields

Infineon power module (low CTE, high Tg, high fillers or fibers)

Bosch/Schweizer/Isola
Resin cracking in standard resins (left), no cracking with advanced epoxies
Low-Frequency - High-Power Magnetics

- Ferrite 3C90:
  - 500 kHz: 0.1 T peak; 700 mW/cc;
  - 1 MHz: 0.02 T; 70 mW/cc;

- Ferrite 3F5 MnZn:
  - 1 MHz; 0.02 T; 30 mW/cc

- Sumida’s ferrite:
  - 1.5 MHz; 0.02 T; 37 mW/cc
  - 1 MHz; 0.02 T; 70 mW/cc
  - 200 kHz; 0.1 T; 250 mW/cc

Vitrovac (Co_{67}Fe_{4}B_{11}Si_{16}Mo_{2}) amorphous flakes:
- 100 kHz; 0.1 Tesla; 30 mW/cc;
- 100 kHz; 0.2 Tesla; 200 mW/cc

- Hitachi metals: Finemet - FT-3L and FT-3M:
  - 20 kHz; 0.1 Tesla; 2 mW/cc
  - 20 kHz; 0.2 Tesla; 15 mW/cc
  - 20 kHz; 1 Tesla; 300 mW/cc

Permeability of 10,000 to 100,000
20 kHz x 50 mT << 500 W/cc

Ms: 1.5 – 2 Tesla;
1-5 A/m of Coercivity
<100 kHz

Nanocrystalline films

Finemet/metglas (Hitachi Metals)
Vittoperm (Vacuum Schmelze)
Nanomet (Alps)
## Comparison of DC capacitors of nominal 1μF/400V_{op}

<table>
<thead>
<tr>
<th></th>
<th>MKP film capacitor</th>
<th>BTO Class 2 MLCC (e.g. X7T)</th>
<th>CeraLink™</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal / rated capacitance</td>
<td>100 %</td>
<td>100 %</td>
<td>100 %</td>
</tr>
<tr>
<td>No bias voltage 0.5 V_{RMS}, 25°C</td>
<td>100%</td>
<td>100 %</td>
<td>35 %</td>
</tr>
<tr>
<td>DC link voltage 0.5 V_{RMS}, 25°C</td>
<td>100 %</td>
<td>35 %</td>
<td>60 %</td>
</tr>
<tr>
<td>DC link voltage 20 V_{RMS}, 25°C</td>
<td>100 %</td>
<td>35 %</td>
<td>100 %</td>
</tr>
<tr>
<td>Typical capacitance density @ DC link voltage 20 V_{RMS}, 25°C</td>
<td>0.7 μF/cm³</td>
<td>2.5 μF/cm³</td>
<td>4.9 μF/cm³</td>
</tr>
<tr>
<td>Typical current rating per capacitance @ 100 kHz, 105°C</td>
<td>&lt;1 A/μF</td>
<td>&lt;4.5 A/μF</td>
<td>12 A/μF</td>
</tr>
</tbody>
</table>

- **KEMET** C0G calcium/zirconate/Ni MLCC
- **TDK** Ceralink capacitors

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Heterogeneous Integration with Nanopackaging

• Power delivery in computing systems
  – Integrated voltage regulator: power conversion closer to the load
  – Capacitors and Inductors: >10 MHz; Impedance < 1 milliohms

• Medium-power packaging
  – Integrated copper carriers
  – Embedded-die packaging with die-attach materials: Silver to nanocopper
  – High-temperature organic packaging

• High-Power packaging:
  – Doubleside cooling, lower parasitics
  – High-voltage passives: 1000 V, planar and higher power densities