Green Innovations for African Renaissance

IEEE Africon 2015 Workshop/Tutorial

Design and Analysis of Low-Power and High-Performance Memory Systems

Workshop/Tutorial Abstract

This tutorial starts with an introduction to memory systems in computing devices such as computers, tablets or smartphones. Then, an in-depth analysis of standard memory systems for low-power and high-performance applications is provided. The interactions between the signaling, clocking architecture and packaging technology of a memory interface as well as how these interactions determine the achievable data rates and power efficiency are discussed. Signaling and clocking schemes for standard memories, including DDR3 and DDR4, and mobile memories, including LPDDR3 and LPPDR4 are detailed and compared against each other. Emerging 2.5D/3D memory systems such as WideIO1/2, HBM1/2, and HMC1/2 are also presented. Packaging options such as BGA, PoP, and the emerging 2.5D/3D are also discussed. To analyze and compare different state-of-the-art memory interfaces, the following metrics are used in the analysis: cost, power efficiency, bandwidth, design complexity, signal and power integrity, thermal solution, and form factor.

Workshop/Tutorial Outline

- *Review of the standard memory systems for workstations, desktop, laptop, tablets, and smartphones. These include memory interfaces for DDR, LPDDR, GDDR, HMC, and HBM systems.*
- *The design challenges of low-power and high-performance memory interfaces in the overall system are presented. The design and optimization of the signalling and clocking architectures, packaging solutions, channel, and power distribution system design is discussed.*
- *The dependence of the memory channels on the system environments is discussed. For example, DDR4 and LPDDR4 and WideIO2 memory systems have different system environment. The driver and receiver complexity and consequently the power consumption depend on the channel attenuation and dispersion and reflection in these memory systems.*
- *The traditional wirebond based packaging technologies for memory application such as Chip-Scale Package (CSP) for DDRx, System-in-Package (SiP) and Package-on-Package (PoP) for LPDDRx are first reviewed. Then, more advanced 2.5D/3D packaging technologies for memory solutions that use TSV technology and Si/Glass interposer for WideIO1 and WideIO2, Hybrid Memory Cube (HMC) and High Bandwidth Memory (HBM) technologies are introduced.*
- *Analysis and comparison of different state-of-the-art memory interfaces using a broad set of metrics including cost, power efficiency, bandwidth, design complexity, signal and power integrity, thermal solution, and form factor are presented.*

Learning Outcome

The attendees will gain an in-depth understanding of high-speed memory interfaces, learn about the interactions between the signaling, clocking architecture and packaging technology of a memory interface, and find out how those interactions determine the achievable data rates and power efficiency. The presenter will demonstrate how this knowledge can be used to analyze and compare different state-of-the-art memory interfaces to help attendees implement or select a solution which best fits their specific application.

Speaker Biography

Wendemagegnehu (Wendem) T. Beyene received his B.S. and M.S. degrees in Electrical Engineering from Columbia University, in 1988 and 1991 respectively, and his Ph.D. degree in Electrical and Computer Engineering from University of Illinois at Urbana-Champaign, in 1997. From 1988 to 1994, he was with the IBM, Microelectronics division, Fishkill, NY, where he worked on design and electrical characterization of advanced multilayer packages. From 1997 to 2000, he was with Hewlett-Packard Company and Agilent Technologies EEsof Divison at Westlake Village, CA working on analog and RF circuit simulation tools. He is currently a Technical Director at Rambus Inc., Sunnyvale, CA and is responsible for signal and power integrity of multi-gigabit memory parallel and serial interface and high-speed link architecture of the development of analysis techniques to define equalization architecture and evaluate timing recovery of high-speed SerDes. His professional interests include high-speed link architecture, simulation and optimization of deterministic and stochastic systems in general and efficient circuit simulation techniques in particular, advanced signaling techniques, and I/O circuitry. He has written over 120 papers in design, modeling, simulation, and measurement of devices, circuits, and high-speed systems. He also holds several granted and pending patents in the area of high-speed links. He also teaches graduate courses at University of California, extension division. He is a senior member of IEEE and has served as Guest Associate Editor of a *Special Issue on high-speed IO channels* in *IEEE Transactions on Advanced Packaging* in May 2009. Since 2010, he has been associate editor of *IEEE Transactions on Components*, *Packaging and Manufacturing Technology*. He also serves on the technical committees of leading international conferences such as *IEEE Electronic Components and Technology Conference* (*ECTC), IEEE Electrical Performance of Electrical Packaging and Systems (EPEPS), IEEE Workshop on High-Performance Chip, Package, and Systems (HPCPS), IEEE* Workshop on Signal and Power Integrity *(SPI), IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)*, and *DesignCon*.