LIVE EVENT

Implementing and Real-Time Testing a Controller for a Grid-Tied Inverter

19 May 2021 | 10:00 - 11:00 (GMT+8)

Starting soon….

Highlights:

Coordinated Control of Distributed Energy Resources (DERs) in Microgrids

in Collaboration with **IEEE Power & Energy Society Singapore Chapter**

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Using Simulink to Develop Grid-Tied Inverter Controls

Table of Contents

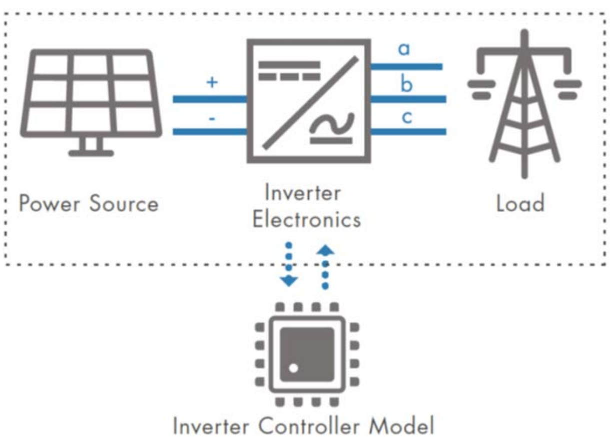
- Introduction
- What is hardware-in-the-loop?
- Overview of solar inverter control development
- Control design tasks for power capture and grid protection
- Code generation for controller and plant
- Hardware-in-the-loop testing with Speedgoat hardware

Key Takeaways

- Simplify control development for power electronics using Simscape Electrical and Speedgoat hardware
- Automatically generate C and HDL code for plant simulations and production code from Simulink and Simscape Electrical
- Use hardware-in-the-loop to test normal operation and fault conditions such as Fault-Ride Through

Simulink and Speedgoat are a common platfor control design and testing

Design and optimize controls using electrical systems simulation



Generate code for the plant

and the controller

About Speedgoat

- A MathWorks associate company, incorporated in 2006 by former MathWorks employees. Headquarters in Switzerland, with subsidiaries in the USA and Germany

- Provider of real-time target computers, expressly designed for use with Simulink

- Real-time core team of around 200 people within MathWorks and Speedgoat. Closely working with the entire MathWorks organization employing around 5,000 people worldwide

What is Our Goal?

- Primary goal is to design power electronics hardware and controllers

Controller

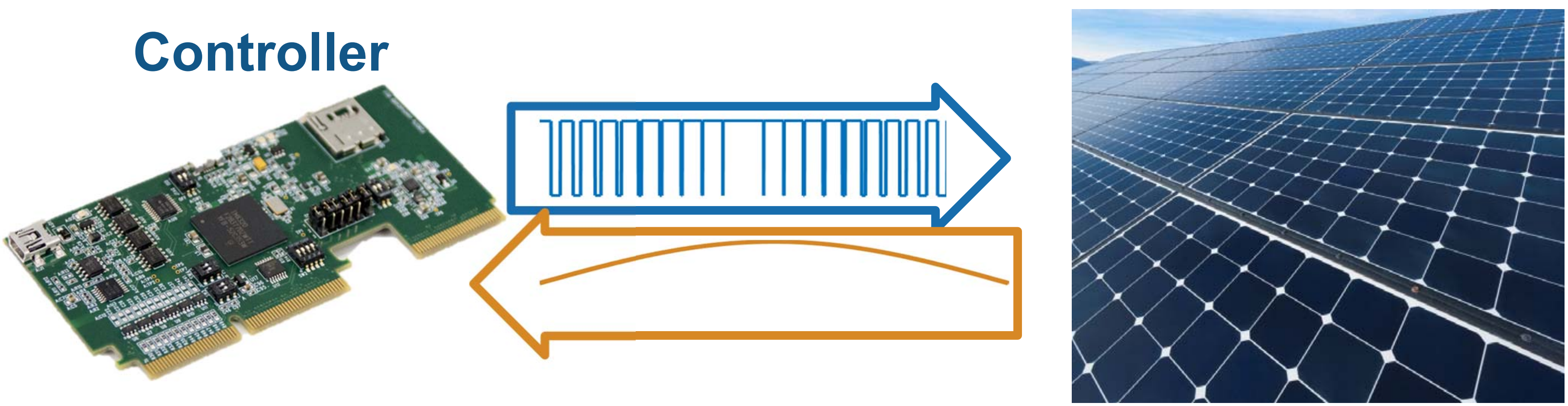
Hardware (Plant)

What is Our Goal?

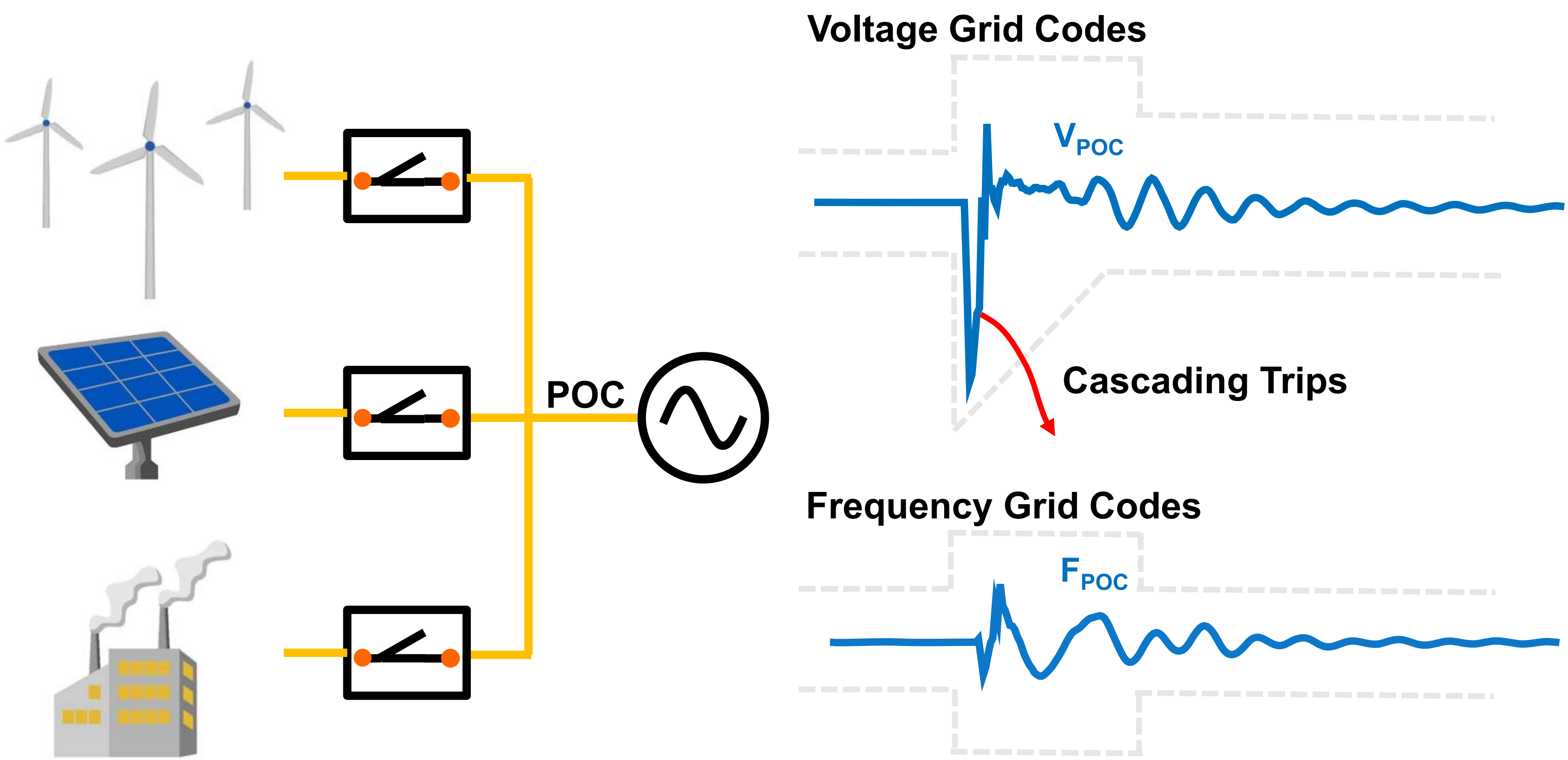
- Primary goal is to design power electronics hardware and controllers
  - Hardware in the loop (HIL) testing can improve this process

Hardware (Plant)

Controller

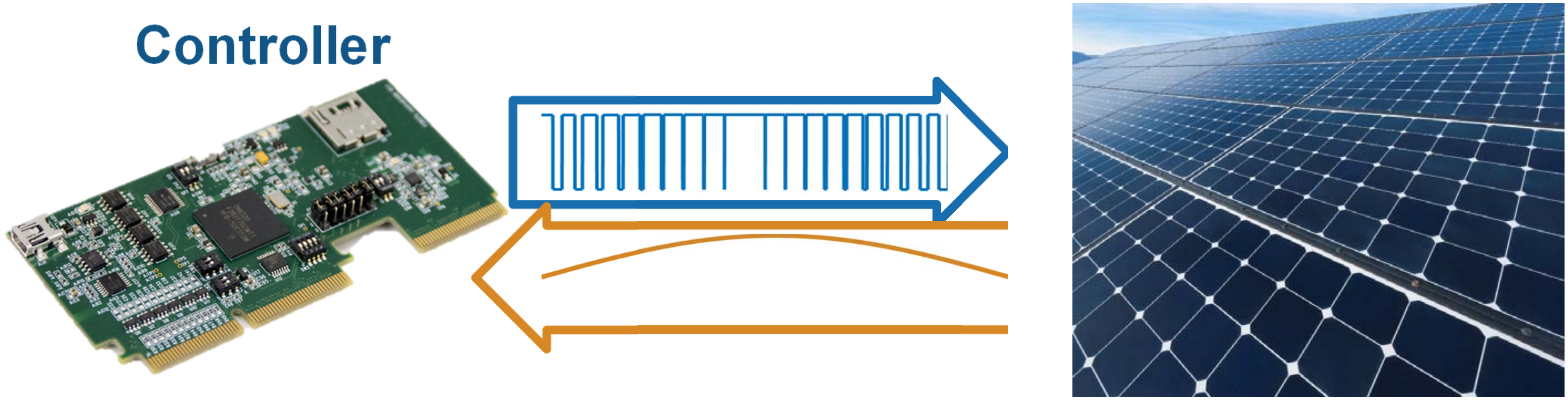


Protecting the Utility Grid



What is Hardware in the Loop (HIL) Testing

- HIL replaces the power electronics hardware with a virtual simulation

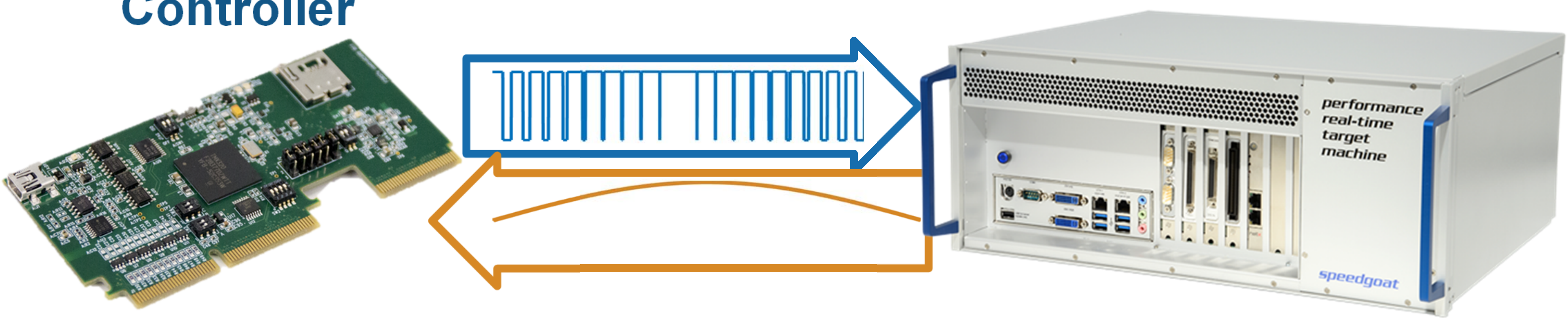


What is Hardware in the Loop (HIL) Testing

- HIL replaces the power electronics hardware with a virtual simulation
  - Controller can operate as if in the real system

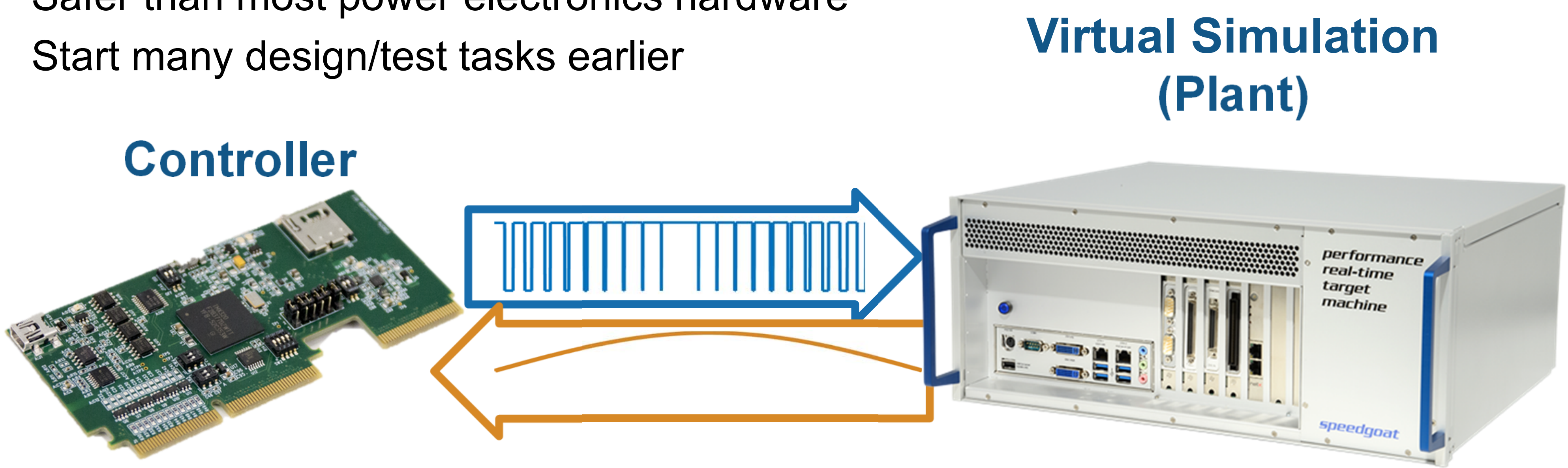
Virtual Simulation (Plant)

Controller

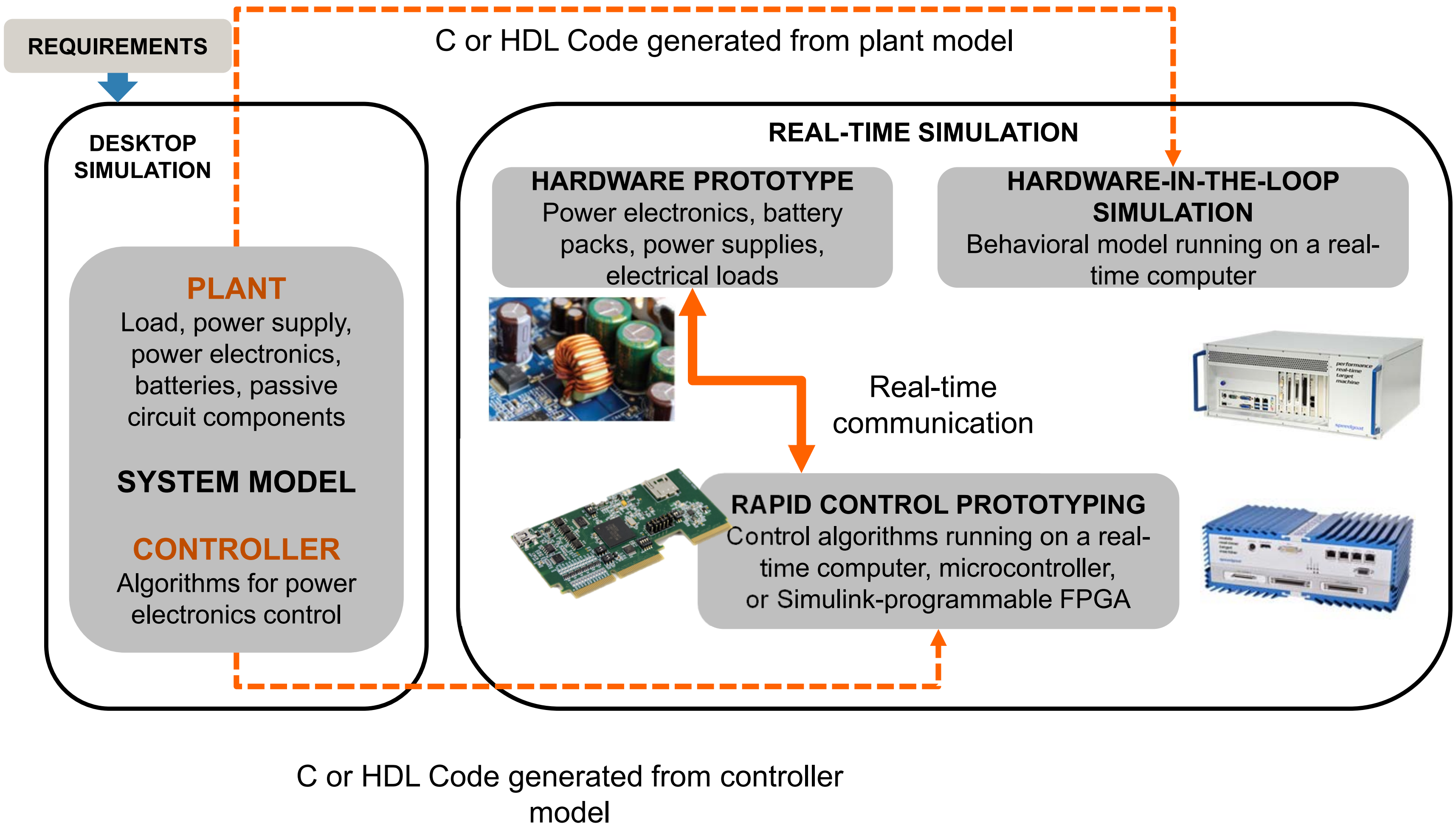


Advantages of Hardware in the Loop (HIL) Testing

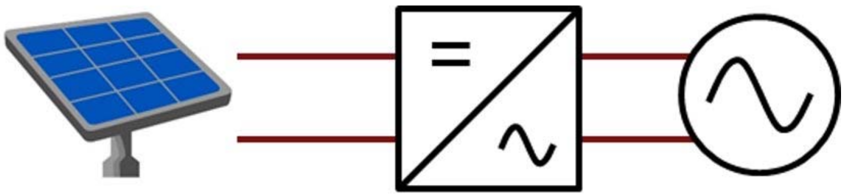
- Can replace prototypes or production hardware with a real-time system
- Easier to automate testing and **test grid code fault scenarios**
- Safer than most power electronics hardware
- Start many design/test tasks earlier

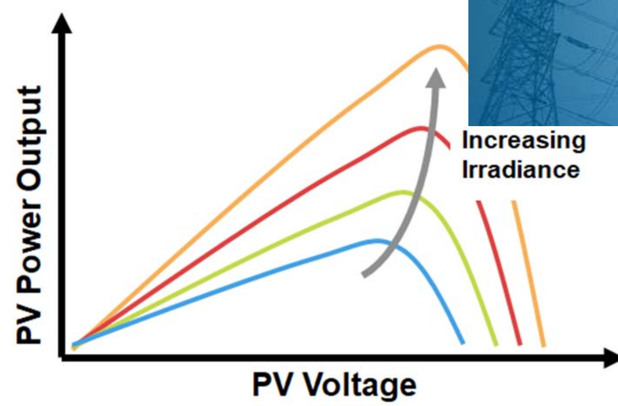


Model Based Design for Power Electronics



Overview of Solar Inverter Control Development

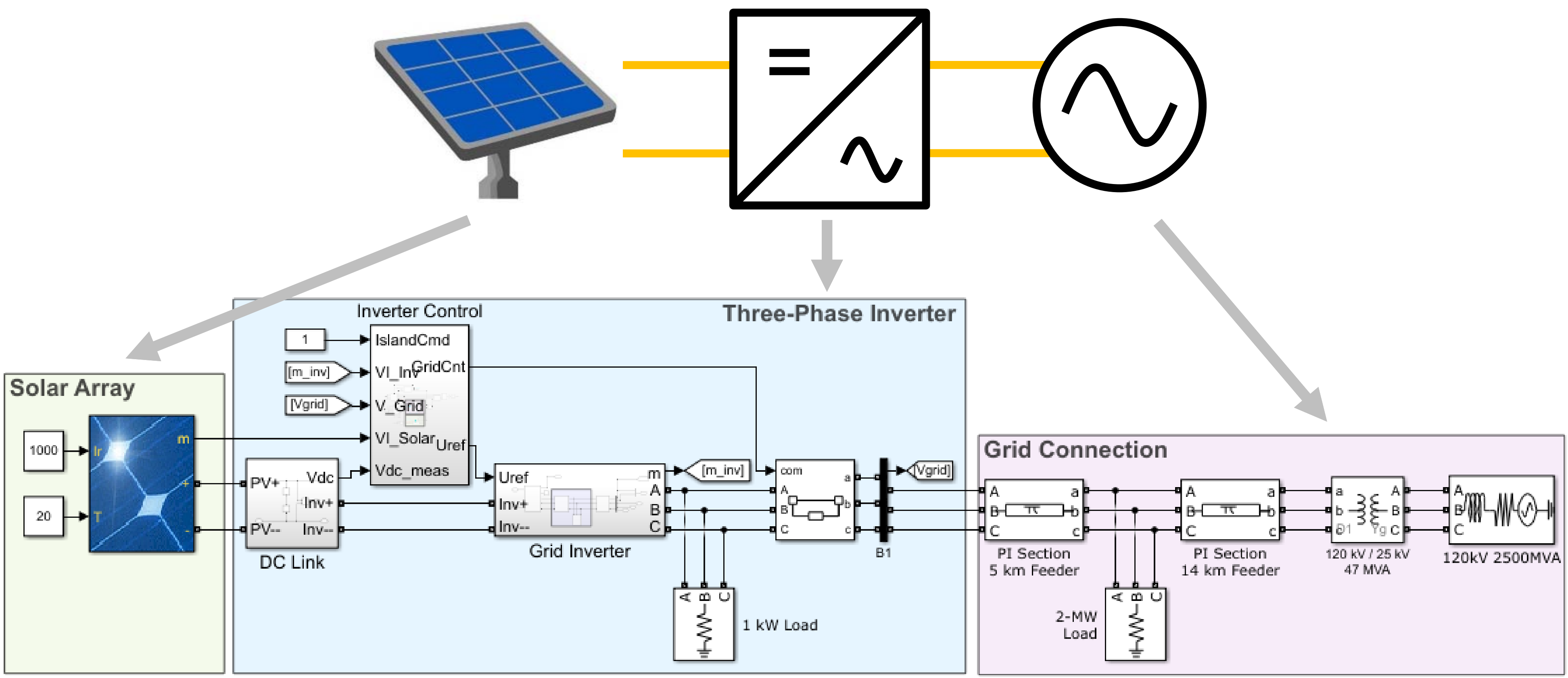




1. **Plant Modeling**
   (Photovoltaic plant, Inverter, Grid)
2. **Control Design**
   (Grid synchronization, MPPT algorithm)
3. **Automatic Code Generation**
   (Deploy code to TI C2000 and Speedgoat hardware)
4. **Hardware-in-the-Loop Testing**
   (Controller verification with Speedgoat hardware)

1 Plant Modeling

Schematic-based modeling with common power electronics topologies



Layers of Control in Smart Grid Applications

IEEE1676 – Power Electronic Building Blocks

Control Transients

Hours

- Peak Shaving/Load Leveling
- Energy Markets
- Integration of Renewables
- Islanding Operation (No Grid)

Seconds

- Voltage/Frequency Regulation
- Transient Smoothing
- Reactive Power Control

m/μ-Seconds

- Switched-Mode Control
- Harmonic Analysis

System Control

Application Control

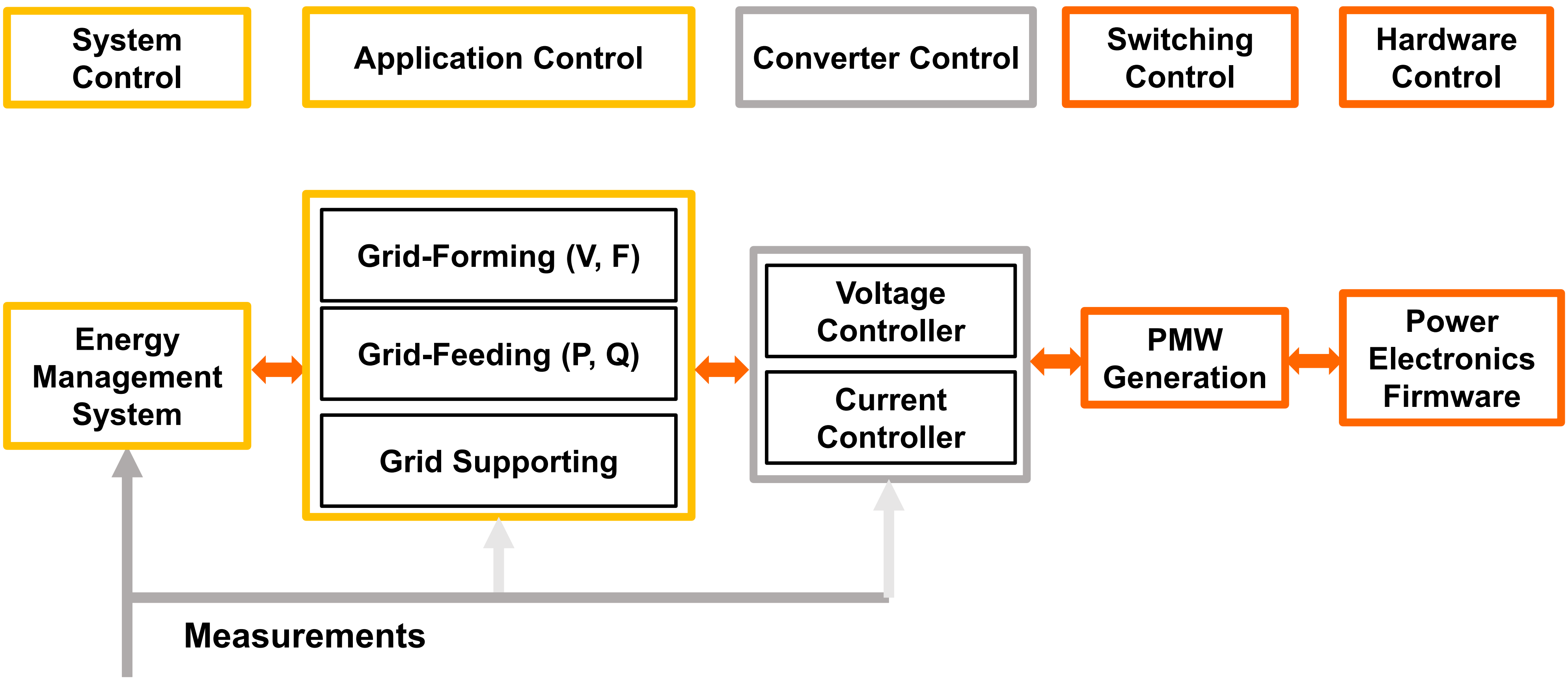
Converter Control

Switching Control

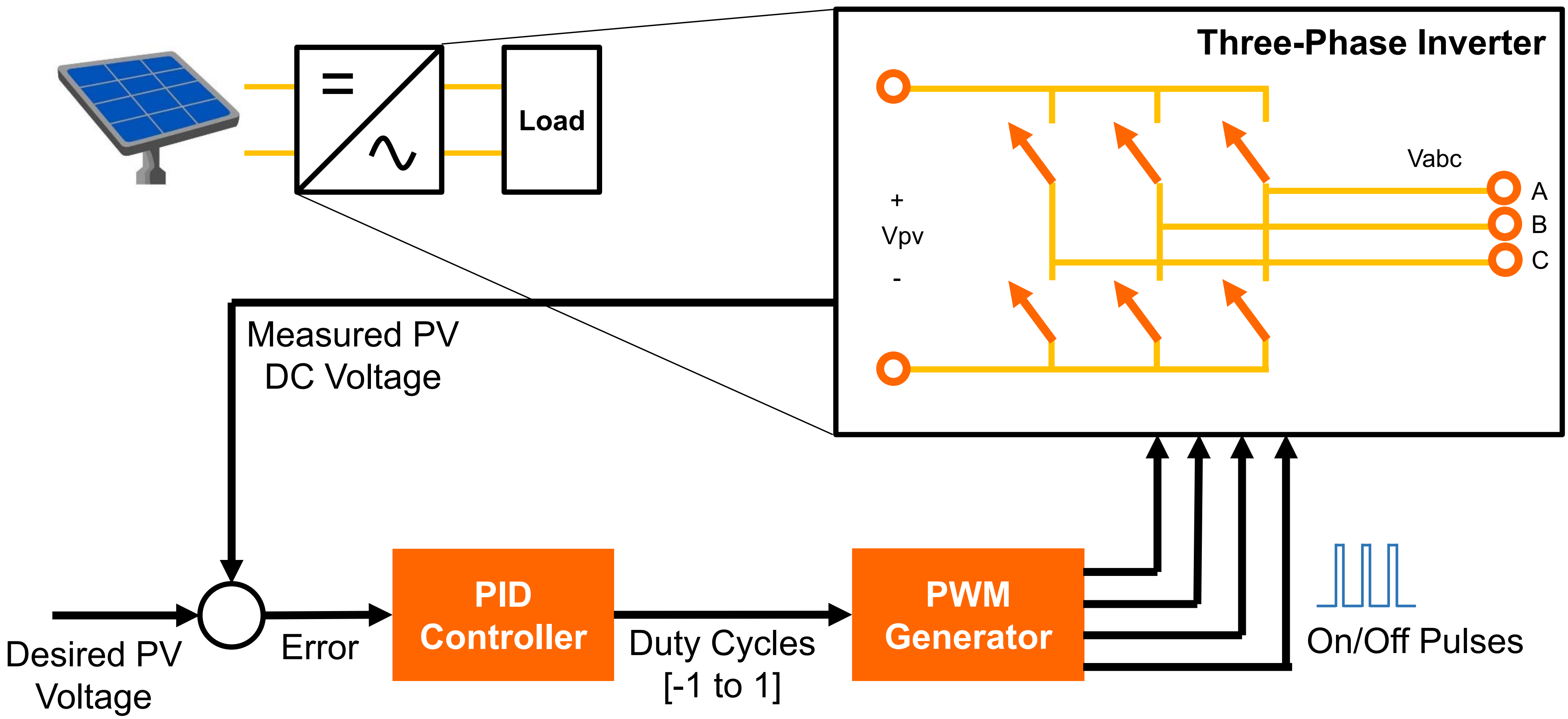
Hardware Control

Layers of Control in Smart Grid Applications

IEEE1676 – Power Electronic Building Blocks

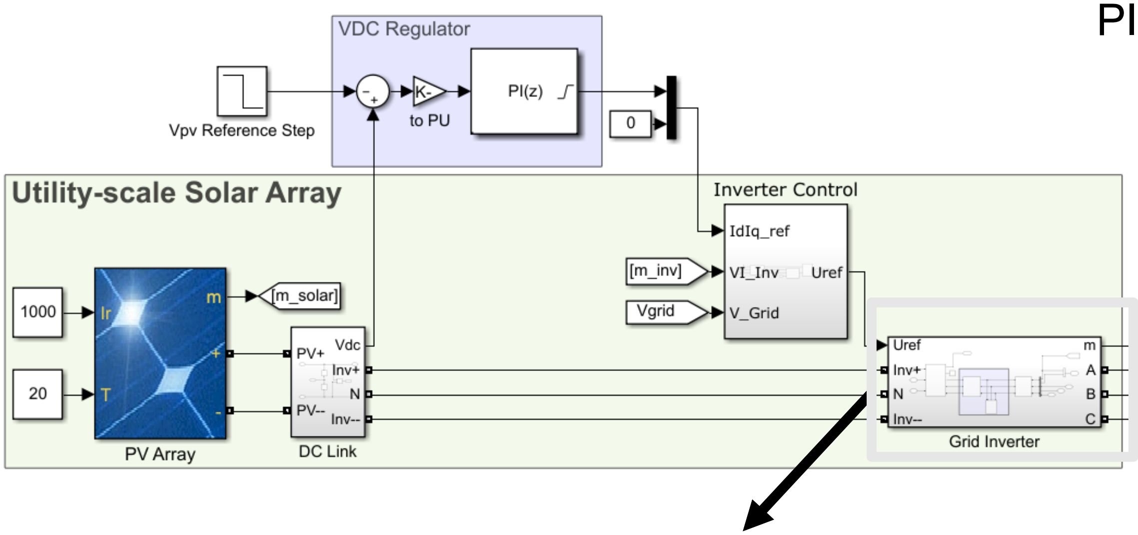


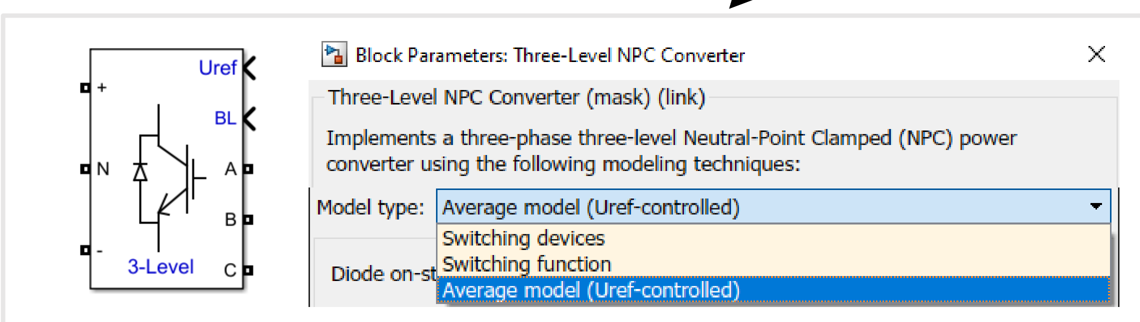
Control Design Task 1 - Power Electronics Feedback



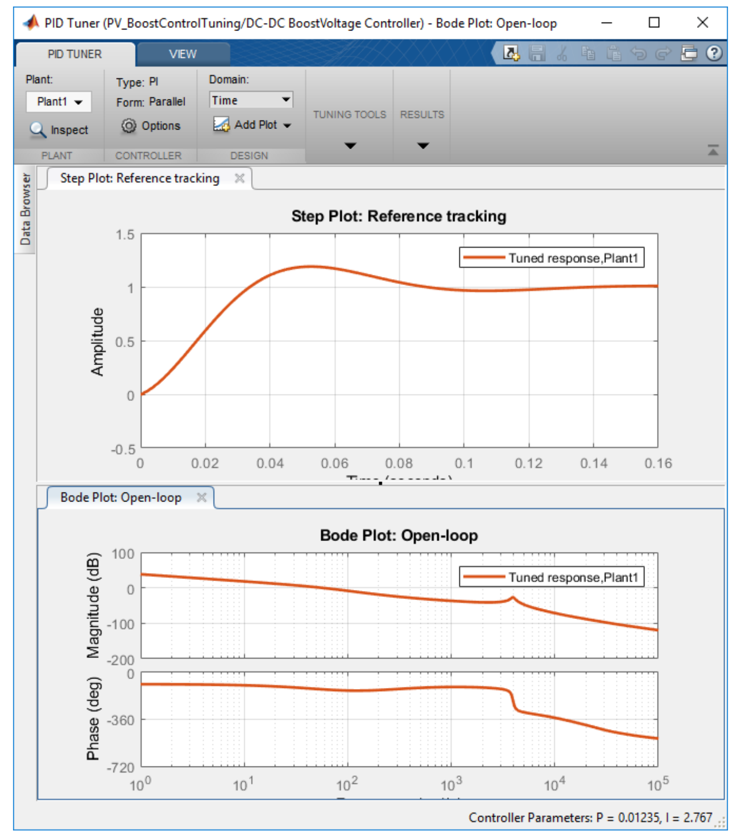
2 Tuning DC-DC Boost Converter Controls

PID Tuning (and other methods) on Non-linear and Switched-Mode Power Systems

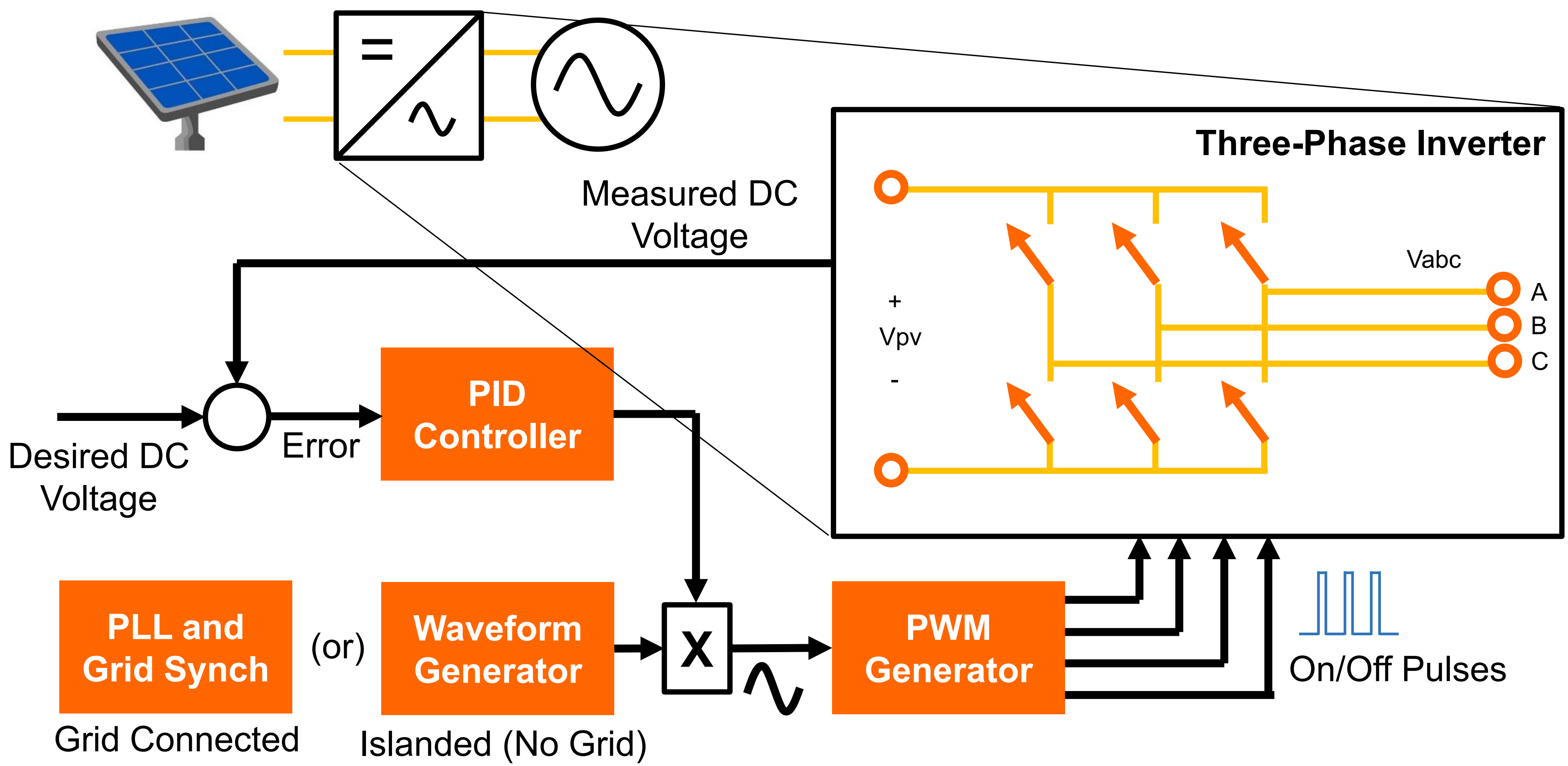




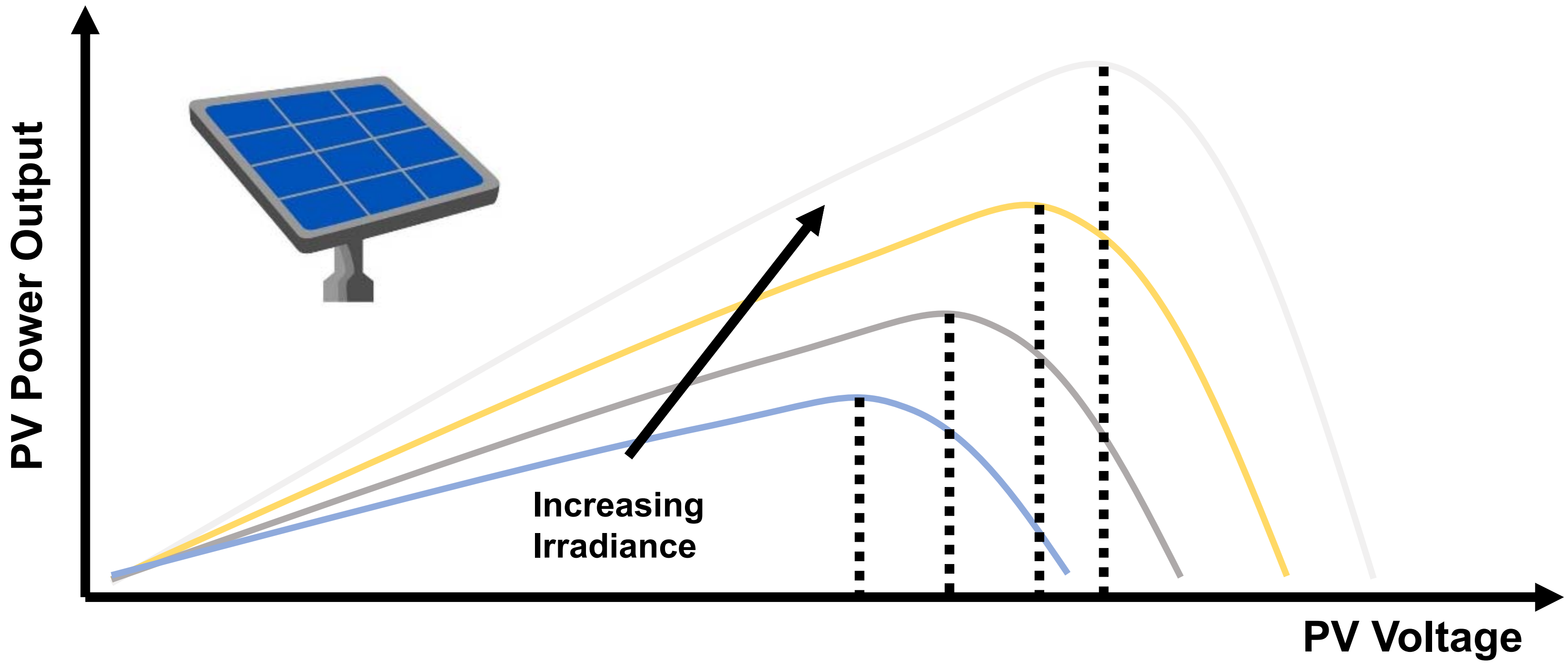
Leverage Average-Value Approximation of Power Electronics for Control Design



2 Control Design Task 2 – Grid Synchronization



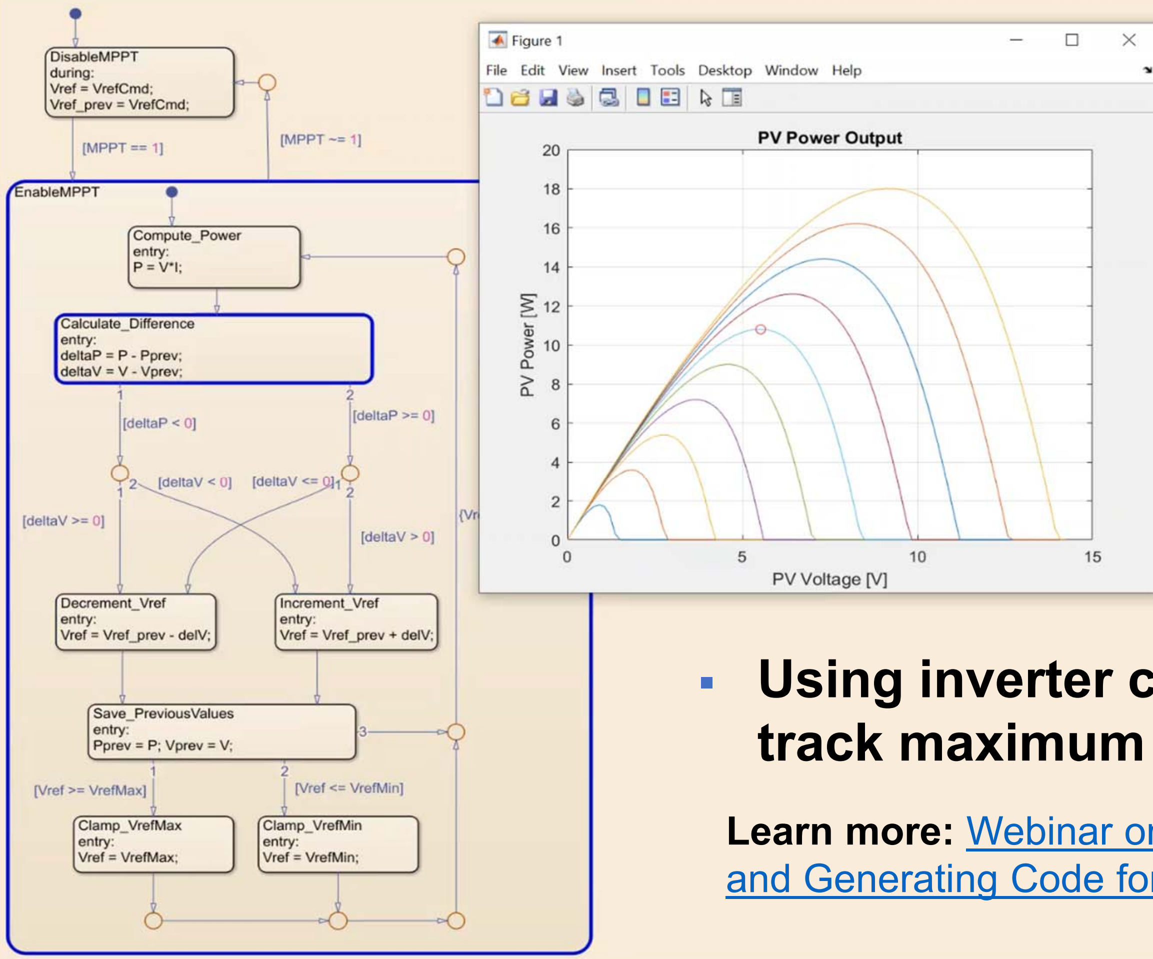
2 Control Design - MPPT



Maximum Power Point Tracking

Automatically adjust desired PV Voltage to find Peak
Power Output at any Operating Condition

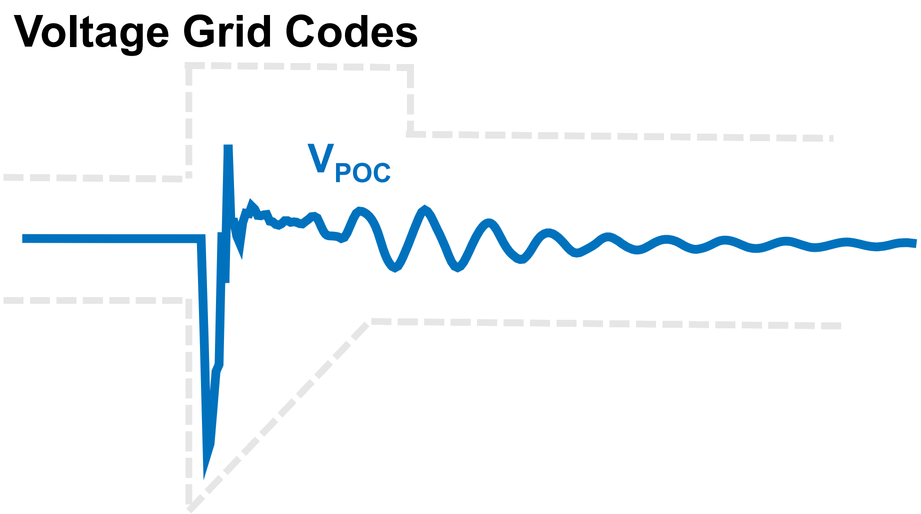
2 Control Design - MPPT

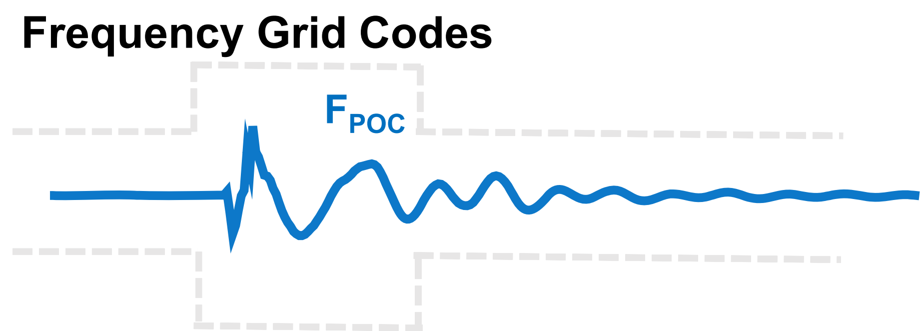


- **Using inverter control to track maximum power point**

Learn more: [Webinar on Modeling, Simulating, and Generating Code for a Solar Inverter]()

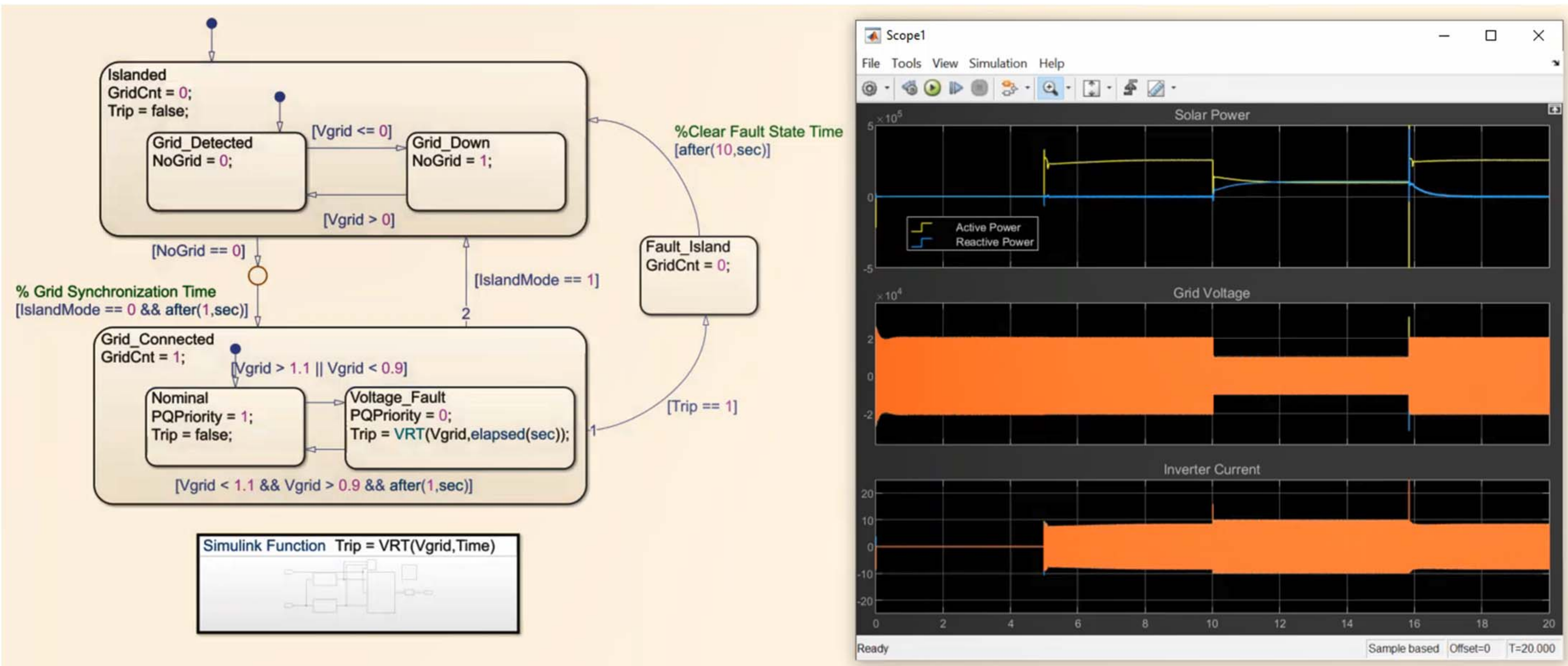
2 Control Design - Designing Fault-Ride Through Algorithms





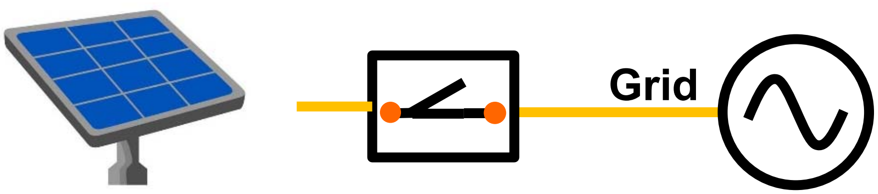
② Control Design - Designing Fault-Ride Through Algorithms

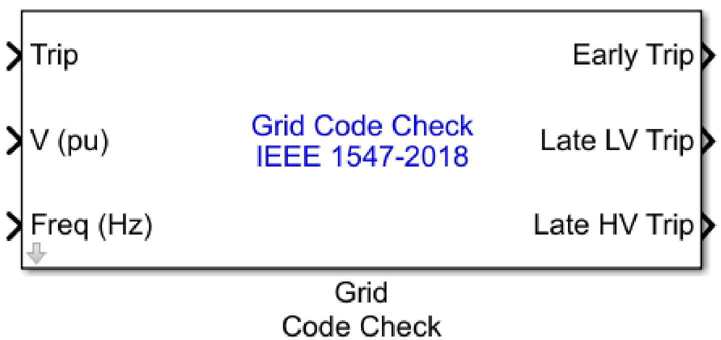
- **Reactive power support during low voltage fault**

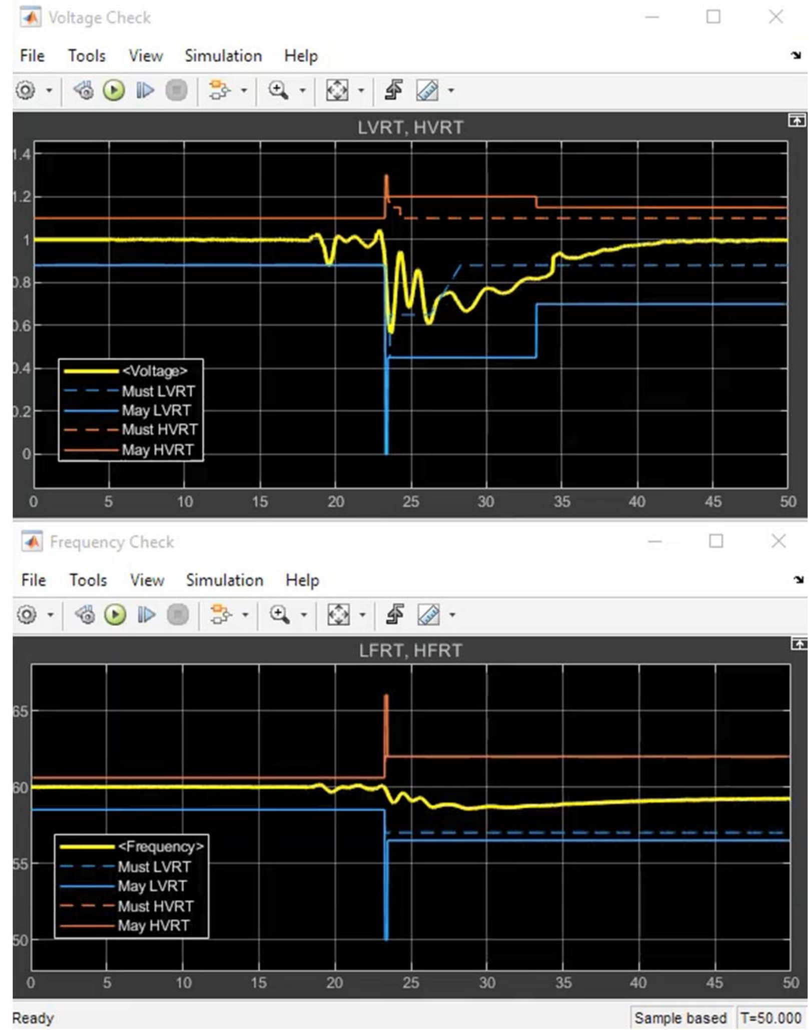


2 Control Design - Fault-Ride Through

- **Testing Fault-Ride Through against Grid Codes such as IEEE 1547-2018**





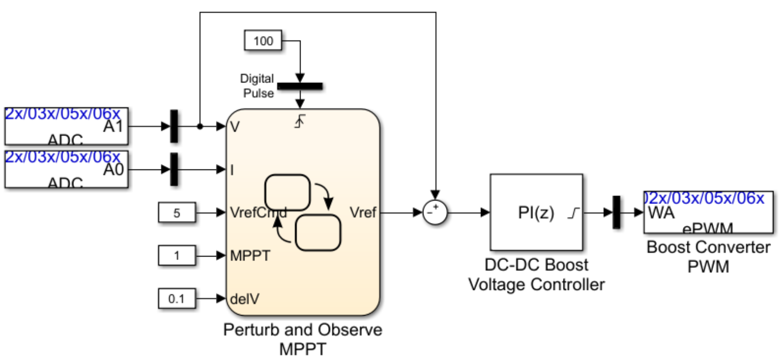


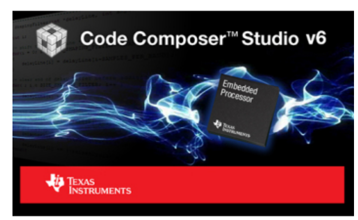
Learn more: Webinar on Renewable Grid Integration Studies

3 Automatic Code Generation
Microcontroller

- **Use Embedded Coder and C2000 hardware support package**

Combine Simulink Algorithms with C2000 IO Blocks	Auto-generate C code	Build and Implement using CCS	Operation Check with TI C2000



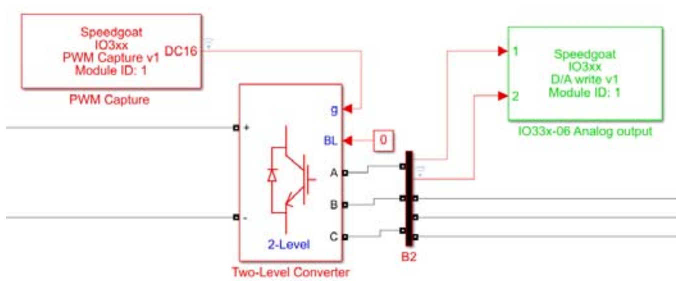


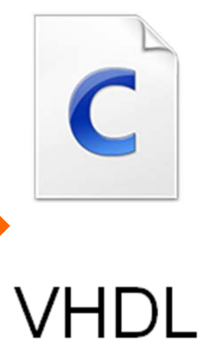
3 Automatic Code Generation

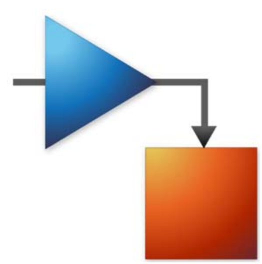
Speedgoat Real-Time Simulator

- Use Simulink Real-Time and HDL Coder for C and HDL code generation
- Deploy to multi-core CPUs or multiple FPGAs
- Wide range of I/O connectivity, communication protocols and I/O functionality

Combine Simulink Model with Speedgoat Driver Blocks	Auto-generate C code or HDL Code	Build using Simulink Real-Time	Operation with Speedgoat Target Computer







4 Hardware-in-the-Loop Testing

- **Reuse models at different levels of fidelity in CPUs and FPGAs**

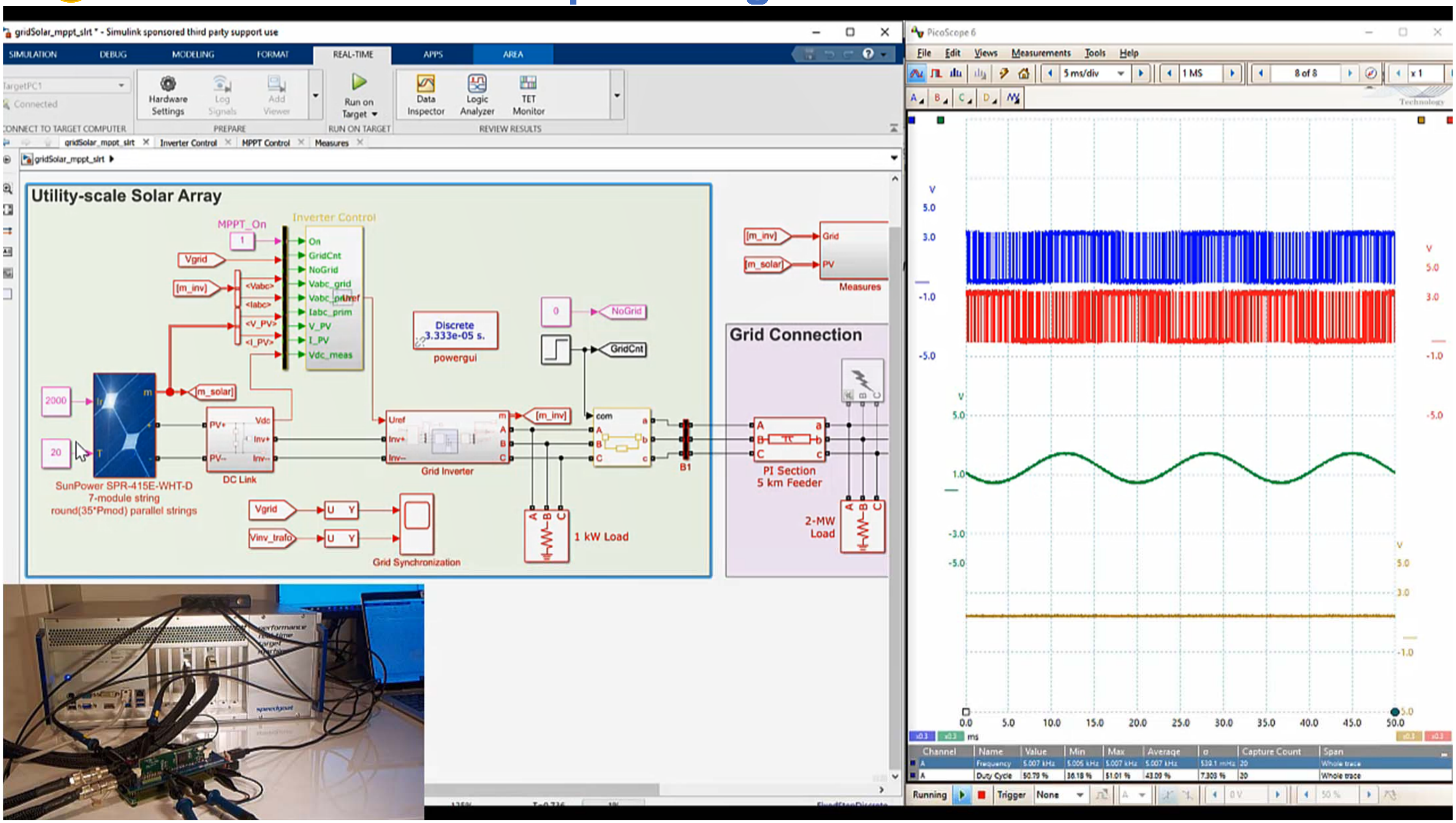
- **Automatic code generation**
  - **Multi-core CPUs using Simulink Real-Time**
  - **Simulink-programmable FPGAs using HDL Coder**

- **Compatibility of Simulink, V&V tools and Speedgoat hardware**

- **HIL simulation with switching dynamics**
  - **CPU workflow up to around 5 KHz switching**
  - **FPGA workflow up to around 100 kHz switching**

4 Hardware-in-the-Loop Testing

MathWorks speedgoat real-time simulation and testing



Conclusion

- Simplify control development for power electronics using Simscape Electrical and Speedgoat hardware
- Automatically generate C and HDL code for plant simulations and production code from Simulink and Simscape Electrical
- Use hardware-in-the-loop to test normal operation and fault conditions like Fault-Ride Through

Learn More

- www.speedgoat.com – Speedgoat real-time solutions
- Developing Solar Inverter Control with Simulink – video series
- HIL for Power Electronics - whitepaper
- Detailed Model of 100 kW Grid-Connected PV Array - example
- MPPT Algorithm - webpage

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Coordinated Control of Distributed Energy Resources (DERs) in Microgrids

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Chairman | IEEE PES Singapore Chapter
Website： https://eexuyan.github.io/soda/index.html

0. Outline

1. REIDS Project

2. Control
1) Islanded mode
2) Grid-tied mode

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1 **REIDS Project**

2 **DER Control**
- Islanded microgrid
- Grid-connected microgrid

0. Outline

1. REIDS Project

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1) Islanded mode

2) Grid-tied mode

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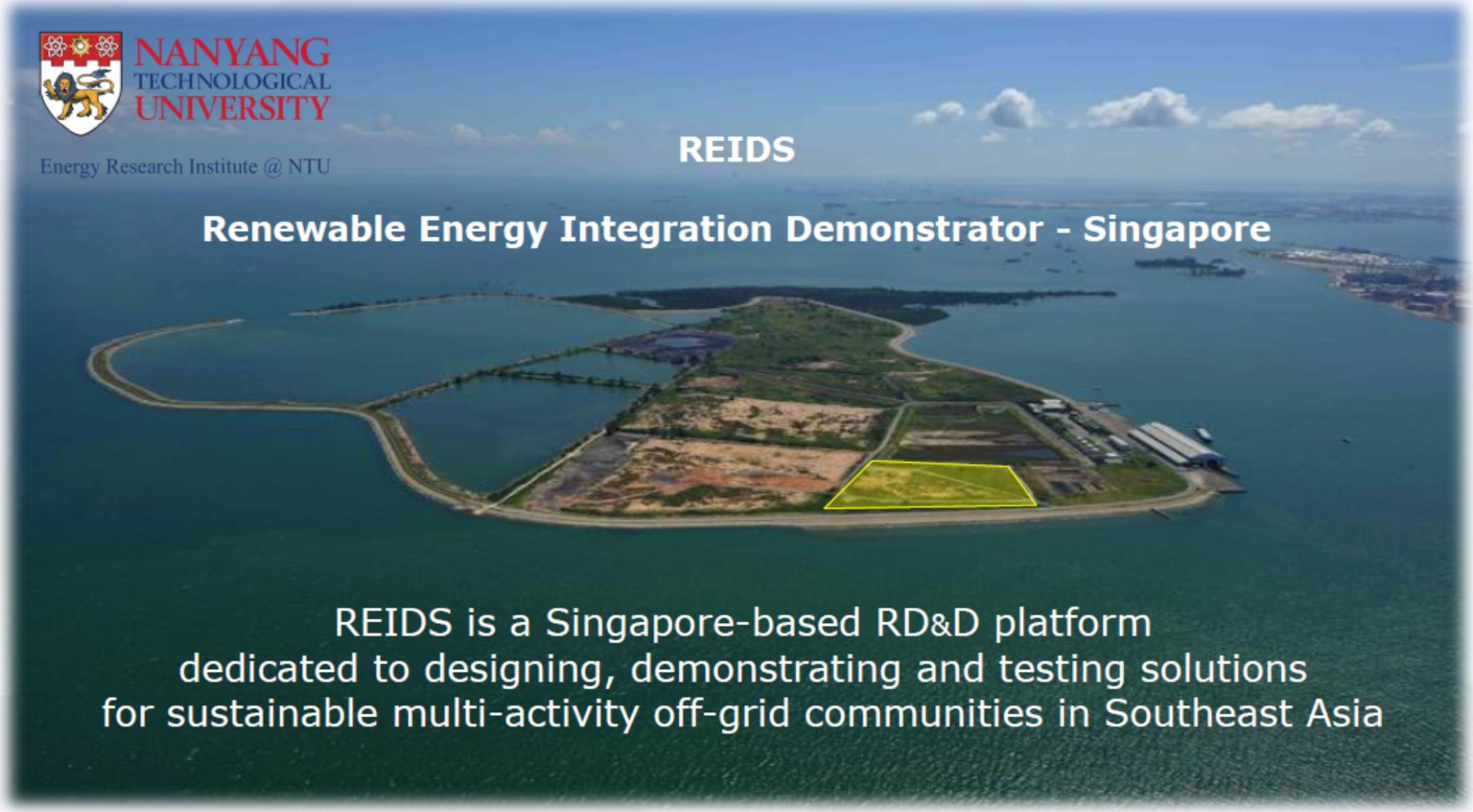
- *Renewable Energy Integration Demonstrator – Singapore* (REIDS)



http://erian.ntu.edu.sg/REIDS/Pages/AboutREIDS.aspx

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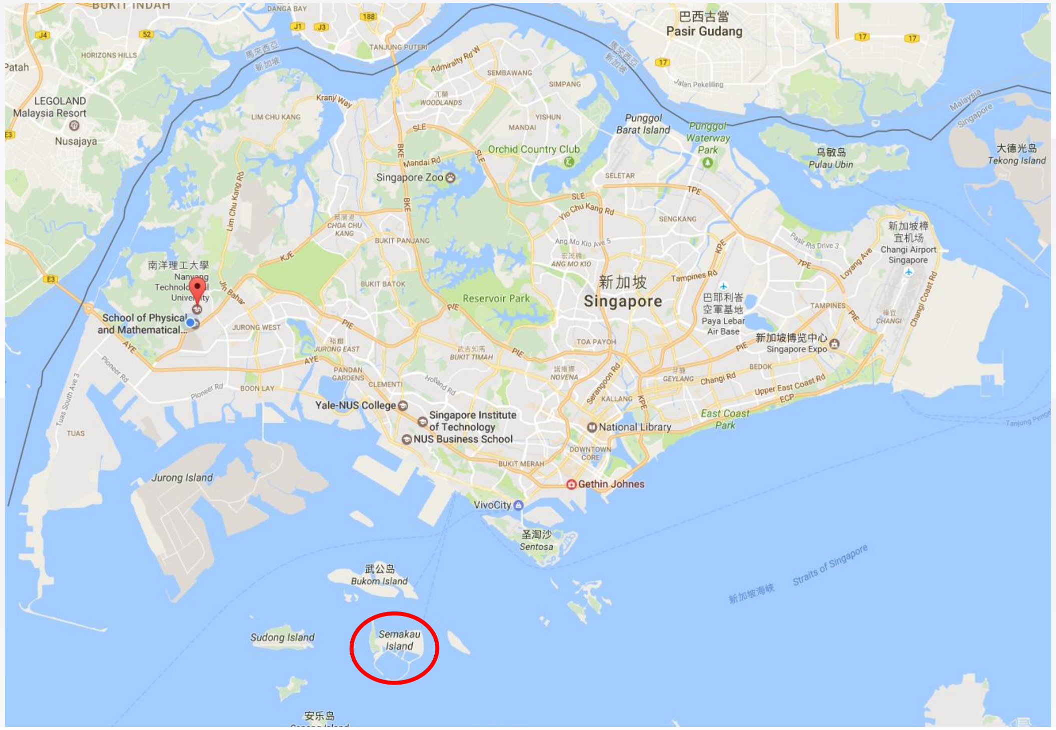

REIDS Partners

accenture
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EMERSON
eNGIe
Evolution Energie
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Keppel Offshore & Marine
MEDCOENERGI Power
MERALCO
muRata INNOVATOR IN ELECTRONICS
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Supporting Agencies

EDB singapore
National Environment Agency Safeguard · Nurture · Cherish
Energy Market Authority Smart Energy, Sustainable Future
National Research Foundation

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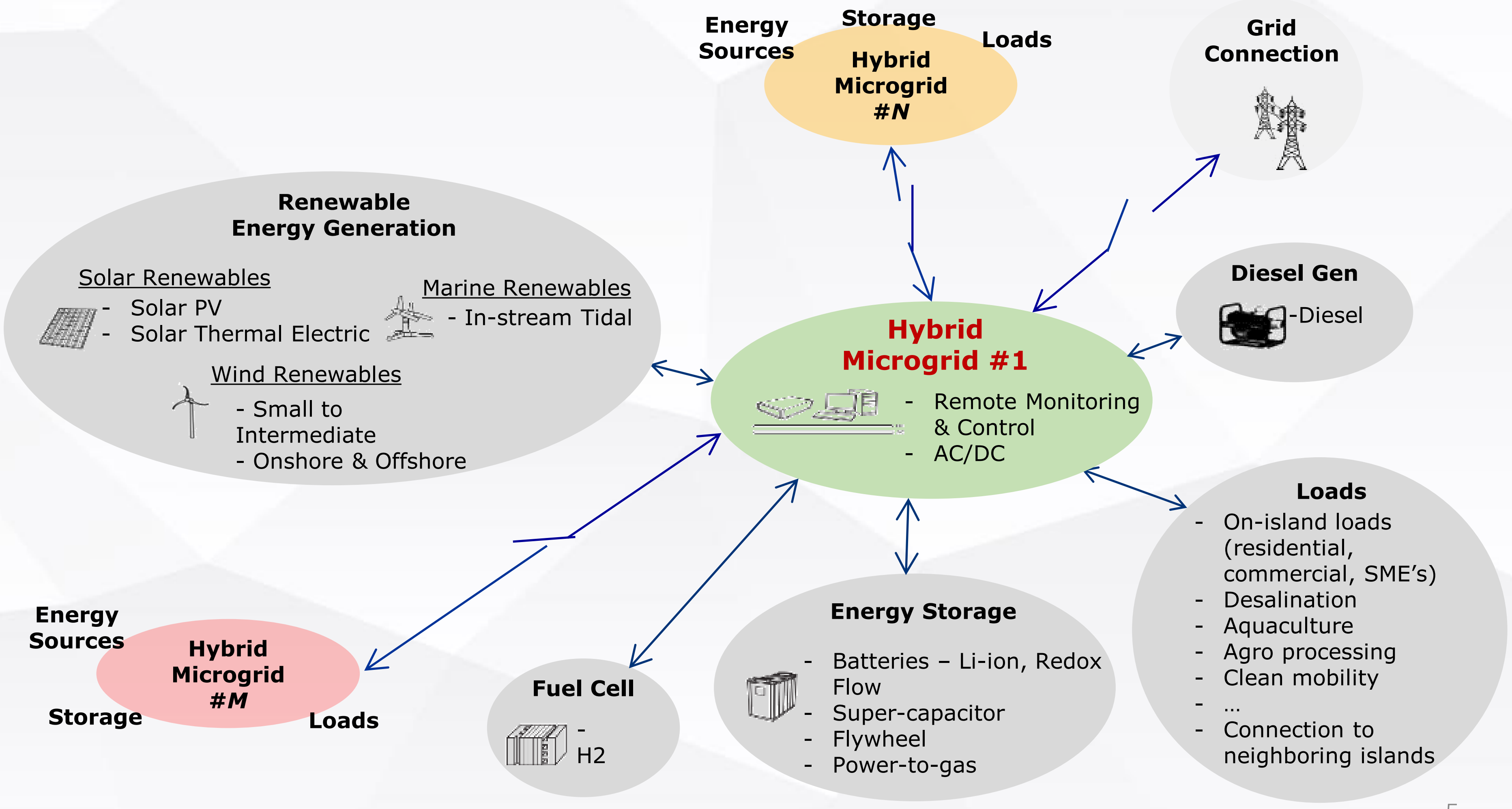
REIDS Roadmap and Framework

Phase I – 4 independent MGs (500kW-1MW each)
Phase II – 4 MGs in a cluster configuration (100kW-250kW each)



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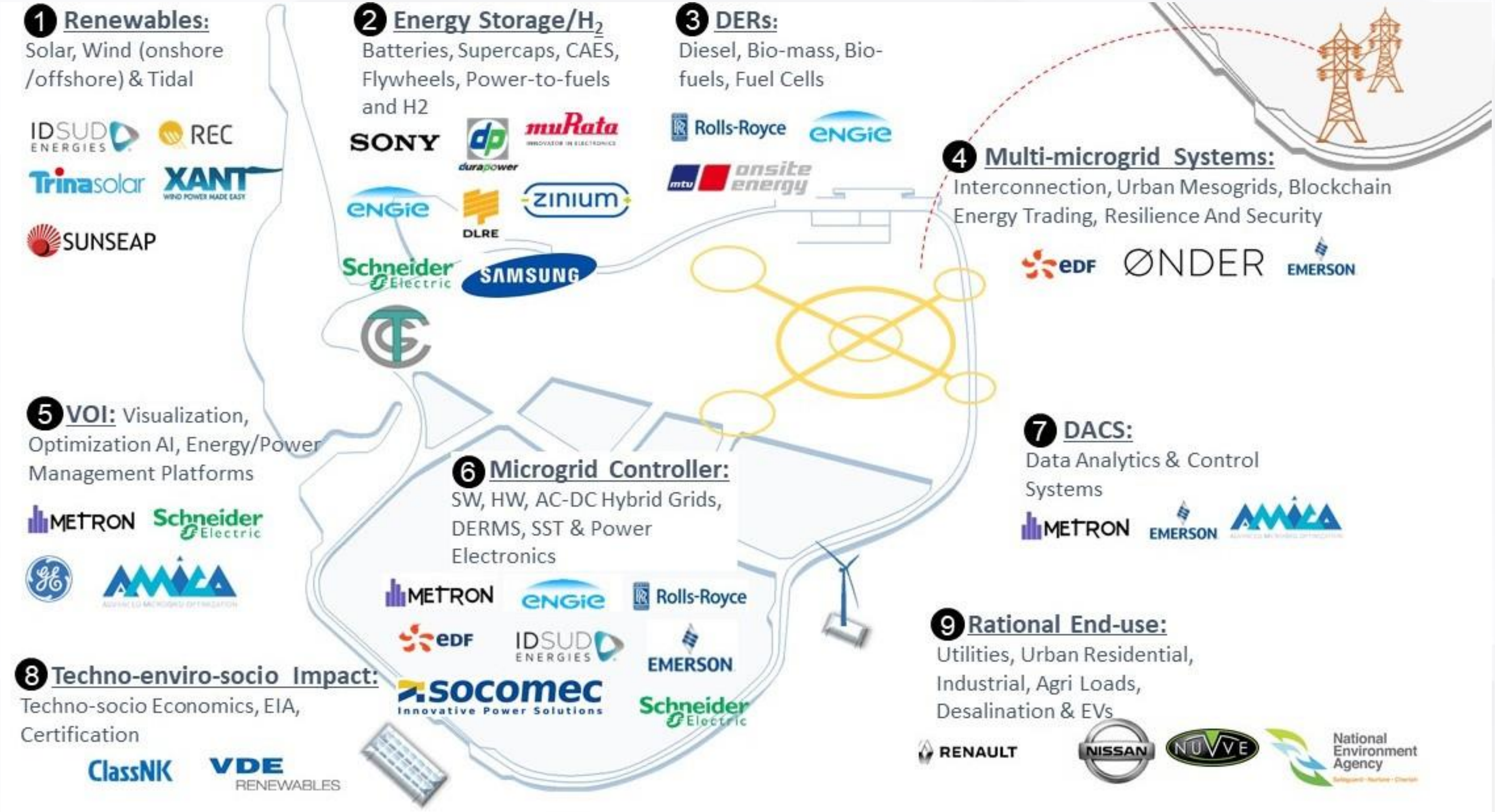
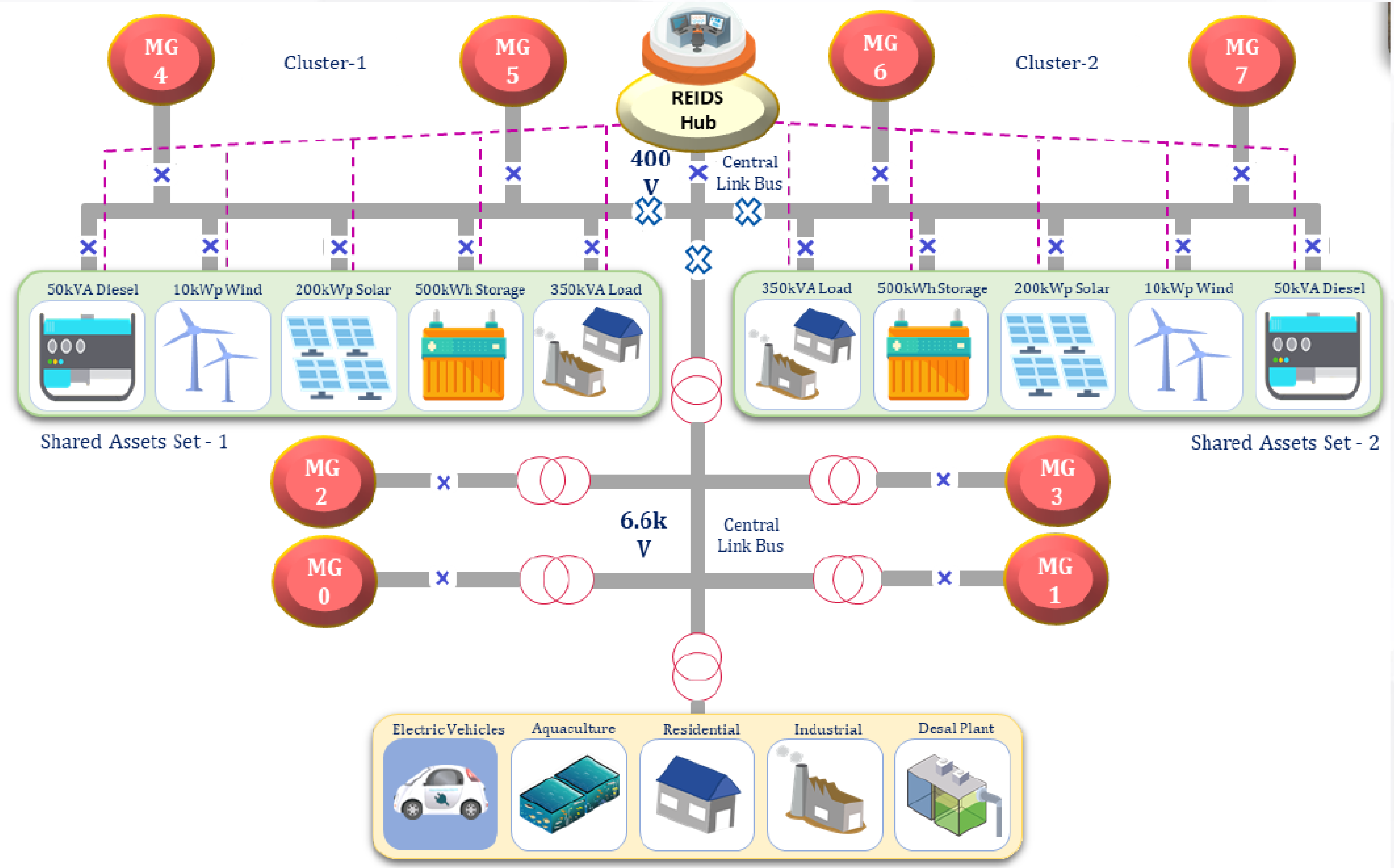
▪ Onboard Industry Collaborators



http://erian.ntu.edu.sg/REIDS/Pages/AboutREIDS.aspx

- REIDS Electrical Structure



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Onsite pictures

MG0 Test & Commissioning - March 2017

0. Outline

1. REIDS Project

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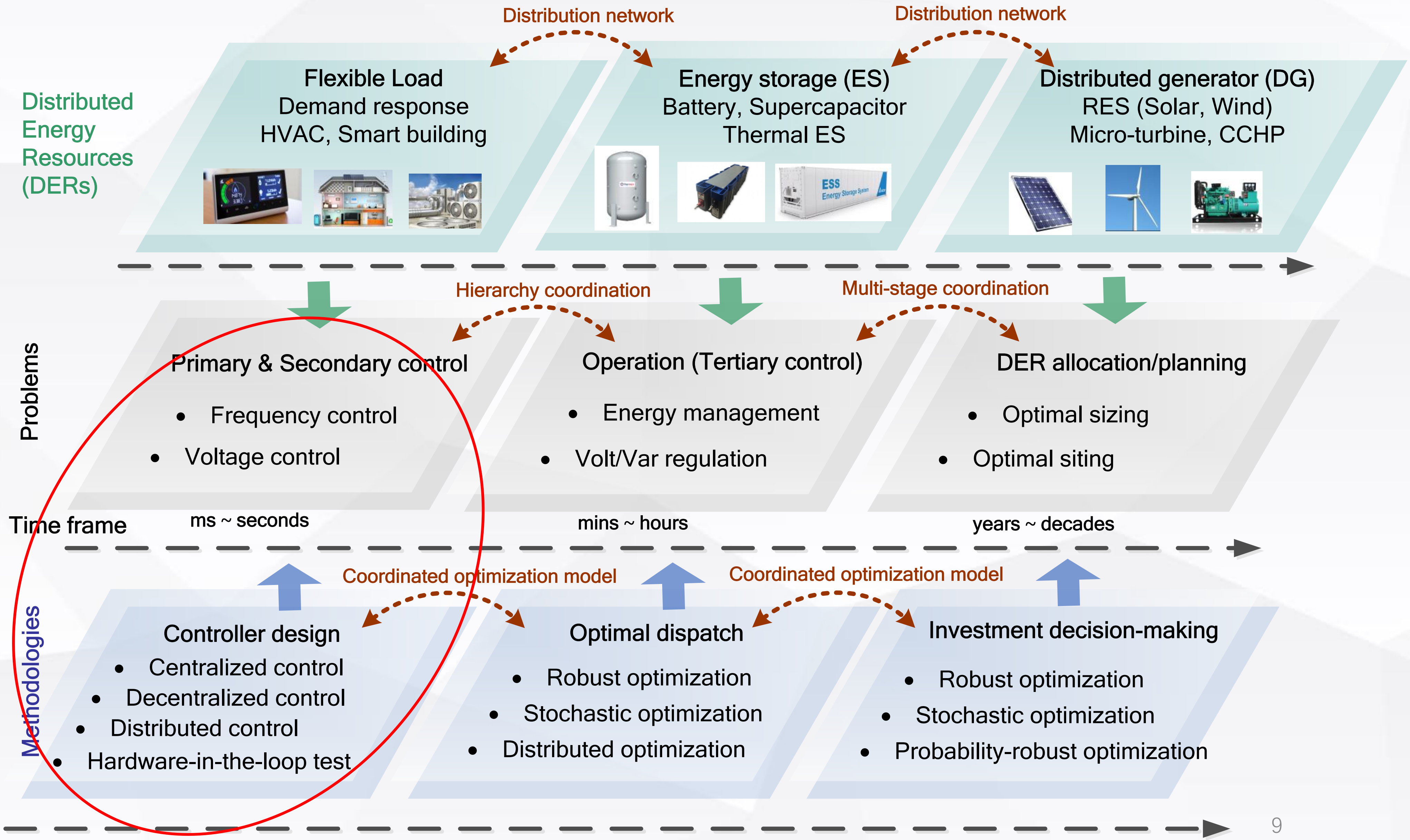
Our research Framework: system-level coordination of DERs



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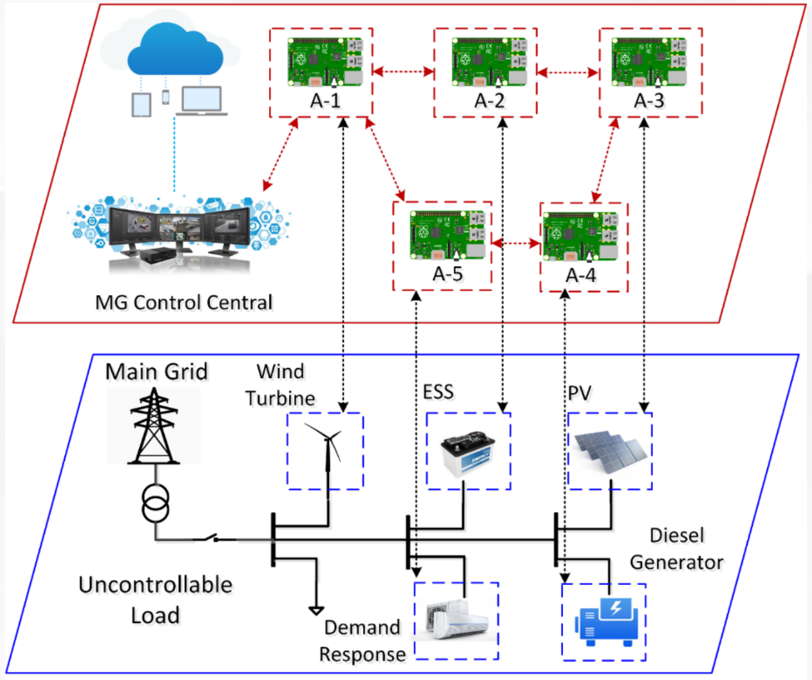
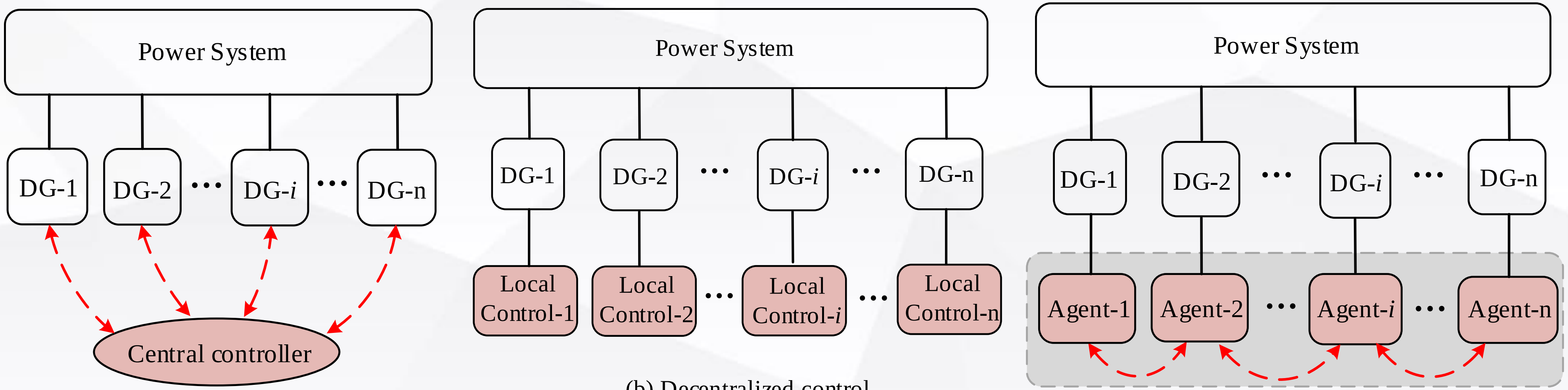
- Control of DERs in Microgrids



1. **Islanded mode:**
   - Distributed control (event-triggered, finite-time)
   - Hardware-in-the-Loop (Hil) validation

2. **Grid-connected mode:**
   - DER for *f* support
   - DER for *V* support



(a) Centralized control

(b) Decentralized control

(c) Distributed control

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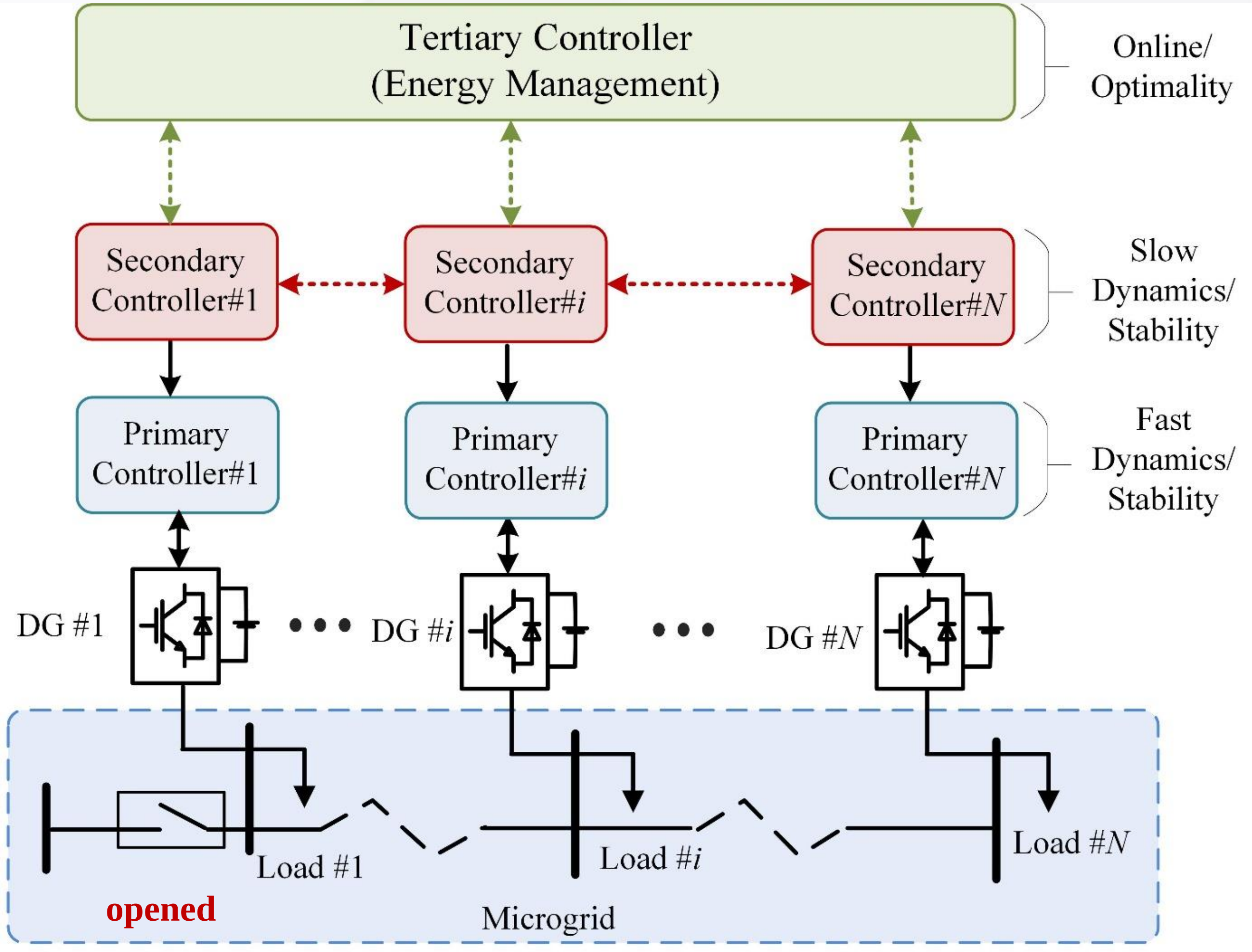
- Hierarchical control of an islanded microgrid



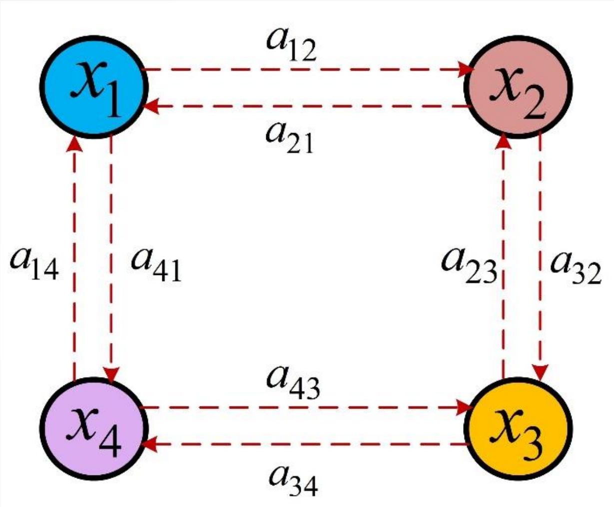
Hierarchical control framework of islanded microgrids

- **Tertiary control (centralized or distributed)**
  - Economic dispatch, optimal power flow.
- **Secondary control (centralized or distributed)**
  - V/f restoration and accurate power balancing
- **Primary control (decentralized)**
  - Inner control loops and droop control
  - Local V/f regulation and power sharing

- Distributed Control – Spatial Coordination of DERs

✓ No need for a central controller
✓ One node only communicates with neighbouring nodes
✓ Share communication and computation burden among nodes
✓ Higher resilience, plug-and-play, scalability, data privacy

Example of communication graph



Adjacent matrix of the graph

$$A = \begin{bmatrix} 0 & a_{12} & 0 & a_{14} \\ a_{21} & 0 & a_{23} & 0 \\ 0 & a_{32} & 0 & a_{34} \\ a_{41} & 0 & a_{43} & 0 \end{bmatrix}$$

a) Average consensus control

$$\dot{x}_i(t) = \sum_{j \in N_i} a_{ij}(t)(x_j(t) - x_i(t))$$

$$\lim_{t \to \infty} \left\| x_i(t) - x_j(t) \right\| = 0$$

b) Leader-follower consensus control

$$\dot{x}_i(t) = \sum_{j=1}^{n} a_{ij}(t)(x_j(t) - x_i(t)) + g_i(x_0(t) - x_i(t)).$$

$$\lim_{t \to \infty} \left\| x_i(t) - x_0(t) \right\| = 0$$

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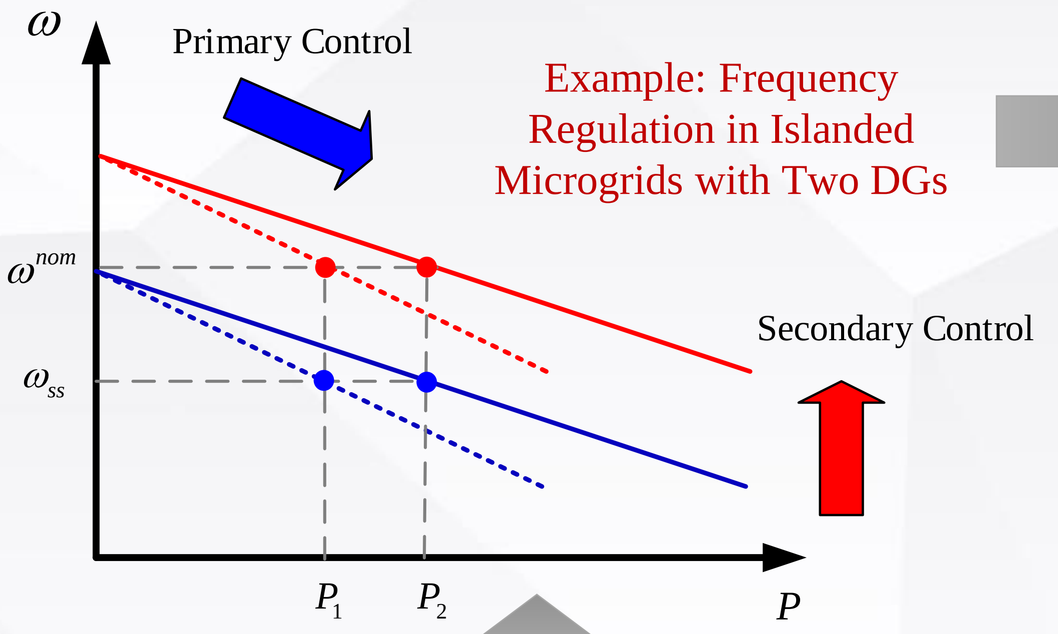
Secondary Controller Design – Principle



Example: Frequency Regulation in Islanded Microgrids with Two DGs

Droop control

$$\omega_i = \omega_i^{\text{nom}} - m_i^P P_i$$

$$V_i = V_i^{\text{nom}} - m_i^Q Q_i$$

Taking Derivative

$$\dot{\omega}_i = \dot{\omega}_i^{\text{nom}} - m_i^P \dot{P}_i$$

$$\dot{V}_i = \dot{V}_i^{\text{nom}} - m_i^Q \dot{Q}_i$$

Problem formulation

$$\omega^{\text{nom}} = \int (\dot{\omega}_i + m_i^P \dot{P}_i) dt = \int (u_i^{\omega} + u_i^P) dt$$

$$V^{\text{nom}} = \int (\dot{V}_i + m_i^Q \dot{Q}_i) dt = \int (u_i^V + u_i^Q) dt$$

Apply consensus control rule

$$u_i^{\omega} = \sum_{j=1}^{N} a_{ij} (\omega_j - \omega_i) + g_i (\omega^{ref} - \omega_i)$$

$$u_i^{p} = \sum_{j=1}^{N} a_{ij} (m_j^P P_j - m_i^P P_i)$$

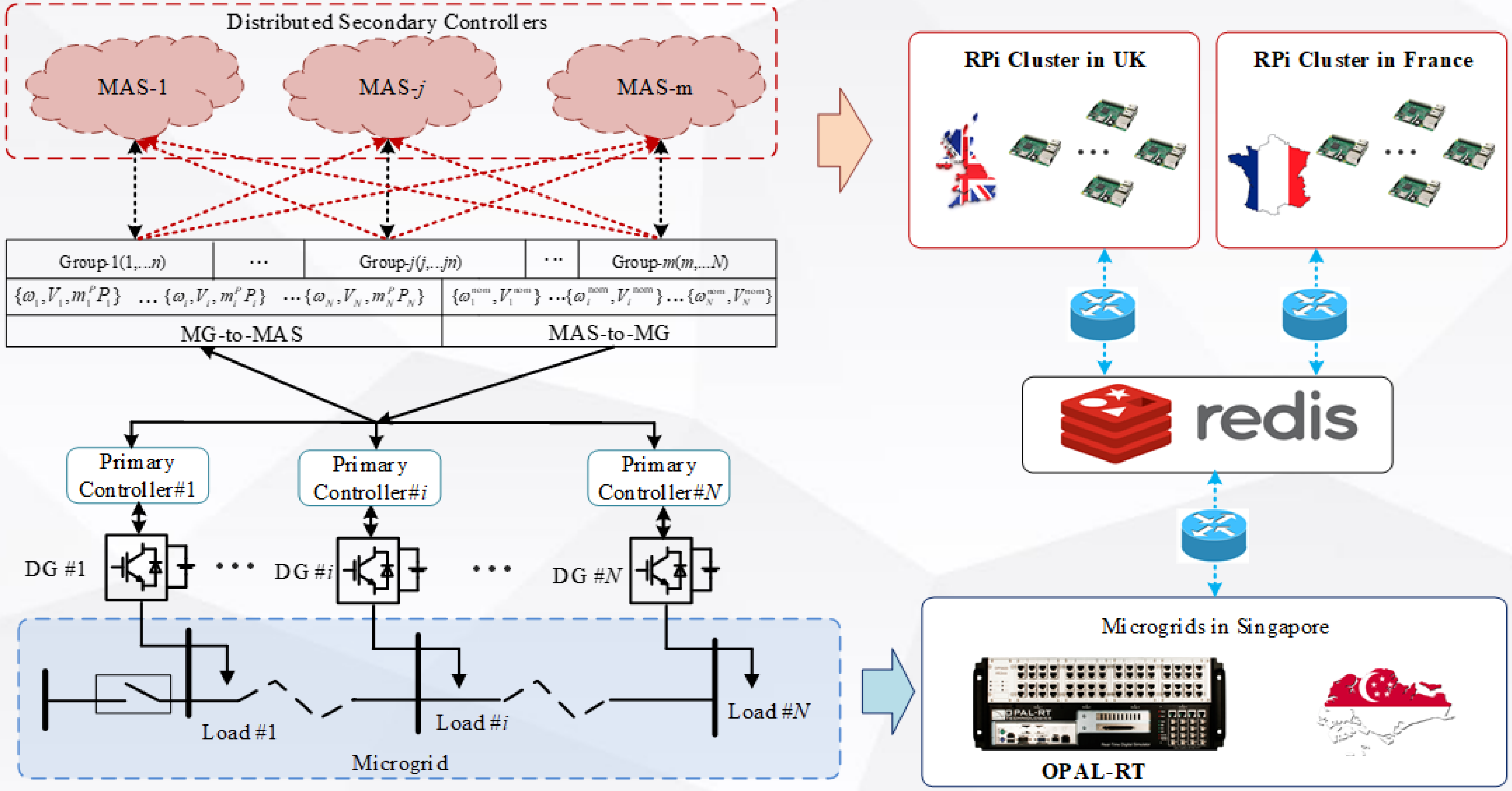
$$u_i^{V} = \sum_{j=1}^{N} a_{ij} (V_j - V_i) + g_i (V^{ref} - V_i)$$

$$u_i^{Q} = \sum_{j=1}^{N} a_{ij} (m_j^Q Q_j - m_i^Q Q_i)$$

▪ Cross-national hardware-in-the-loop (HiL) testbed

Jointly developed by NTU (Singapore), University of Strathclyde (UK), and G2E Lab (France)

- Microgrids system with OPAL-RT in Singapore.
- Distributed controllers in Raspberry Pi in UK and France.
- Software environment based on gRPC and data exchange via Redis cloud server.



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0. Outline

1. REIDS Project

2. Control

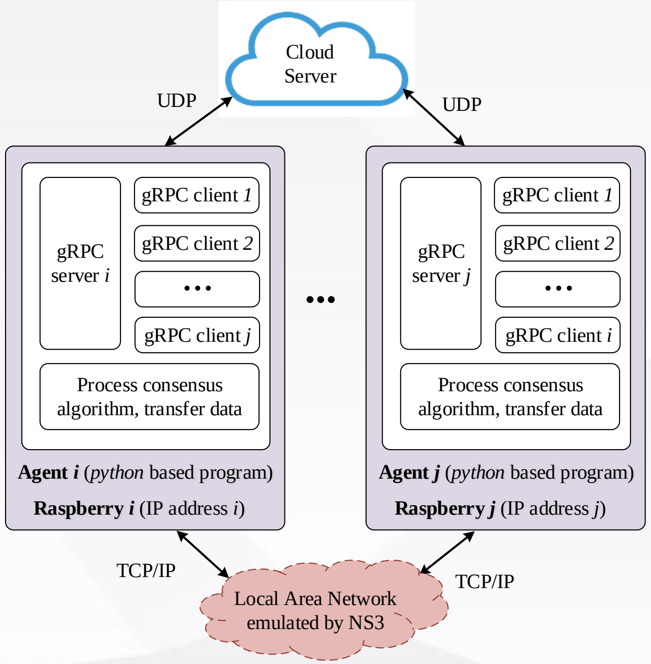
1) Islanded mode

2) Grid-tied mode

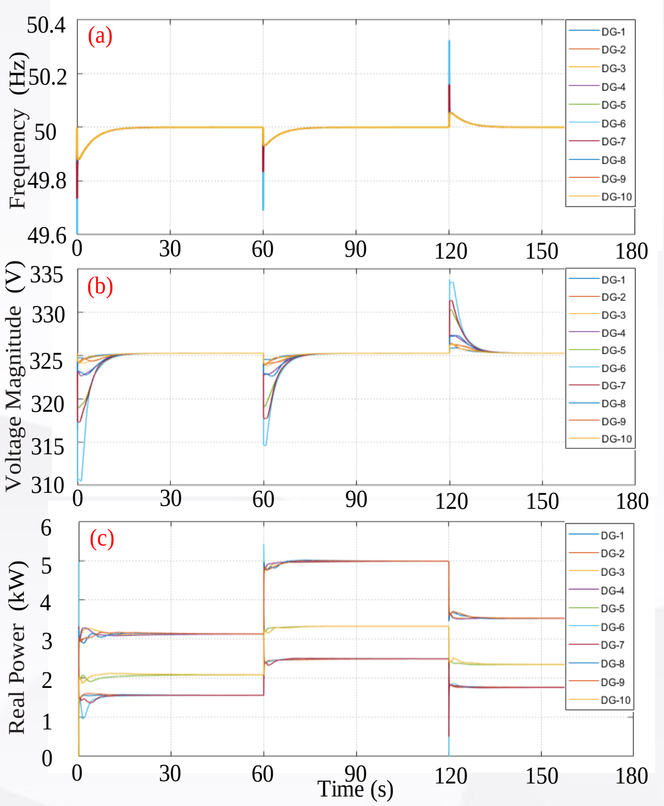
HiL Validation Results – Controller performance

Test system: 10-DG with two controller in UK and France (Each controller for 5 DGs)

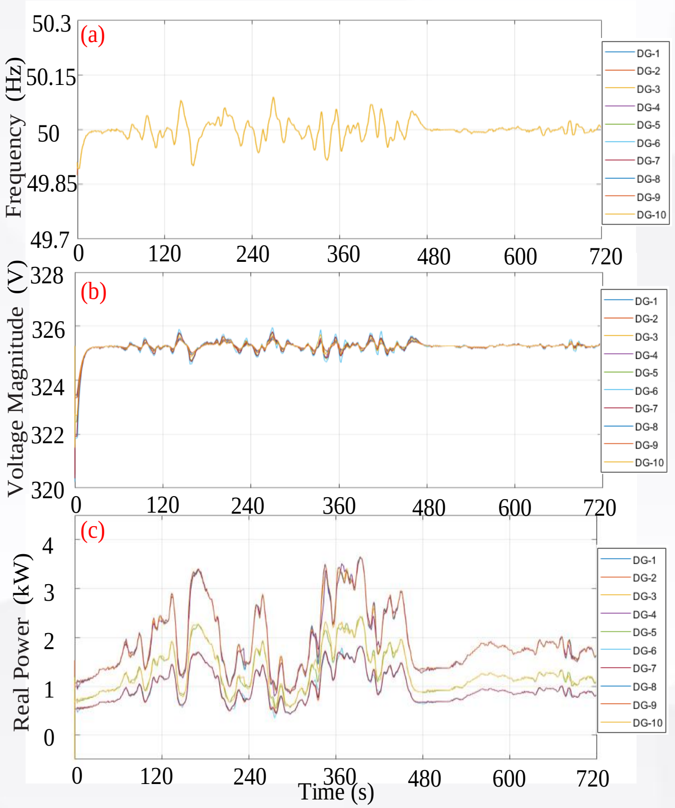
Structure of each agent based on gRPC



a) step load change case



b) Real PV and load profile case



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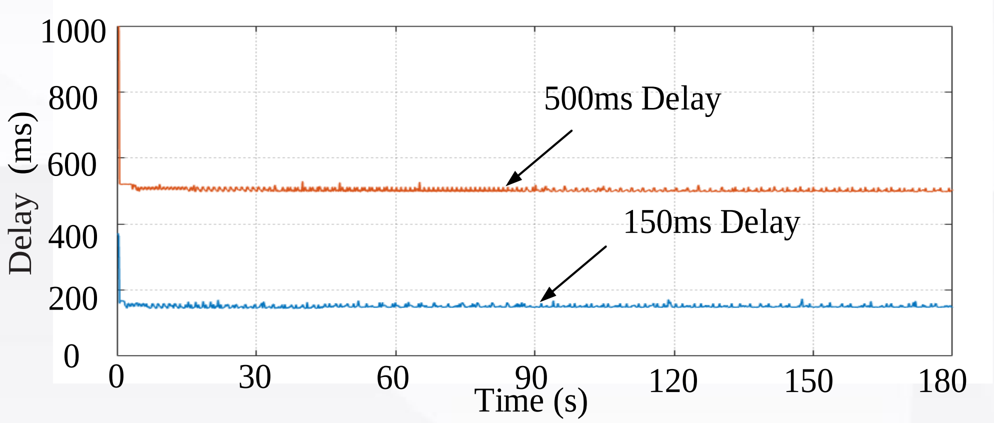
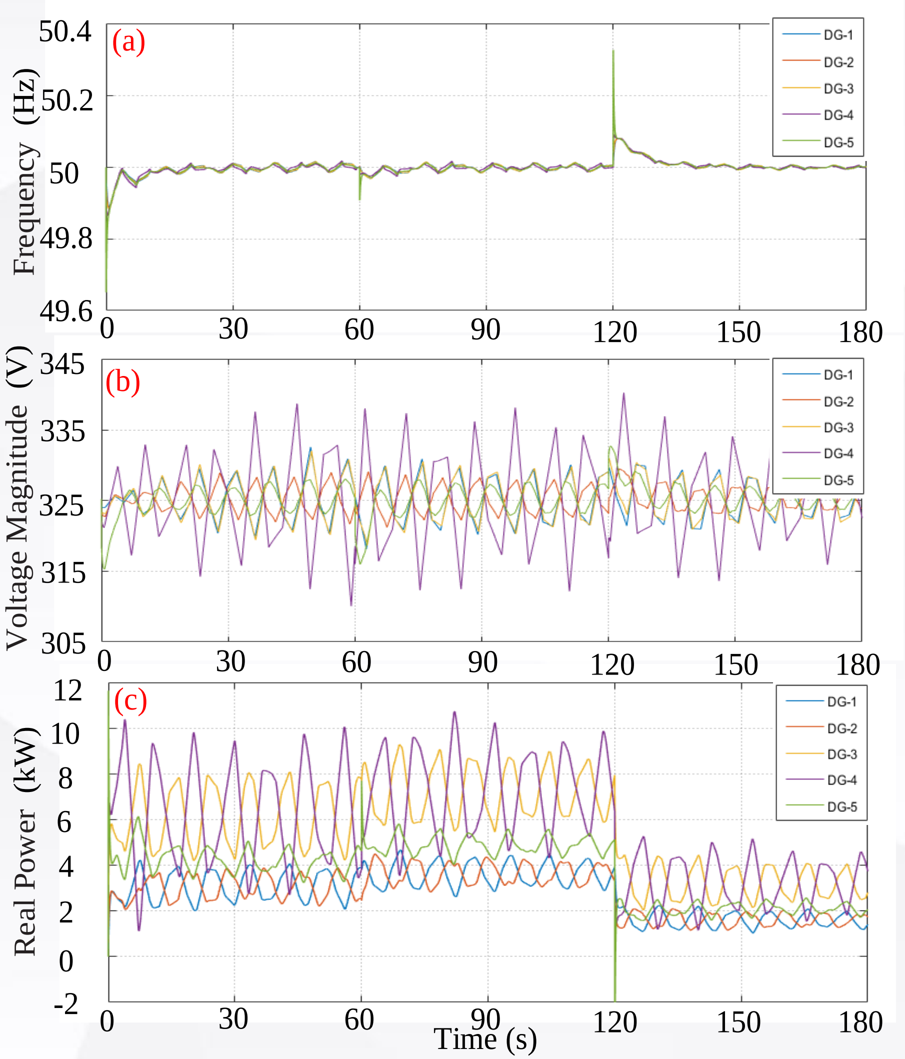
▪ HiL Validation Results – Communication delay

Communication delay emulated by NS3 simulation tools.



Test system: 5-DG MG with one MAS in UK



System oscillation under large delay, which can be mitigated by tuning the control gain.

- ✓ Larger control gain -> converge faster -> withstand smaller delay.
- ✓ Smaller control gain -> converge slower -> withstand larger delay

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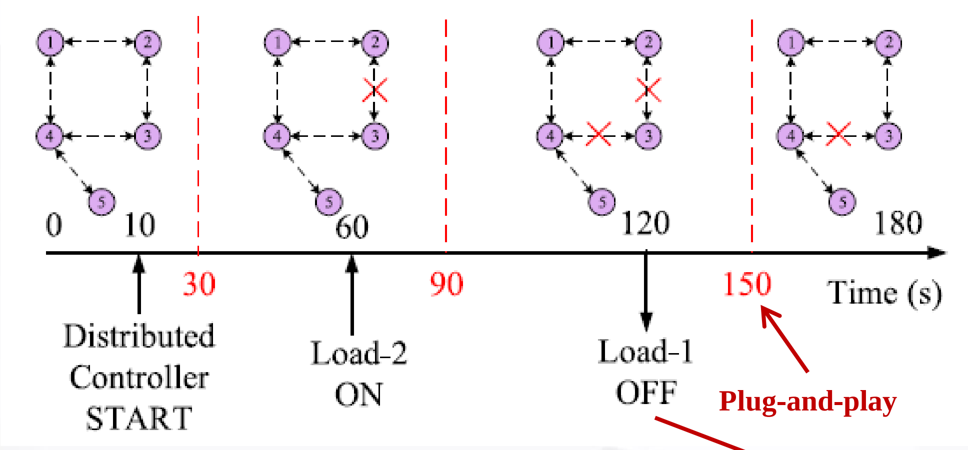
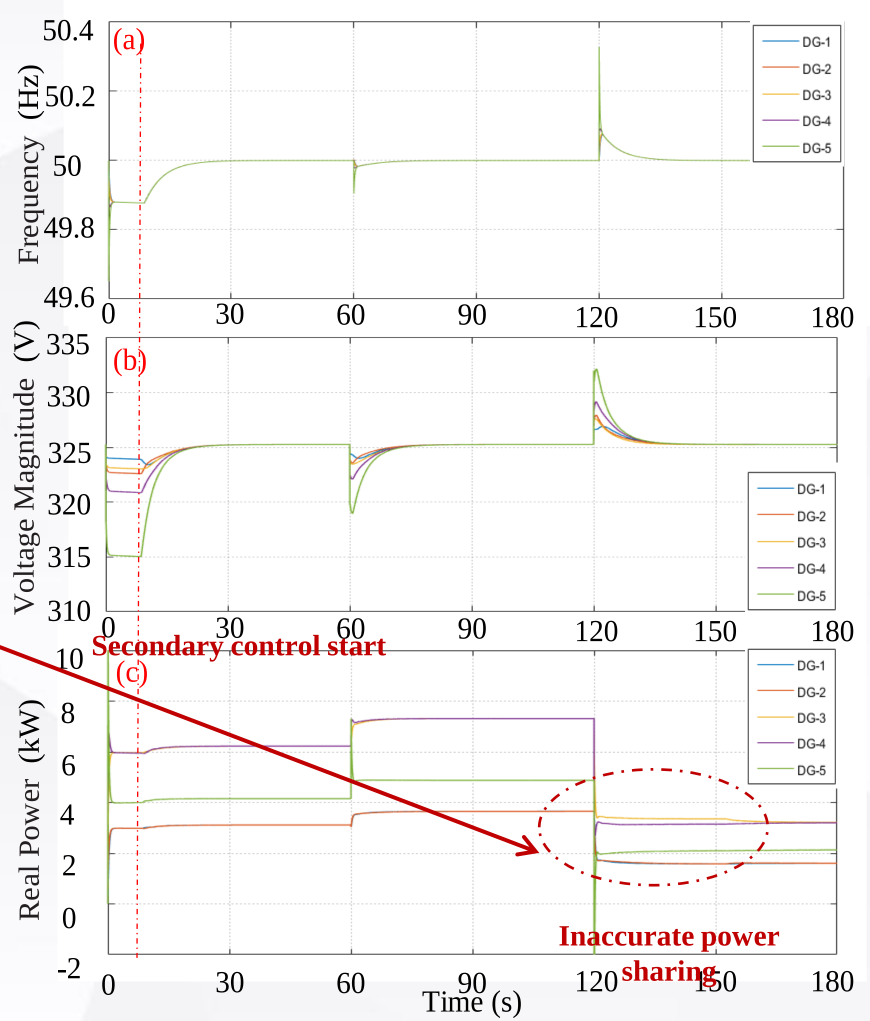
HiL Validation Results – Communication failures

Communication failures



Test system: 5-DG MG with one controller in UK



- ✓ Failure of communication will affect the convergence speed
- ✓ Loss of communication will lead to inaccurate power sharing

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- Grid-connected mode of Microgrids (DER support)

Voltage control support:

mitigate voltage deviation

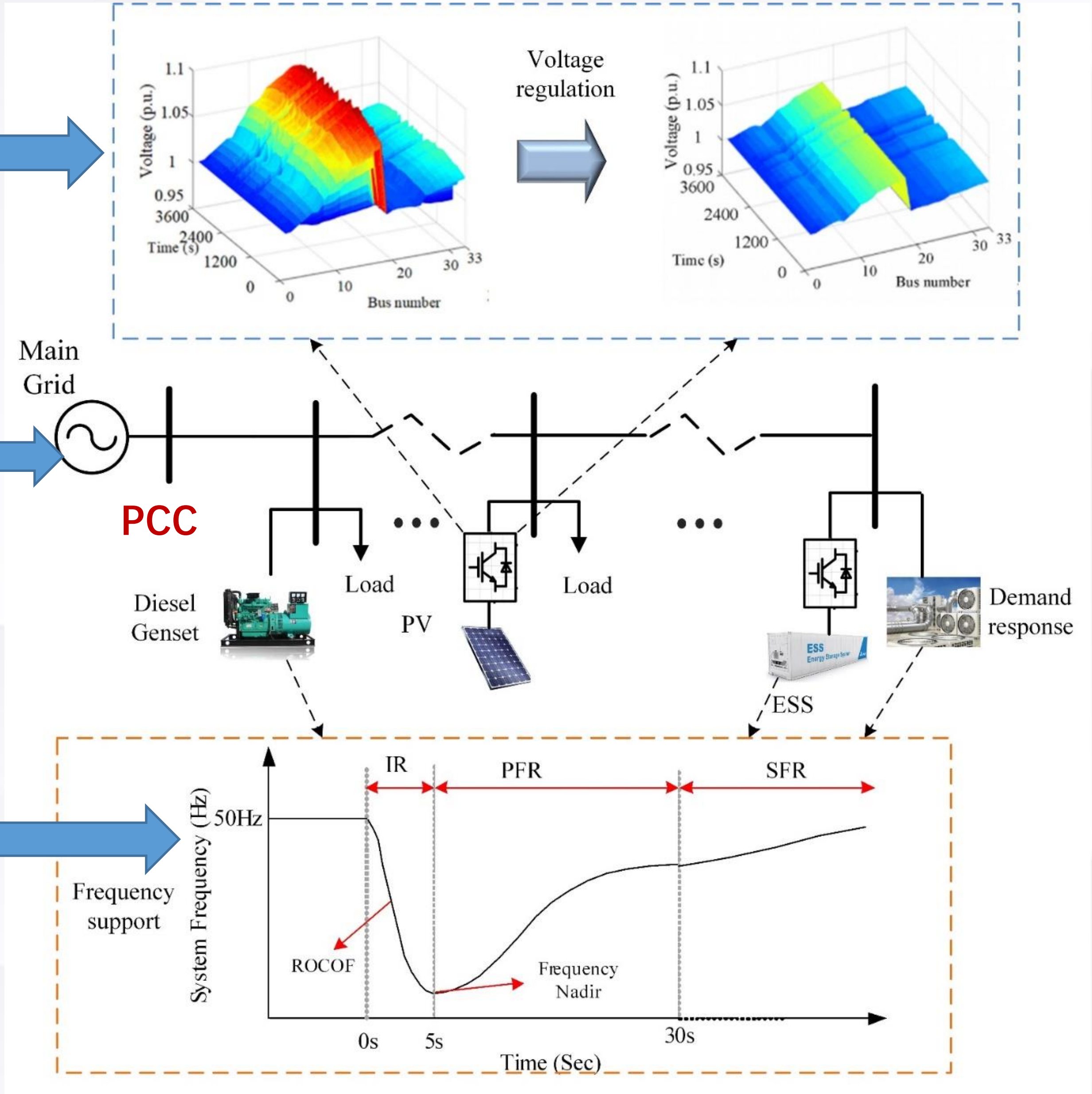
(seconds to minutes)

Frequency and voltage are dominated by the main grid through point of coupling connection (PCC).

Frequency control support:

mitigate frequency variation

(ms to seconds)



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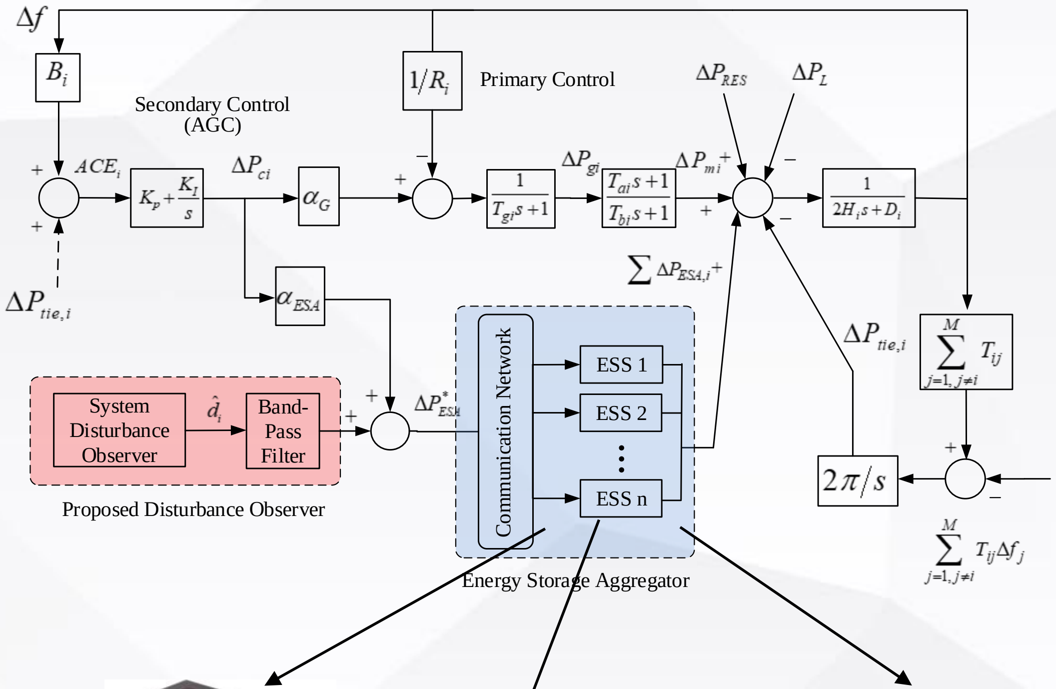
▪ Frequency Support from Aggregated Energy Storage

Proposed load frequency control (LFC) framework



$$\Delta \dot{f}_i(t) = -\frac{D_i}{2H_i}\Delta f_i(t) + \frac{1}{2H_i}\left(\Delta P_{mi}(t) - \Delta P_{L,i}(t) + \Delta P_{RES,i}(t) - \Delta P_{tie,i}(t) + \Delta P_{ESA,i}(t)\right)$$

$$\Delta \dot{P}_{mi}(t) = -\frac{1}{T_{bi}}\Delta P_{mi}(t) + \frac{1}{T_{bi}}\Delta P_{gi}(t) + \frac{T_{ai}}{T_{bi}}\Delta \dot{P}_{gi}(t)$$

$$\Delta \dot{P}_{gi}(t) = -\frac{1}{T_{gi}}\Delta P_{gi}(t) + \frac{1}{T_{gi}}\Delta P_{ci}(t) - \frac{1}{R_i T_{gi}}\Delta f_i(t)$$

LFC with primary control

$$\Delta \dot{P}_{tie,i}(t) = 2\pi \cdot \left[\sum_{j=1, j\neq i}^{M} T_{ij}(\Delta f_i(t) - \Delta f_j(t))\right]$$

Tie-line power flow

$$ACE_i(t) = B_i \Delta f_i(t) + \Delta P_{tie,i}(t)$$

$$\Delta P_{ci}(t) = -K_P ACE_i(t) - K_I \int ACE_i(t)$$

Secondary control

Lead acid battery

Lithium ion battery

• • •

Vanadium redox battery

Y. Wang, **Y. Xu***, Y. Tang, et al "Aggregated Energy Storage for Power System Frequency Control: A Finite-Time Consensus Approach," ***IEEE Trans. Smart Grid*, May 2018,**

0. Outline

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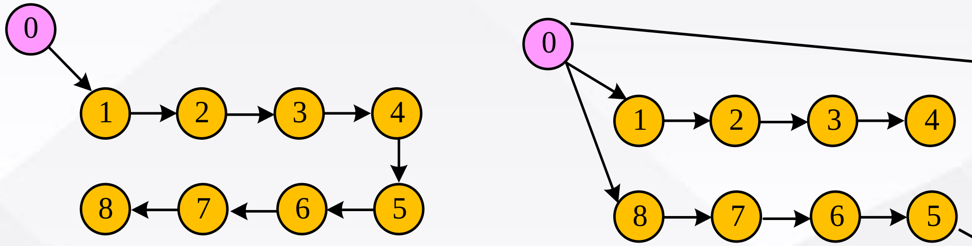
Frequency Support from Aggregated Energy Storage

Communication topologies of ESSs



(a) $\bar{\mathcal{G}}_1$ (b) $\bar{\mathcal{G}}_2$

Leader model

$$\begin{cases} \dot{e}_0(t) = K_{ESS}\, p_0(t) \\ p_0(t) = \dfrac{P^{*}_{ESA}(t)}{P^{max}_{ESA}} \end{cases}$$

LFC power reference

ESS model (follower)

$$\begin{cases} \dot{e}_i(t) = K_{ESS}\, p_i(t) \\ \dot{p}_i(t) = u_i(t) \end{cases}, \quad i = 1, 2..., N.$$

Matrices to describe graph

Adjacent Matrix

$$\boldsymbol{A} = [aij] \qquad a_{ij} = \begin{cases} 1, & \text{if } (v_i, v_j) \in \mathcal{E} \\ 0, & \text{otherwise.} \end{cases}$$

Pinning Matrix

$$\boldsymbol{G} = \text{diag}\{gi\} \quad g_i = \begin{cases} 1, & \text{if } \exists (v_i, v_0) \\ 0, & \text{otherwise.} \end{cases}$$

Proposed Control Law

$$u_i(t) = \sum_{j=1}^{N} a_{ij}(sig(e_i(t) - e_j(t))^{\alpha}) - g_i(sig(e_i(t) - e_0(t))^{\alpha})$$

Consensus SOC

$$-\gamma \sum_{j=1}^{N} a_{ij}(sig(p_i(t) - p_j(t))^{\beta}) - g_i(sig(p_i(t) - p_0(t))^{\beta})$$

LFC power reference

Control Objectives: achieve LFC power reference with consensus SOC

$$\lim_{t \to T_0} \|e_i(t) - e_0(t)\| = 0, \quad \lim_{t \to T_0} \|p_i(t) - p_0(t)\| = 0$$

$$e_i(t) = e_0(t), \quad p_i(t) = p_0(t), \quad \forall t \geq T_0, \quad i = 1, 2, ...N.$$

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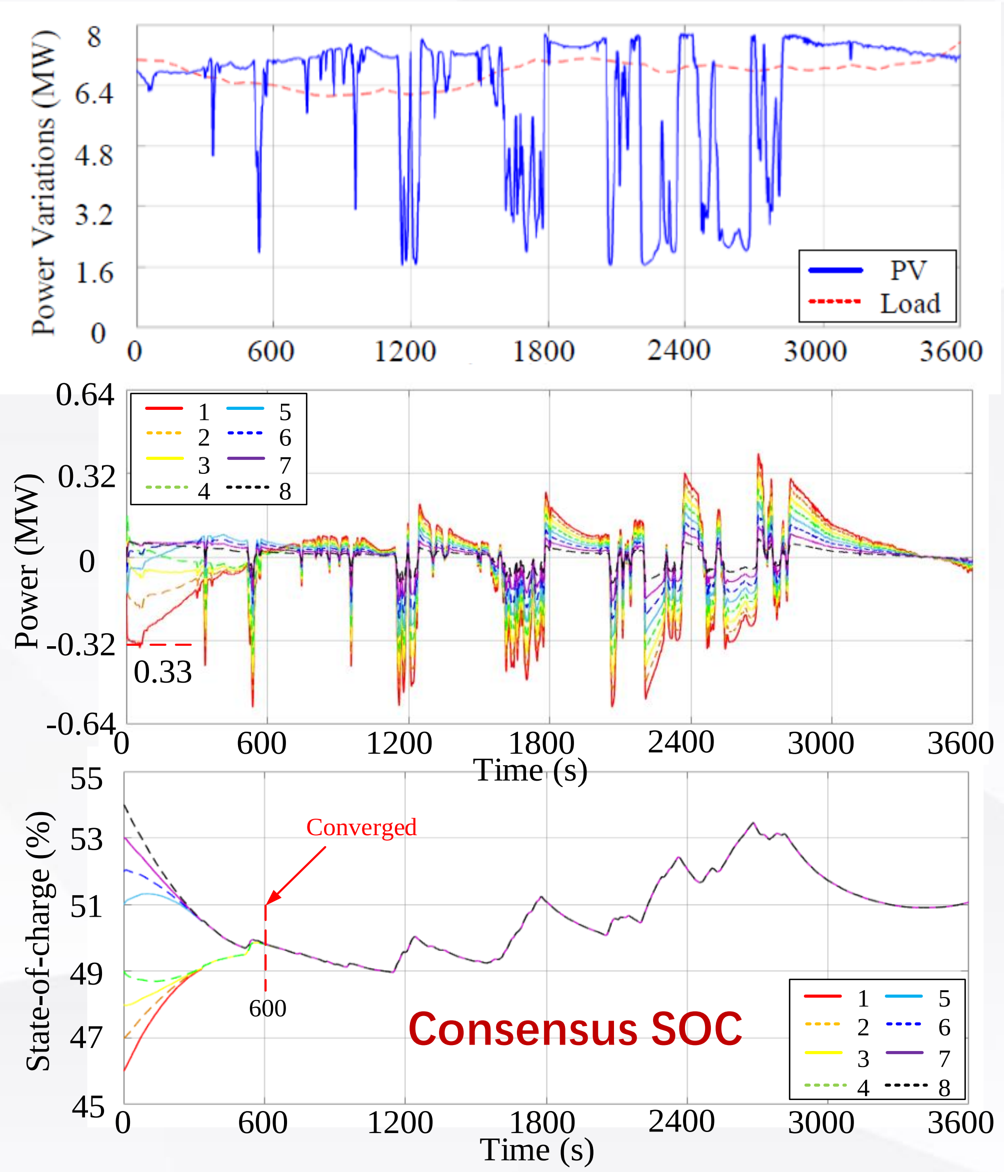
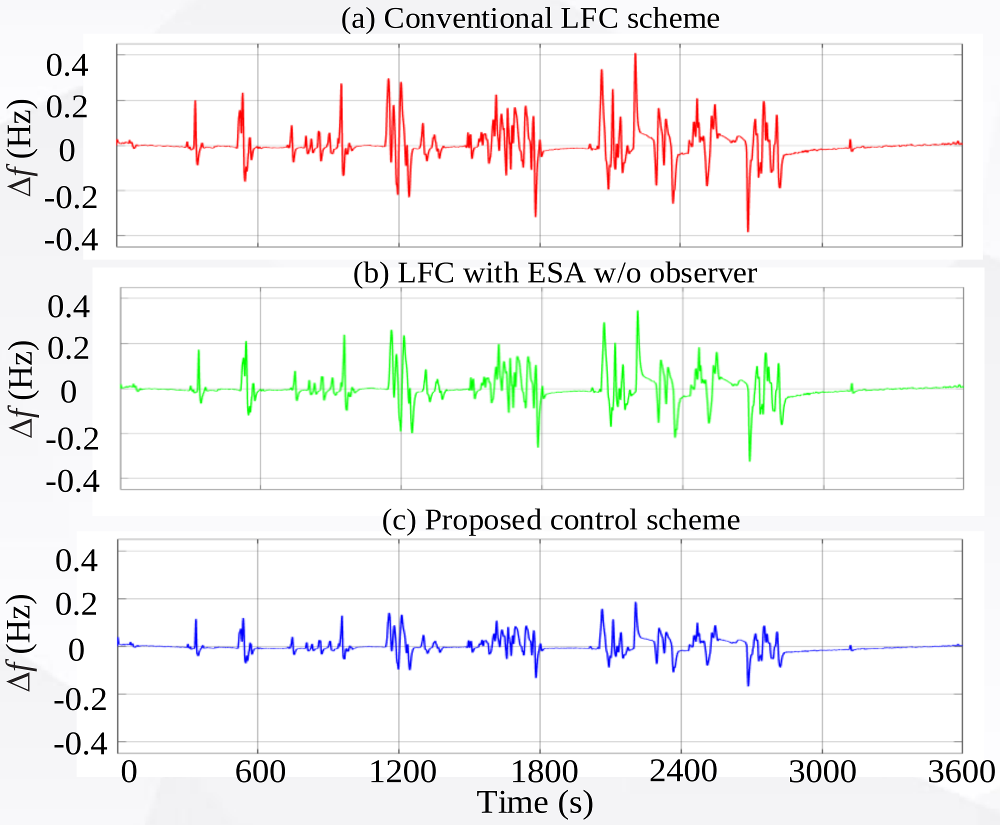
Simulation Results

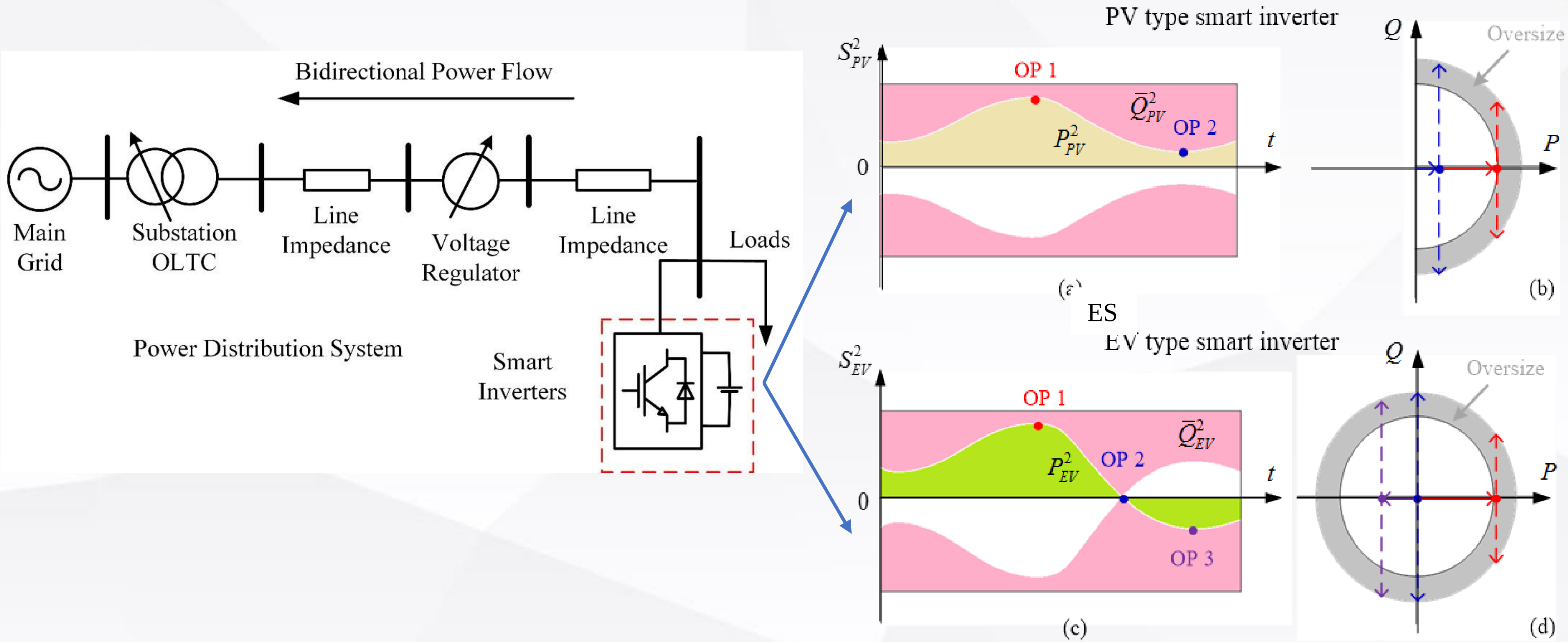




Y. Wang, **Y. Xu***, Y. Tang, et al "Aggregated Energy Storage for Power System Frequency Control: A Finite-Time Consensus Approach," ***IEEE Trans. Smart Grid, May 2018.***

- Real-time Voltage/Var Control (VVC) Support from DERs

- Existing Challenges: High PV penetration level, massive EV charging.
- Voltage quality issues: Voltage rise, drop and fast fluctuations.
- Potential solutions: inverter-assisted voltage/var support



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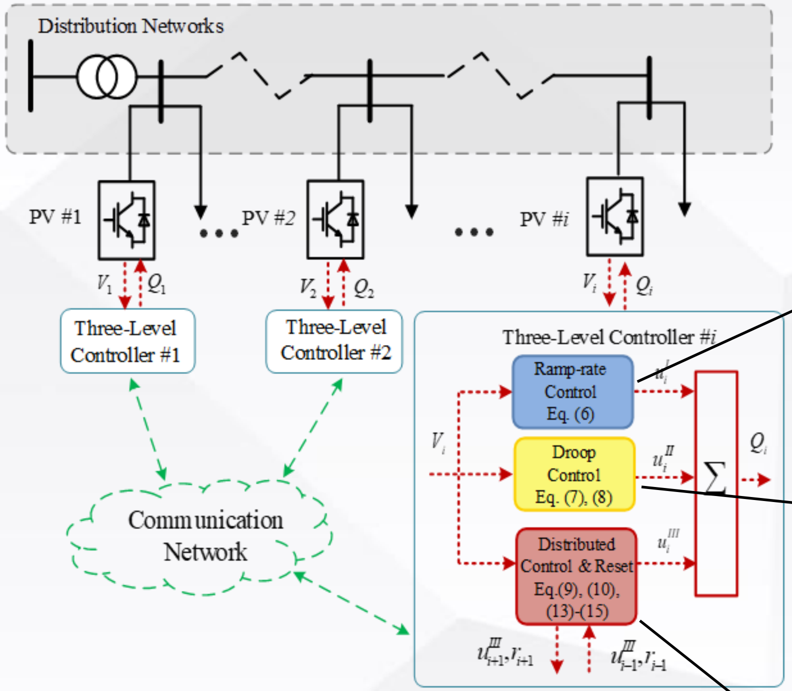
▪ Real-Time Coordinated Voltage/Var Control Controller



Controller design:

Level I: Ramp-rate Control -> smooth voltage fluctuation

$$u_i^I(t) = K_i^I\left[V_i(t) - \frac{\sum_{j=t-\omega}^{t} V_i(j)}{T(t) - T(t-\omega)}\right]$$

Level II: Droop Control -> immediate voltage support

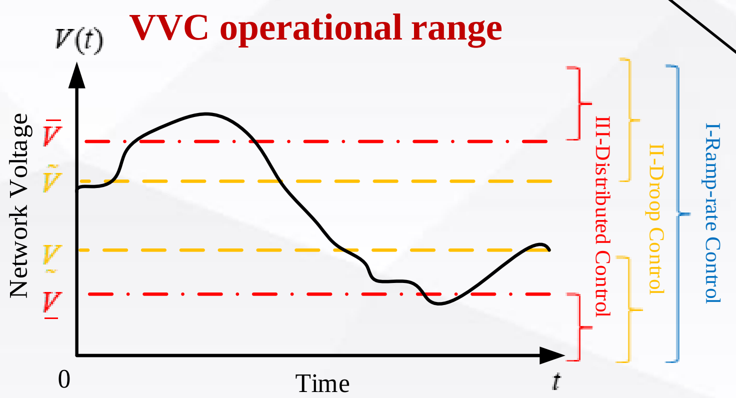
$$u_i^{II}(t) = \begin{cases} K_i^{II}(V_i(t) - \tilde{V}), & V_i(t) > \tilde{V} \\ 0, & \underset{\sim}{V} \le V_i(t) \le \tilde{V} \\ K_i^{II}(V_i(t) - \underset{\sim}{V}), & V_i(t) < \underset{\sim}{V} \end{cases}$$

Level III: Distributed Control -> voltage regulation to acceptable range

$$\dot{u}_i^{III}(t) = G_i^{III}\left[\sum_{i=1}^{N} a_{ij}(u_j^{III}(t) - u_i^{III}(t))\right] + e(t)$$

$$e(t) = \begin{cases} K_i^{III}(V_i(t) - \bar{V}), & V_i > \bar{V} \\ 0, & \underline{V} \le V_i \le \bar{V} \\ K_i^{III}(V_i(t) - \underline{V}), & V_i < \underline{V} \end{cases}$$

Dynamic consensus



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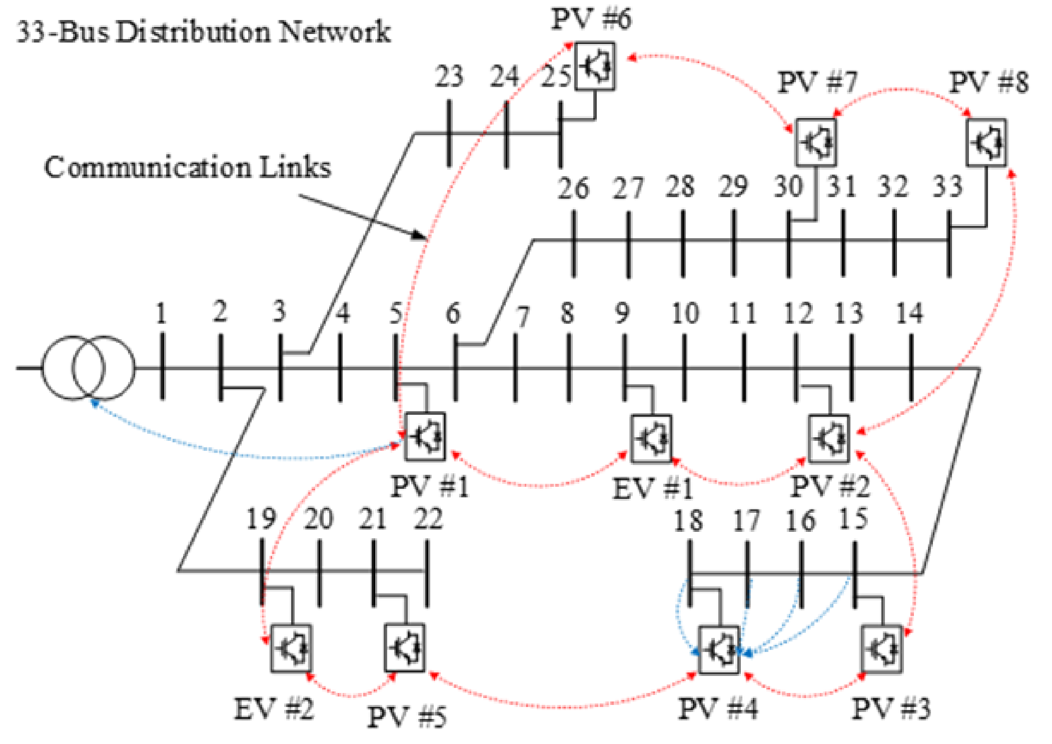
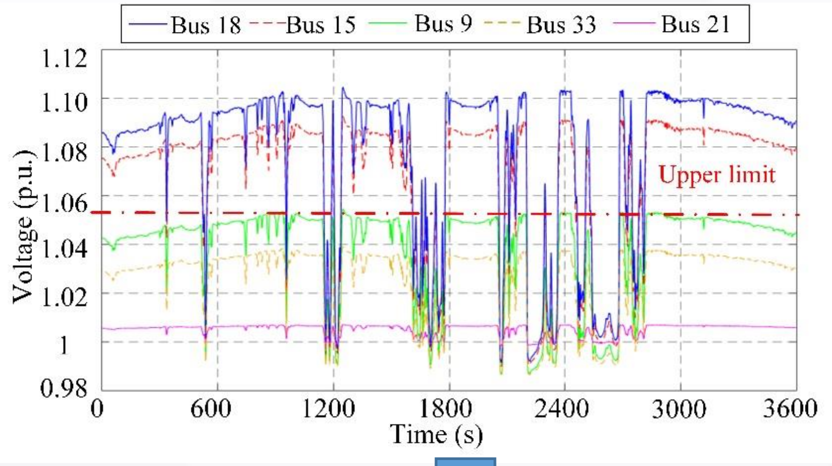
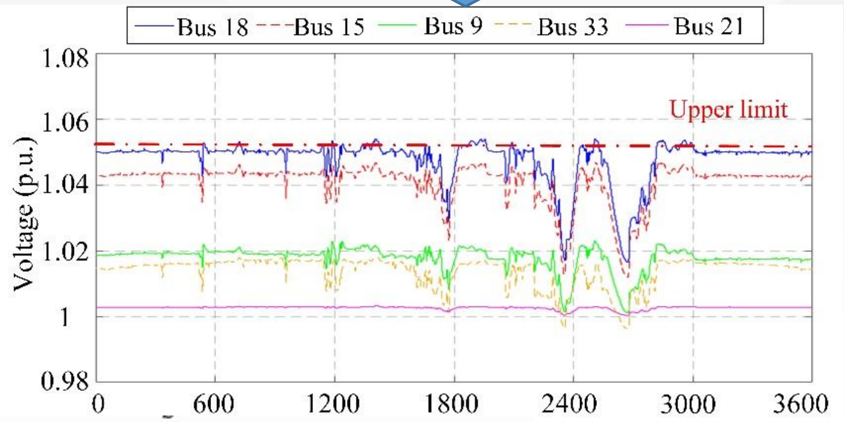
- Simulation Tests

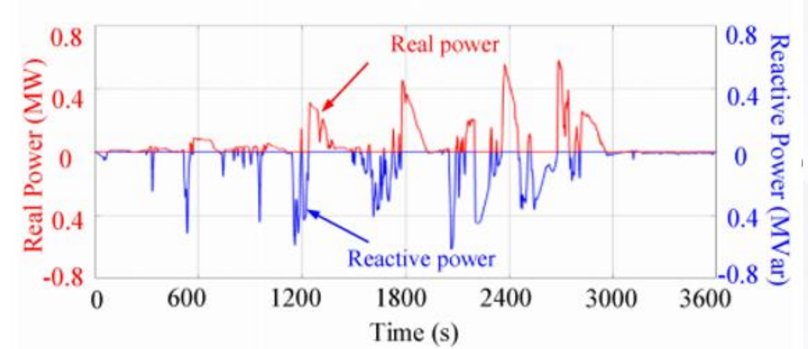


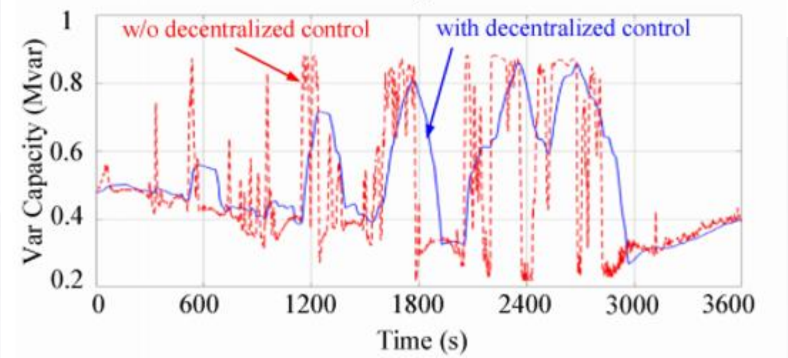
Real-time voltage/var control from inverters



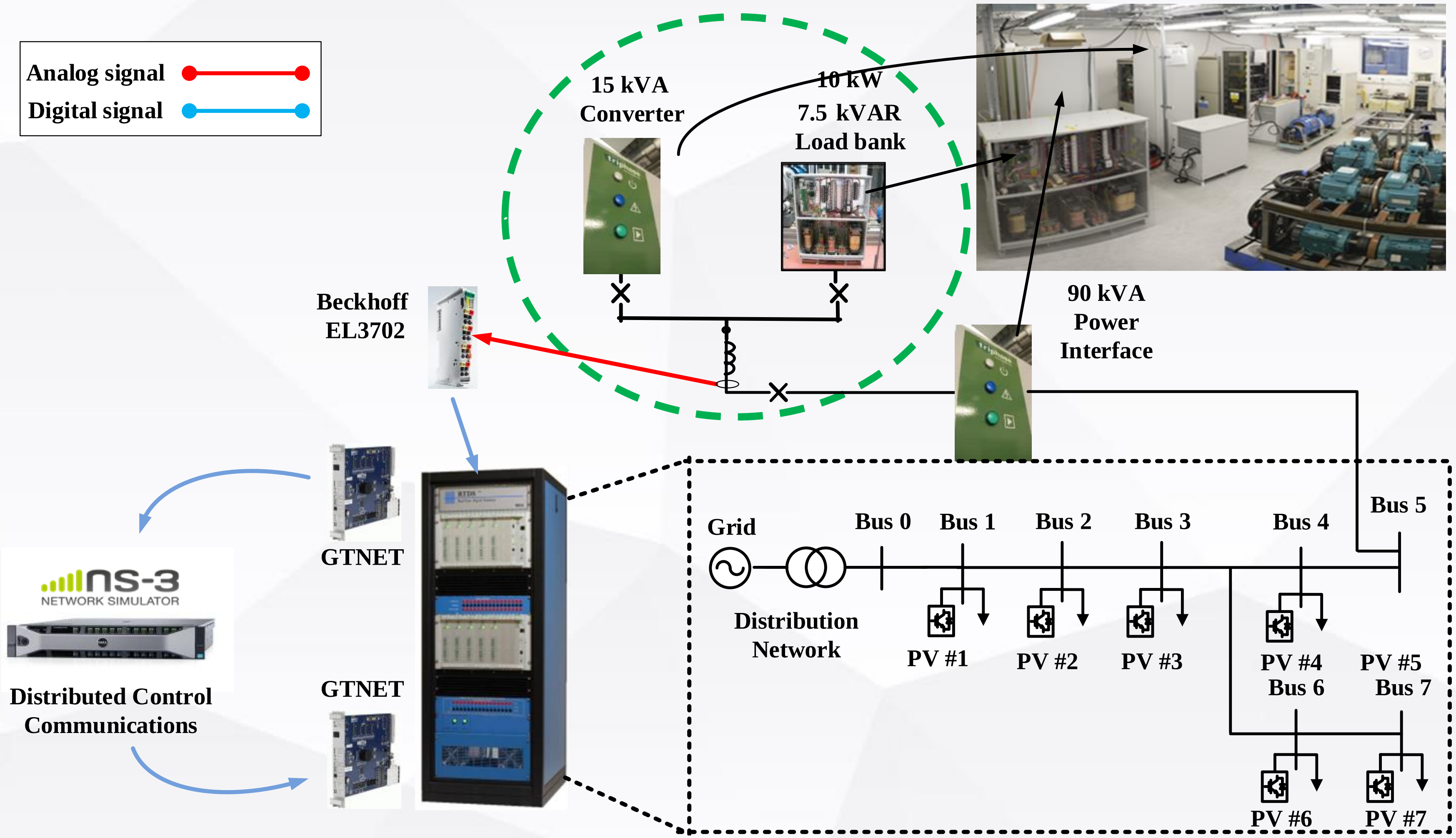


Effectiveness of ramp-rate control





▪ Power Hardware-in-the-Loop (PHiL) Test



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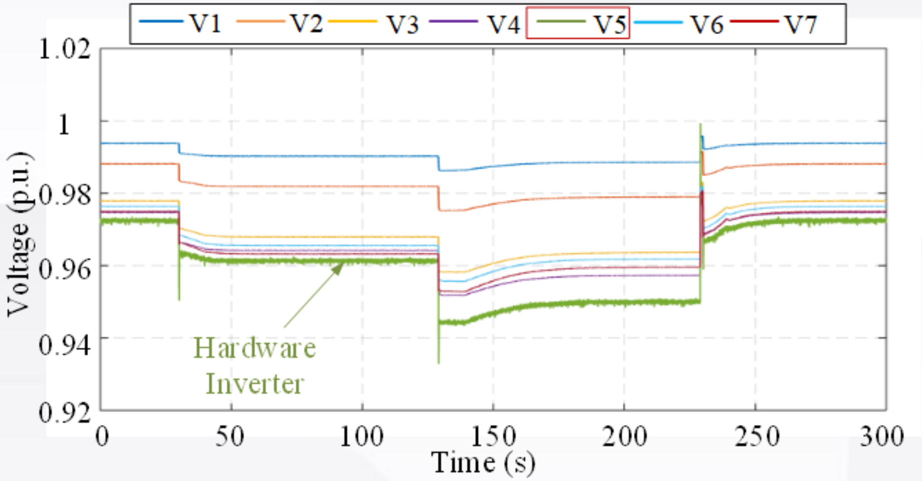
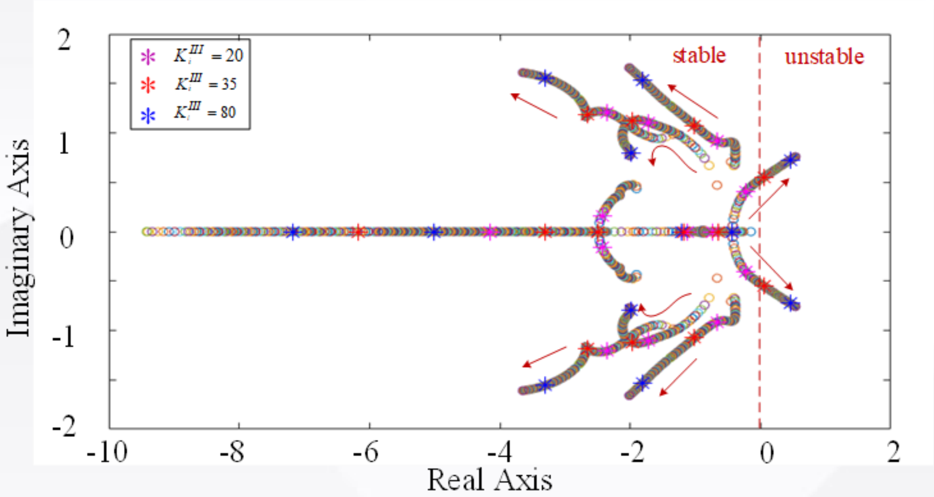
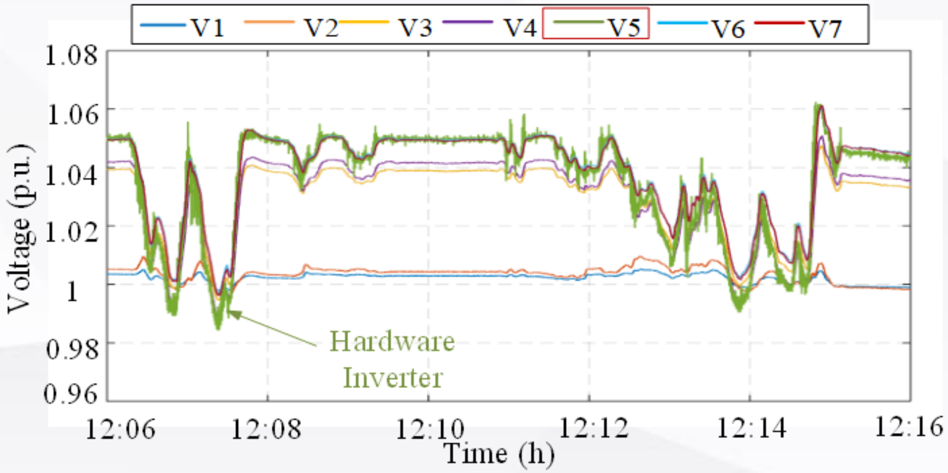
- Power HiL Results and Eigenvalues



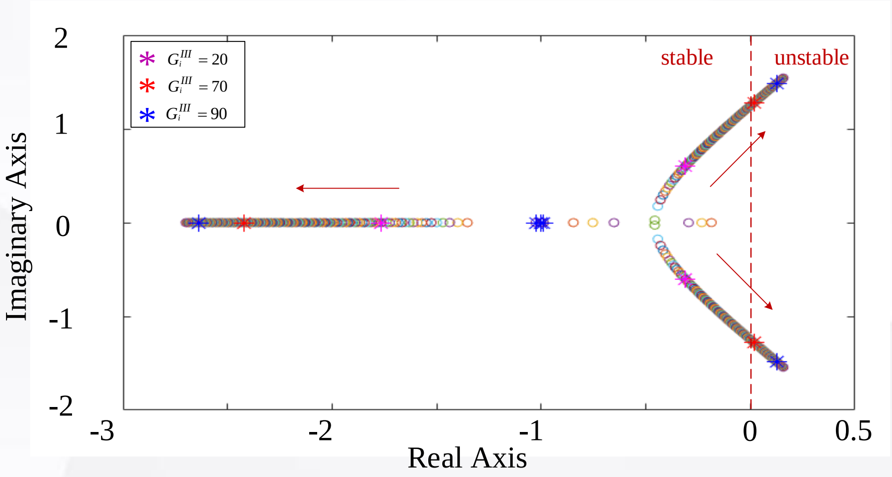
Voltage profiles under step load changes



Trace of eigenvalues under different control gains



Voltage profiles under real PV and load data



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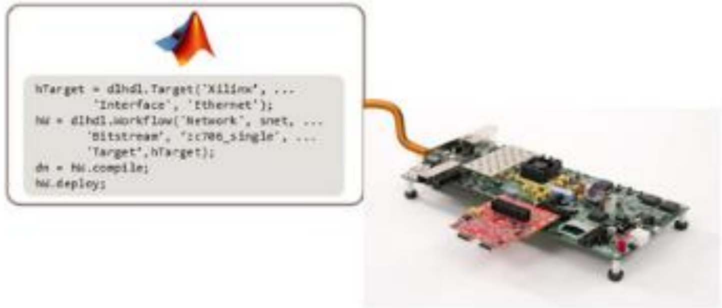

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