Self Healing Nano-Electronics for Nano-Spacecraft in Deep Space Missions

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Outline

- Introduction
- Design of Sustainable Electronics
- Pristine Device
- Damage and Recovery
- Applications
- Conclusions
Voyager into Interstellar Space

Voyager spacecraft is exploring where nothing from Earth has flown before.

*The NASA spacecraft, which rose from Earth on a September morning 40 years ago, has traveled farther than anyone, or anything, in history.*

Source: www.nasa.gov
Interstellar Missions

But, Voyager will end around 2025 due to power shutdown.

Source: www.nasa.gov
Journey to Alpha Centauri

- Alpha Centauri
  - The nearest star from Sun (4.37 light years)
  - The fastest spaceship takes 18,000 years.
Spacecraft-on-a-Chip: nano-spacecraft

- Theoretical speed is one-fifth of light speed.
- Interstellar mission can be possible in 20 years.
Nano-Spacecraft Technology

**CubeSat (Cal Poly, Stanford Univ.)**
- Directed energy interstellar study (UCSB)
- Wafer-scaled spacecraft
- Propulsion for interstellar exploration

*Source: www.nasa.gov*

**KickSat (Cornell Univ.)**
- Gyroscope
- Magnetometer
- Solar cells
- Microcontroller
- Antenna
- Radio


*Source: https://commons.wikimedia.org*
Technological Issues

- Lifetime of COTS* chips ~ 10 years
  ➔ Deep space mission > 20 years
- Limited radiation hardening strategy
  ➔ No flight path control and radiation shielding

*COTS: commercial off-the-shelf
Current Status

On earth,
repairing or replacing components is available with low cost and short time.

In space,
a service center is not available. Therefore, new technology such as self-healing process is required, which greatly saves cost and time for deep space exploration.
Important Features of CMOS

On Earth
- Reliability
- Performance

In Space
- Reliability
- Performance

- Focus on performance
  - High performance (HP)
  - Low operating power (LOP)
  - Low standby power (LSTP)

- Focus on reliability
  - Single-event effect (SEE)
  - Total ionizing dose (TID)
  - Displacement damage

Degradation Mechanisms

- Sources of device degradation
  - Radiation: high energy particle
  - Operation: electric field

Trapped charges

Interface states
Example of Annealing/Baking

![Diagram showing the process of annealing and baking in semiconductor materials]

→ **Damage recovery by thermal annealing**
On-Chip High Temperature Annealing of PMOS Dosimeter

Figure 1. PMOS RADFET surrounded by a serpentine poly-silicon resistor, $R=200\Omega$.

A. Kelleher et al., RADECS 95
Radically Extending the Cycling Endurance of Flash Memory

H.-T. Lue et al., IEDM 2012
Sustainable Space Electronics

Nano-heater (gate)

Silicon nanowire
gate-all-around FET

Damaged → Fresh

Trapped charges
Interface states

Thermal annealing

Demonstration of highly reliable logic transistor, high-speed DRAM, and Flash memory
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  – Silicon Nanowire Gate-All-Around FET
  – Built-in Nano-Heater

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Gate-All-Around (GAA) FET

Inherent structural advantages for radiation and self-healing process
Process Flow

Bulk substrate

Suspended SiNW by one-step etching route
- Sacrificial oxidation
- Oxide dep. and CMP*
- Partial oxide etching (STI**) and CMP
- Thermal oxidation
- In-situ n⁺ poly-Si dep.
- Poly-Si CMP and HM*** dep.
- Dual pads gate patterning
- Spacer formation
- S/D implantation
- RTA**** and H₂ annealing

*CMP: chemical mechanical polishing, **STI: shallow trench isolation,
***HM: hard mask, ****RTA: rapid thermal annealing
Formation of Suspended SiNWs

- **Suspended SiNW**: basic building block for GAA FETs
- **Previous approaches**: SOI substrate and epitaxial growth
  - CMOS low-compatible, high cost, and low throughput
SiNW by One-Step Etching Route

Deep Si etching

Polymer

PR $\text{C}_4\text{F}_8$

Bulk-Si

PR $\text{SF}_6$

Bulk-Si

*PR: photo-resist

Anisotropic etching

Scallop

Isotropic etching

500 nm

10 μm

Anisotropic etching

Polymerization (passivation: $\text{C}_4\text{F}_8$)

Isotropic etching ($\text{SF}_6$)
SiNWs from a Bulk Substrate

CMOS compatible one-step etching route

D.-I. Moon et al., IEEE EDL 32 (4)
Highly scaled SiNW GAA FET on a bulk substrate
- Gate length \((L_G) = 30 \text{ nm}\), SiNW diameter \((D_{NW}) = 15 \text{ nm}\)
- Gate dielectric: thermal oxide, O/N/O stacks
Built-in Nano-Heater

Dual contact pads
Current ↑ →
Temperature ↑

Current heating
Gate
S
D

Current, I (mA)
0.0
0.3
0.6
0.9

Voltage, V (V)
0
1
2
3
4
5
6
7

Temperature (°C)
0
200
400
600
800
1000
1200
1400
1600

Breakdown
Healing
Measurement
Simulation
Electro-Thermal Simulation

Temperature by the nano-heater > 900 °C, 10 ns
Heat transfer from the gate to the dielectric
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• Introduction
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• Pristine Device
  – Electrical Characteristics
  – Short-Channel Effects

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Electrical Characteristics

- Silicon nanowire gate-all-around FET on a bulk substrate
  - DIBL: 150 mV/V, SS: 87 mV/dec, $I_{ON}/I_{OFF} > 10^6$

D.-I. Moon et al., IEEE EDL 32 (4)
Short-Channel Effects (SCEs)

Excellent immunity against SCEs despite the device built on a bulk substrate → GAA structure with SiNW channel

D.-I. Moon et al., IEEE EDL 32 (4)
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  – Radiation Aspect
  – Operation Aspect

• Applications
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Total Ionizing Dose (TID)

- **Semi-permanent device degradation** caused by radiation-induced fixed charge and interface trap

- **Representative phenomena**
  - Threshold voltage shift
  - Increment of subthreshold swing
  - Reduction in on/off current ratio

- **Accumulated damage according to cumulative radiation dose**

TID in SiNW GAA FETs

$\gamma$-ray by $^{60}$Co source
Dose rate = 460 rad/s

$\Delta V_T$ (mV)

$\Delta S_S$ (mV/dec)

$L_G$ (nm)

30 50 70 90

Total dose = 5 Mrad
(SiO$_2$)

$\Delta S_S$ (mV/dec)

0 2 4 6

0 2 4 6 8 10

Total dose (Mrad)

$L_G$ = 30 nm

$V_T$, $S_S$, and $I_D$ degradation

$L_G \downarrow \Rightarrow$ TID effect $\uparrow$

Total dose $\uparrow \Rightarrow$ TID effect $\uparrow$
Recovery of TID Damages

Healing conditions: ± 2 V for 200 ms
Complete recovery of $V_T$, SS, and $I_D$
Single Event Effect (SEE)

- **Non-destructive malfunction (transient):** soft faults
  - Single-event upset (SEU)
  - Single-event transient (SET)
  - Single/multiple Bit Upsets (S/MBU)
  - Single-event functional interrupt (SEFI)

- **Destructive malfunction:** hard faults
  - Single-event upset (SEU)
  - Single-event burnout (SEB)
  - Single-event gate rupture (SEGR)

- **Hardening techniques**
  - Dual interlocked storage cell (circuit-level)
  - Error detection and correction (system-level)

Structural Dependence

Electron-hole pair generation by radiation
Number of gates $\uparrow \Rightarrow$ Leakage current $\downarrow$
SEE of SiNW GAA FET

Scaling: $D_{NW} \downarrow \Rightarrow$ SEE $\downarrow$ vs. $L_G \downarrow \Rightarrow$ SEE $\uparrow$

Floating body of GAA $\Rightarrow$ bipolar effect

*LET: linear energy transfer
**Single Transistor Latch (STL)**

Device degradation by latch

Removal of hot carrier stress by Joule heating
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Floating Body Cell (FBC)

Floating body as a charge storage

High-speed volatile memory (DRAM)
Reliability issue from the charge generation
Self-Healing in FBC

Iterative self-healing process:
$10^{11}$ operations $\rightarrow$ degradation $\rightarrow$ annealing

✓ Endurance $> 10^{12}$ cycles & retention $> 100$ ms
Flash Memory

Program/erase stress on a tunneling layer
Increment of trapped charge/interface state
Self-Healing in Flash Memory

Iterative self-healing process:
1 P/E operation → annealing → no degradation

☑️ Endurance > $10^4$ cycles & retention > 10 years
Word-Line Design

In memory array, a long word-line (WL) is required for high density. And many bit-lines are included in one WL.

Thermal distribution: non-uniform along the WL
- Center temp.: 900 °C
- Edge temp.: 300 °C
Thermally Uniform WL

**Conventional**

WL (Heat source) - Heat sink

**Thermally isolated WL**

Thermal bridge between heat source and sink
- Heat source (WL) → thermal island
- Uniform temperature regardless of a length of WL
All parts of logic and memory are not used at the same time!

On-the-fly thermal annealing
Idle state → aging check → recovery process
Data loss during the healing: copy to redundancy
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High Reliability Applications

- **Space**
  - Image: Texas Instruments

- **Military**
  - Image: Texas Instruments

- **Transportation**
  - Image: Texas Instruments

- **Automobile**
  - Image: Tesla

- **Medical equipment**
  - Image: Intuitive Surgical Systems

- **Server and network**
  - Image: Google
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Conclusions

- The temperature arising from Joule heat by the gate was applied for the on-the-fly self-healing process.

- The lifetime of devices can be extended, which opens an opportunity for nano-spacecraft to sustain more than 20 years of deep space exploration.
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By far, R&D activities across in industry, academia, and government have focused on “How to improve endurance against the radiation.”

But, this project is “How to recover and self-heal to healthy condition” as human immune systems.

Thank you for your attention.