UNIVERSITY OF CALIFORNIA, SANTA CRUZ

RRAM Architectures and Circuits at Nanoscale

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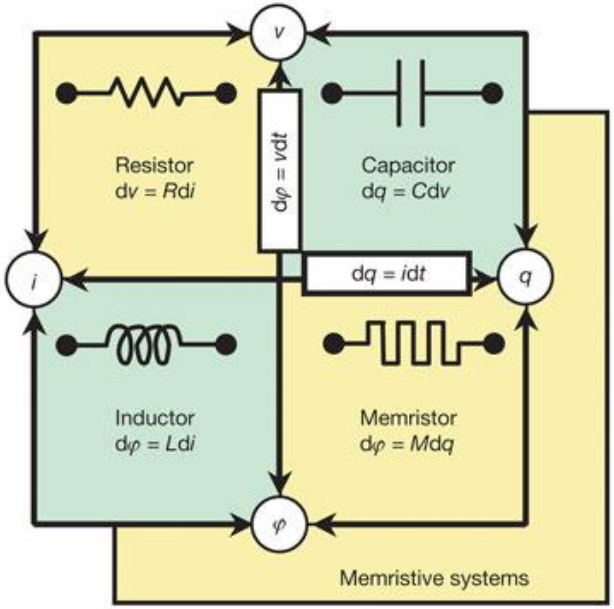
April 6, 2012

Outline of This Talk

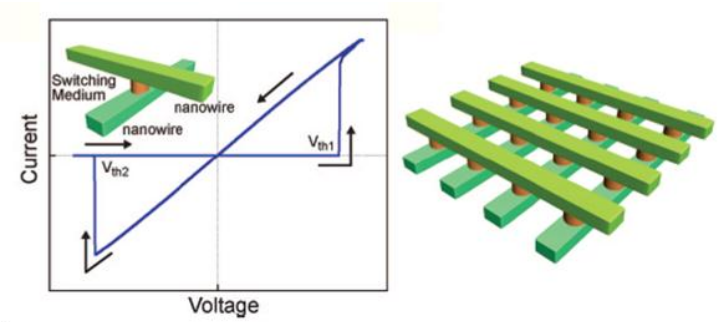
Memristors and Memristive Electronics

- Circuit Theoretic and Design Research
  - Memristive nonlinear dynamics
  - Compact device modeling
  - Low Power Systems Design

- Nanoelectronics- Memristive Systems
  - Ultra-dense nonvolatile memories
  - Stateful Boolean logic and resistive nanocomputing
  - Self-reconfigurable circuits and systems
  - Neuromorphic synaptic circuits and systems, memory-intensive systems for bioinformatics and other applications



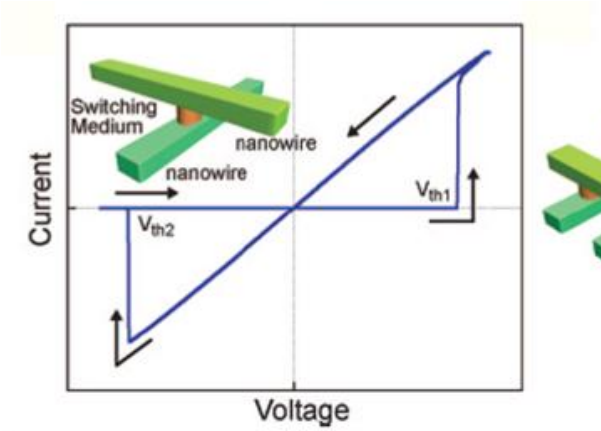
Memristor as 4th fundamental device

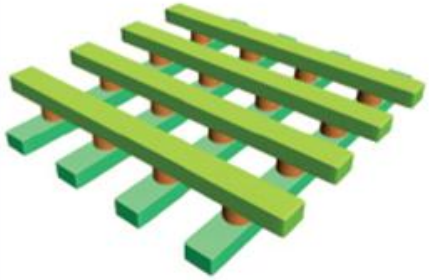


Memristor dynamics and crossbar integration

Nonvolatile Resistive Memory

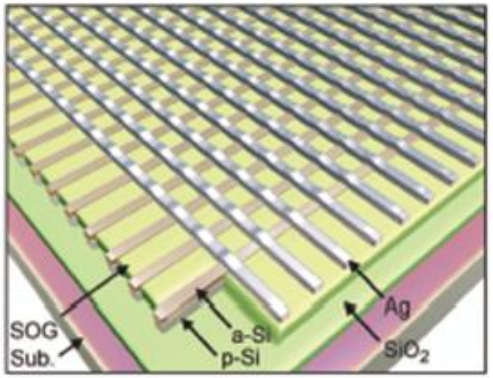
- Nanotechnology Enables Ultra-Dense Memory

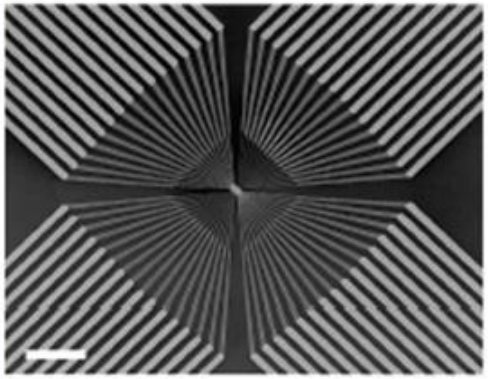




Memristive devices array
in a nano-crossbar structure

Early memory based on
p-Si/a-Si/Ag
by Univ. of Michigan



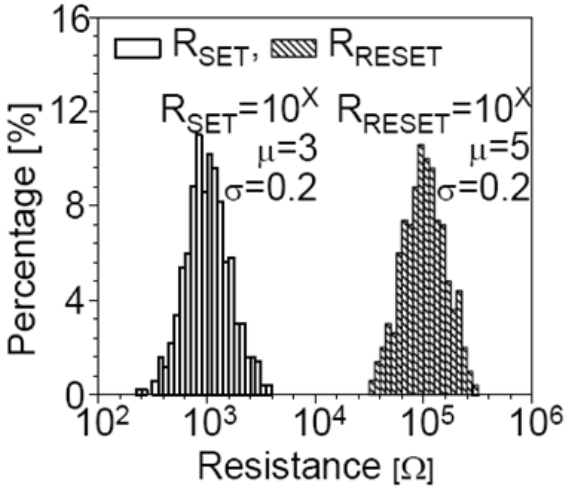


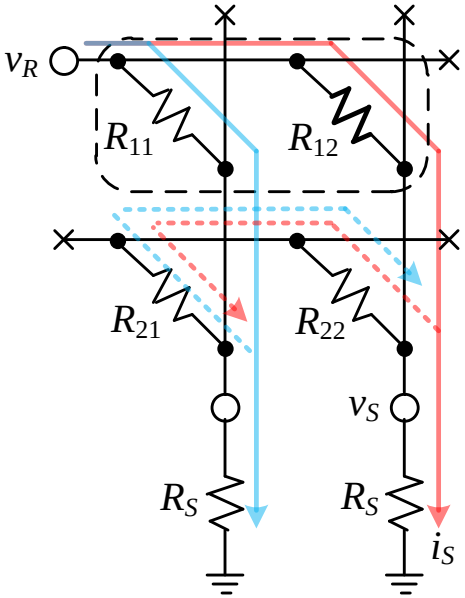
Ref. S.H. Cho, *et. al.*, Nano Letters, 2009

Resistive Random Access Memory (RRAM)

- Key factors of importance
  - Physical Geometry
  - Process/Thermal Reliability
  - Embedding Compatibility into CMOS
  - Forming or formingless
  - 3D Stackability
- Challenges for Memory Devices
  - Number of Storage Bits/Device
  - Retention >10 years
  - Endurance > 10^{17}
  - Read/Write Energy < 1fJ/bit
  - Read/Write Speed < 1ns

Issues on RRAMs





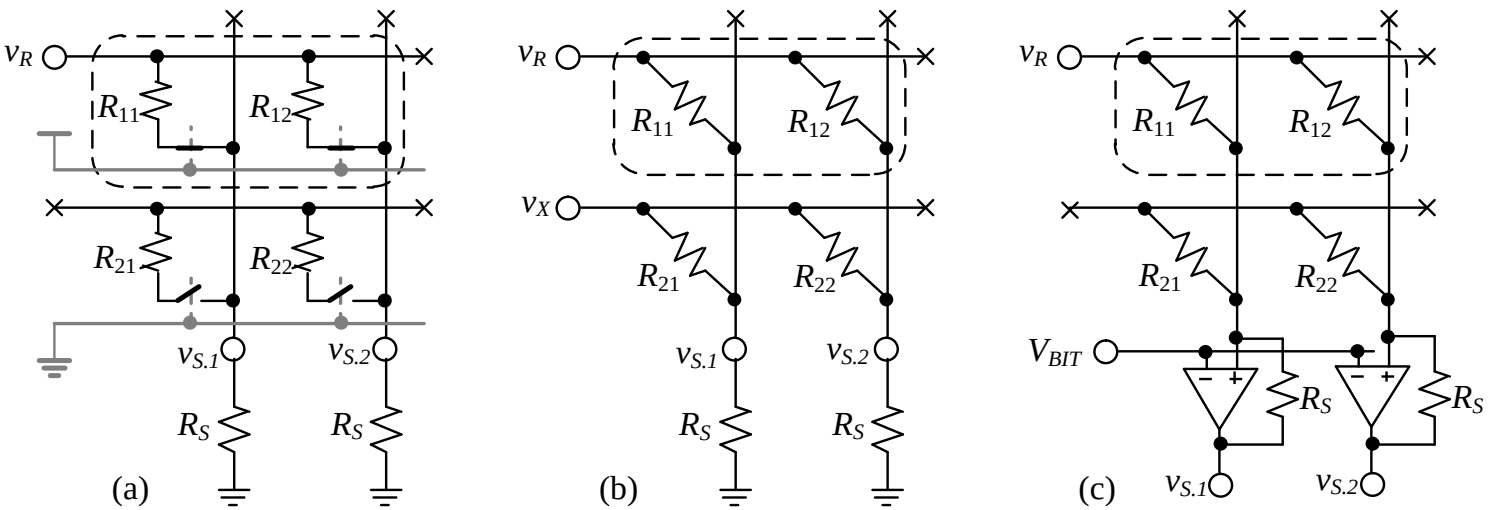
- Technology issues
  - Reliable device process (Variability)
  - Multi-layer memory integration
- Circuit issues
  - Power consumption for Write/Read operations
  - Performance degradation by "Sneak currents"
  - "Data-pattern" sensitive power & read performance

How to deal with "Sneak Currents"?

With selection devices (e.g., 1T1R or 1D1R)

Trading-off with power ($0 \le v_X < v_R$)

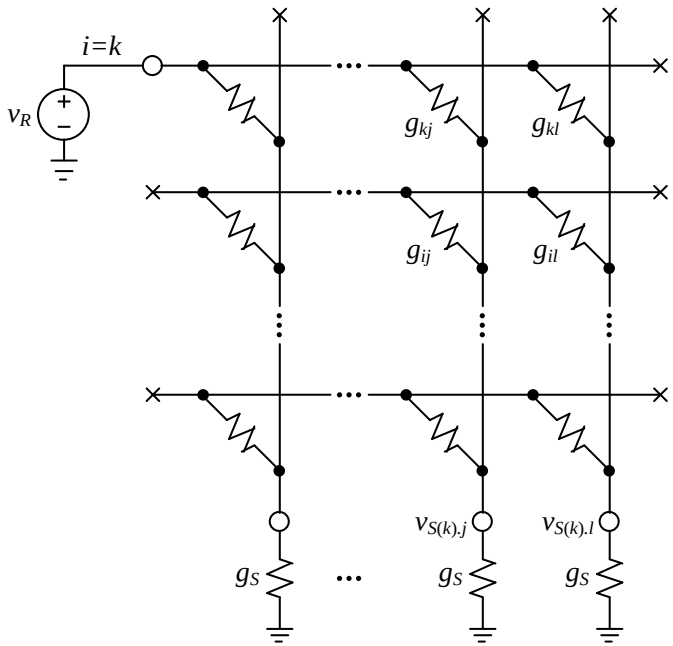
Forced bit-line voltages (e.g., TIA type)

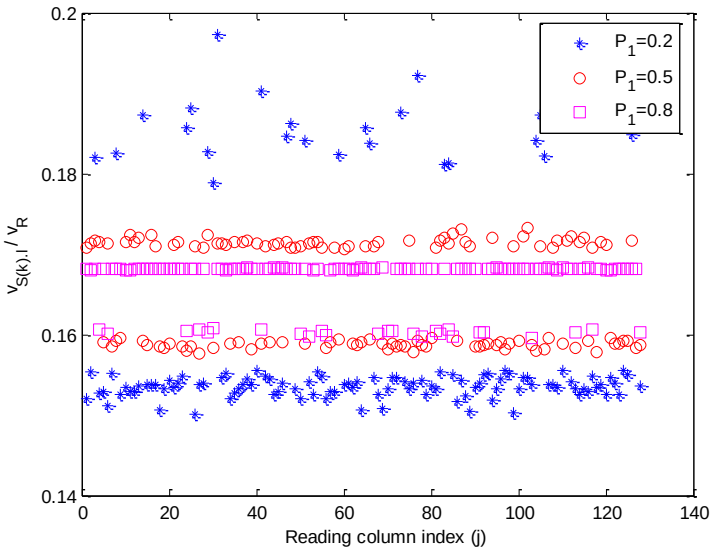


Performance	(a)	(b)	(c)
Sensing margin	Large	Narrow	Large
Speed	Fast	Fast	Slow
Power	Low	Moderate ~ High	Low
2D capacity	Low	High	High
3D stackability	Challenging	Good	Good

Sensing Behaviors of RRAMs

- Passive RRAM with Resistor Terminations
  - Sensing performance is highly dependent on the stored "Data-pattern", due to "Sneak Currents"
  - The more low-resistance cells lead to the lower sensing margin





Data-pattern sensitive Read performance (128x128 array)

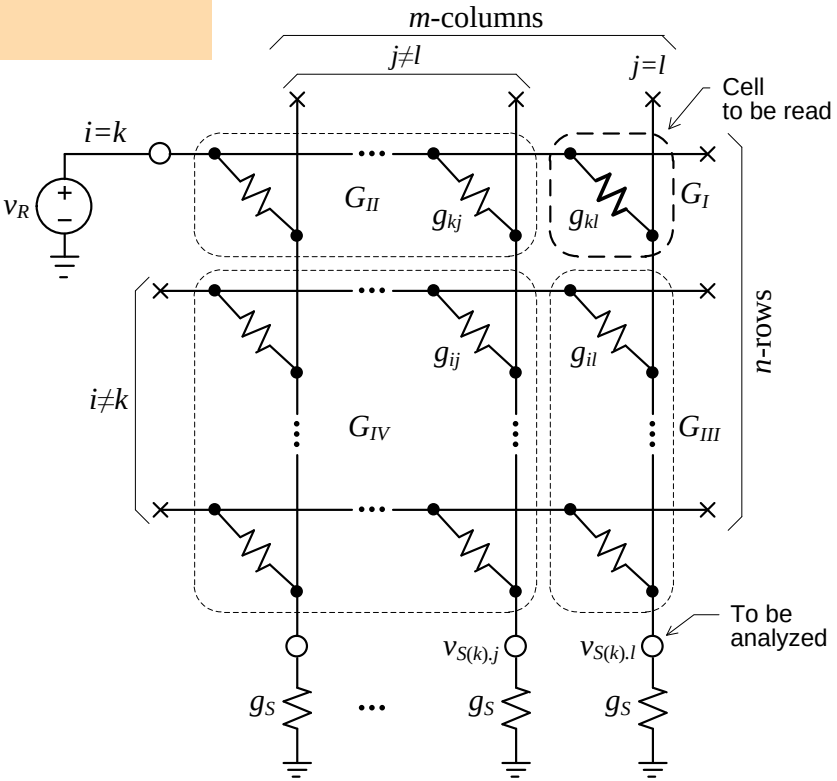
RRAM Modeling

- Analysis and Estimation of RRAM Performance ($m \times n$ array)
  - Full node analysis needs to solve for

$$\left(g_S + \sum_{i \in I_U} g_{ij}\right) \cdot v_{S(k).j} = g_{kj} \cdot v_R + \sum_{i \in I_k} \frac{g_{ij}}{\sum_{y \in J_U} g_{iy}} \sum_{u \in I_U} \left(g_{iu} \cdot v_{S(k).u}\right)$$

for j=1, 2, …, m

  - A worst case equivalent model has been reported in 1969.
  - Computation efficient statistical model for analysis of data- and variability-dependency
  - Sub-grouping for modeling
    - G_I : cell to be read (k, l)
    - G_{II} : cells in reading row
    - G_{III} : cells in reading column
    - G_{IV} : all the others

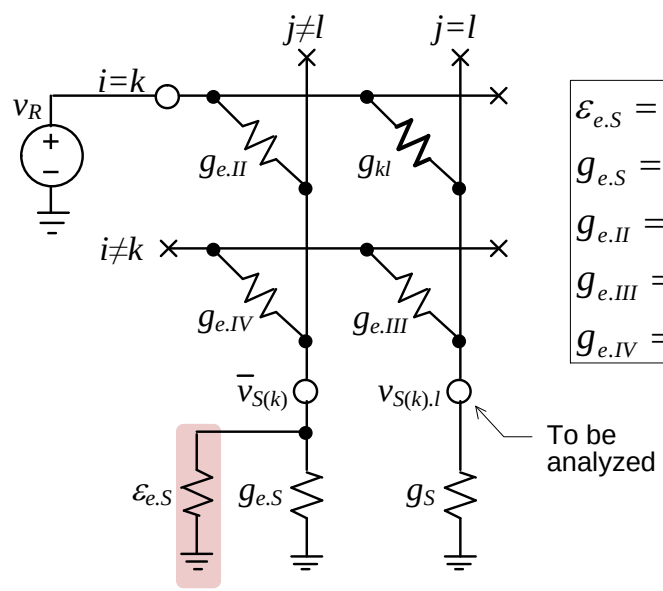


2x2 Equivalent Memory Model

$$\underbrace{\begin{bmatrix} (g_{e.S}+\varepsilon_{e.S})+g_{e.IV}+g_{e.II} & 0 \\ 0 & g_S+g_{e.III}+g_{kl} \end{bmatrix}}_{\mathbf{G_{P(k)}}} \cdot \underbrace{\begin{bmatrix} \bar{v}_{S(k)} \\ v_{S(k).l} \end{bmatrix}}_{\mathbf{V_{S(k)}}} = \underbrace{\begin{bmatrix} g_{e.II} \\ g_{kl} \end{bmatrix}}_{\mathbf{G_{a(k)}}} \cdot v_R + \underbrace{\frac{1}{g_{e.IV}+g_{e.III}} \cdot \begin{bmatrix} g_{e.IV}g_{e.IV} & g_{e.IV}g_{e.III} \\ g_{e.III}g_{e.IV} & g_{e.III}g_{e.III} \end{bmatrix}}_{\mathbf{C_{X(k)}}} \cdot \underbrace{\begin{bmatrix} \bar{v}_{S(k)} \\ v_{S(k).l} \end{bmatrix}}_{\mathbf{V_{S(k)}}}$$

- 2×2 equivalent model for $n \times m$ RRAM array
  - Each group is represented in a single equivalent admittance
  - Capable of flexible analysis and ease of simulation

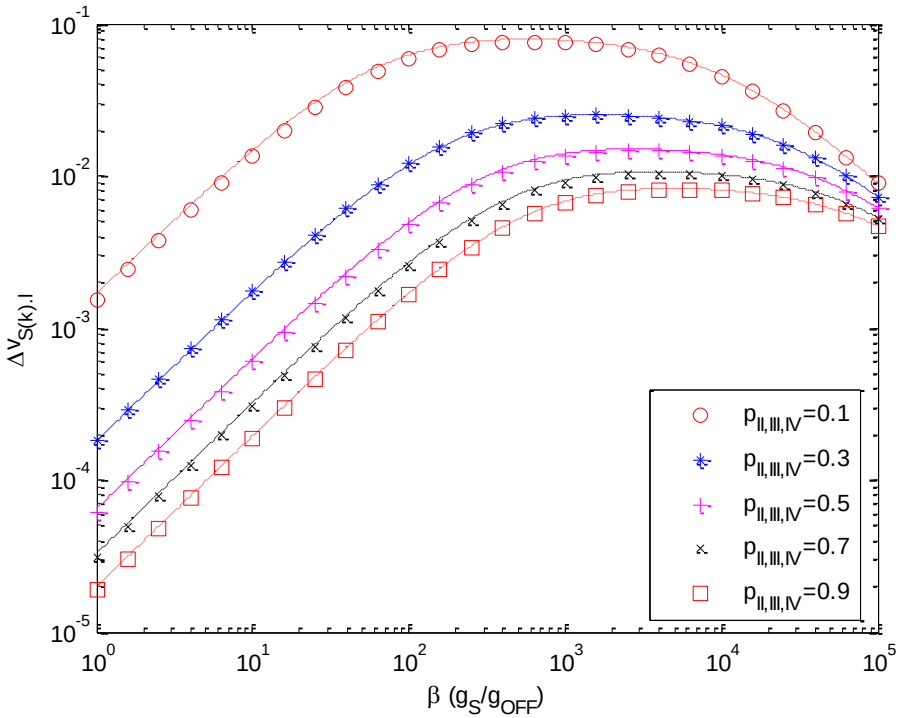
$$\mathbf{V_{S(k)}} = \left[\mathbf{G_P} - \mathbf{C_{X(k)}}\right]^{-1} \cdot \mathbf{G_{a(k)}} \cdot v_R$$



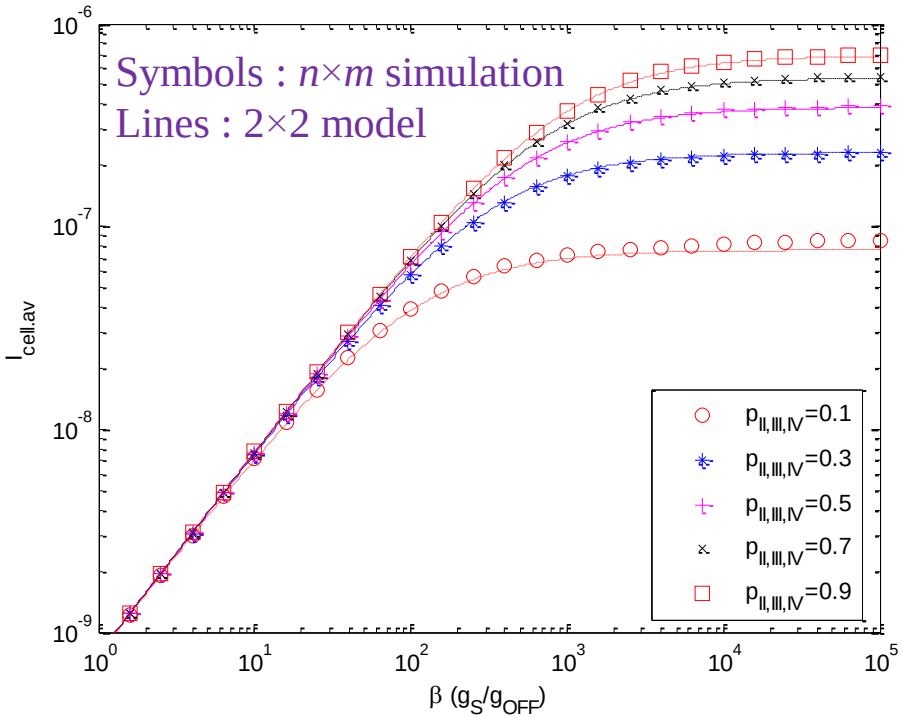
$$\varepsilon_{e.S} = (m-1)\varepsilon_{II}$$
$$g_{e.S} = (m-1)g_S$$
$$g_{e.II} = (m-1)\bar{g}_{II}$$
$$g_{e.III} = (n-1)\bar{g}_X$$
$$g_{e.IV} = (m-1)(n-1)\bar{g}_{IV}$$

2x2 Model Results

- Example for 128×128 array
  - Conditions : $\alpha = R_{OFF}/R_{ON} = 10^3$, ($R_{OFF}$=10 MΩ, R_{ON}=10 kΩ)
  - Data-pattern dependent β ($=R_{OFF}/R_S$) is desirable



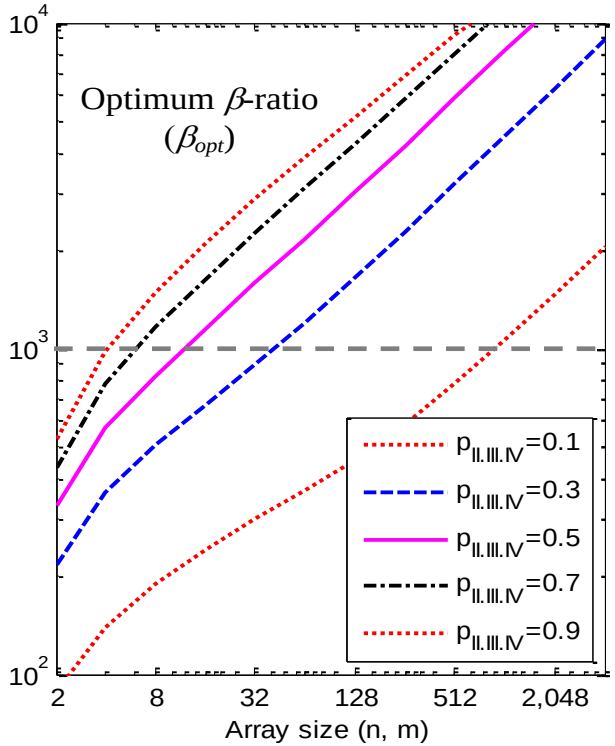
(a) Detection margin

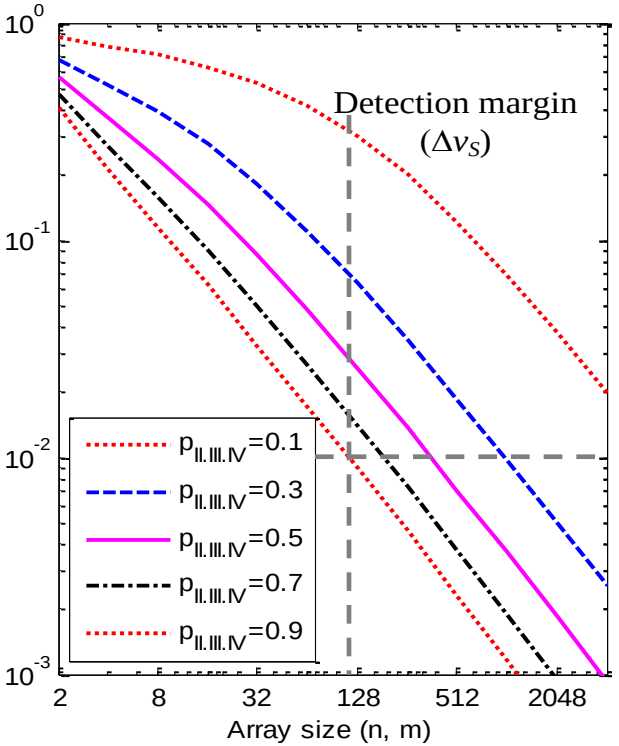


(b) Average cell current

Array Size Dependency

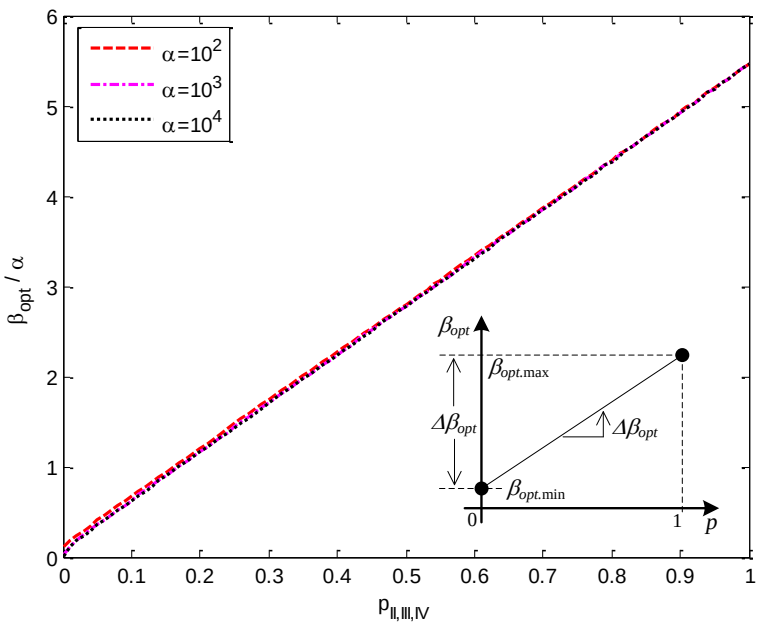
- Optimal R_S ($R_{S.opt}$)
  - Generally required to be small for large array sizes
  - Sensitive to data-pattern
- Detection margin (Δv_S)
  - Decreases with array size
  - Sensitive to data-pattern
  - For 1% margin, n & m <128

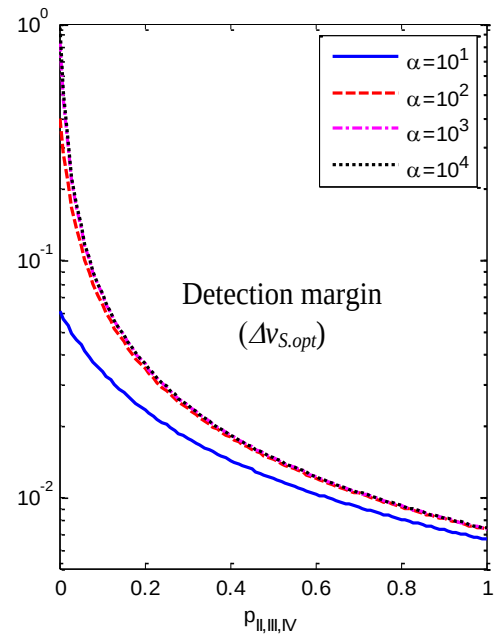




Data-Pattern Dependency

- Highly sensitive performance to data-pattern
  - β_{opt}/α is approximately linear to data probability
  - Data dependent optimum β-ratio ($\beta_{opt}=R_{OFF}/R_{S.opt}$) is desirable
- α-ratio ($=R_{OFF}/R_{ON}$) dependency
  - Generally good for larger α-ratios (rapidly desensitized as $\alpha > 10^2$)





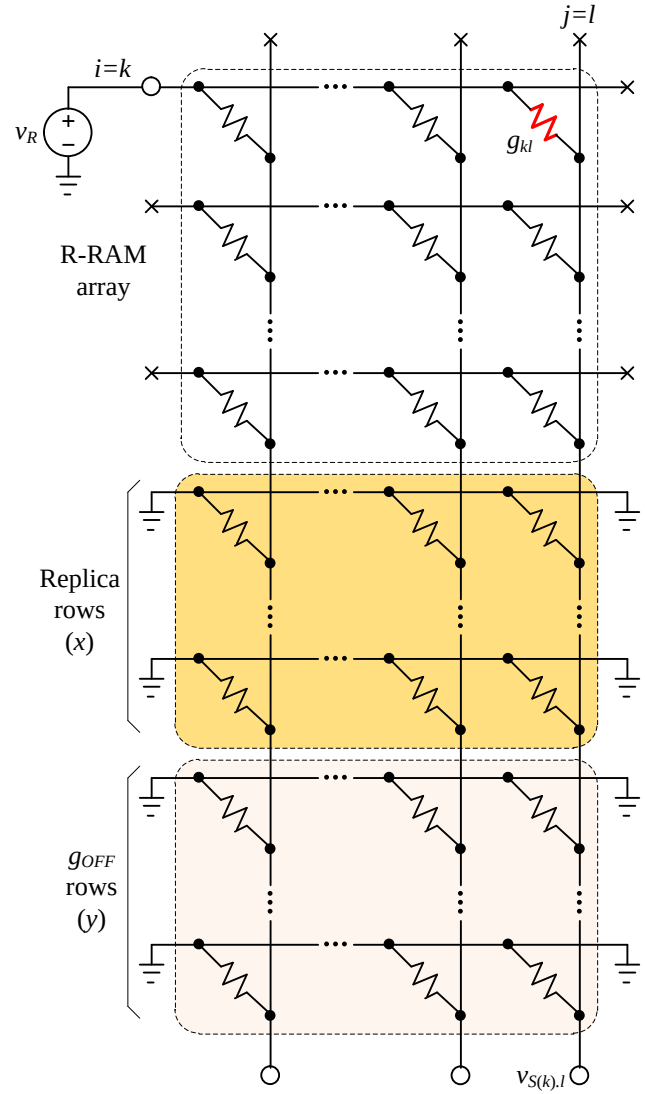
Data-Dependent Adaptable $R_{S.opt}$

- Adaptable g_S configuration
  - Composed of grounded replica rows and fixed resistance rows.
    - x # of replica rows
    - y # of g_{OFF} rows
  - Expected value of g_S

$$x = \frac{\Delta\beta_{opt}}{\alpha - 1} \approx \frac{\Delta\beta_{opt}}{\alpha}, \text{ and } y = \left(\beta_{opt.\min} - x\right)$$

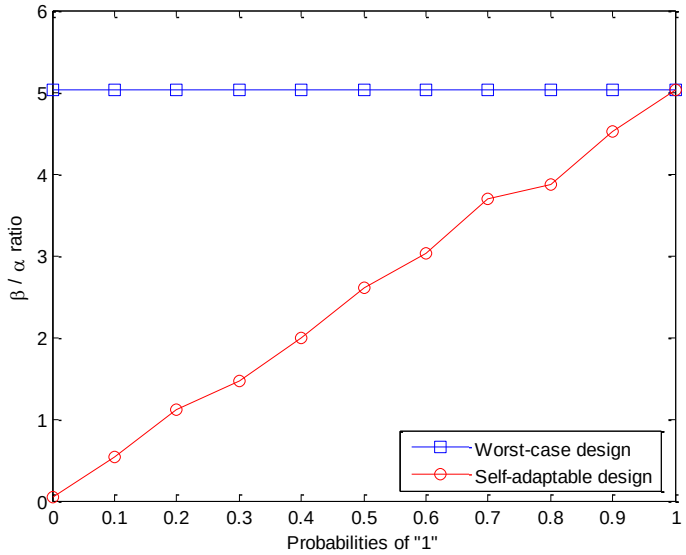
$$\Rightarrow \overline{\beta} = x(\alpha - 1)p_1 + (x + y) \approx \beta_{opt}$$

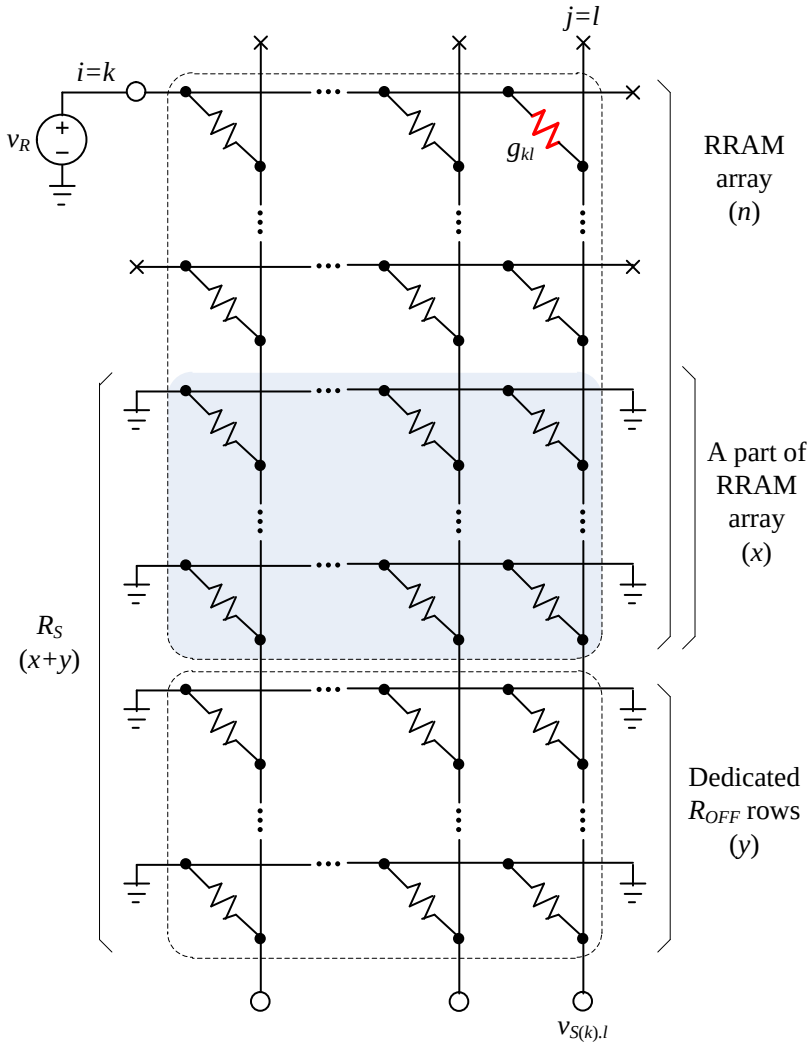
  - Adaptable $R_{S.opt}$ leads to both low-power and large detection margin.



Adaptable $R_{S.opt}$ Example

- 128×128 RRAM array
  - R_{ON}=10kΩ, R_{OFF}=10MΩ (α=10^3)
  - R_S constructions by
    - Reconnecting a part of unread RRAM (x=5)
    - Dedicated R_{OFF} rows (y=35)





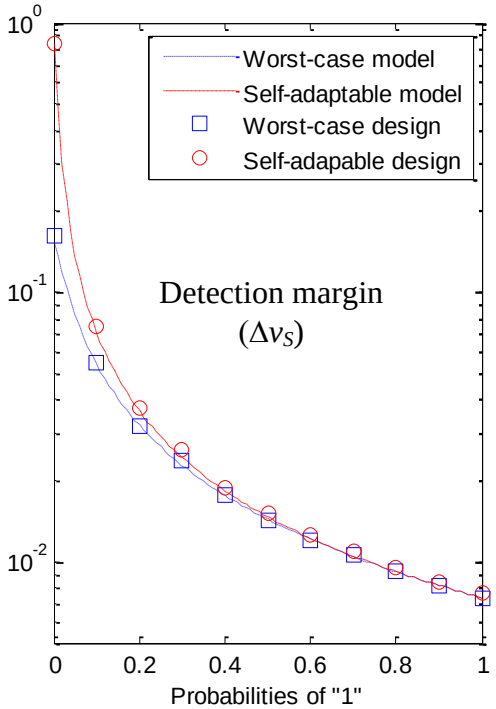
Worst Case vs. Self-adaptable

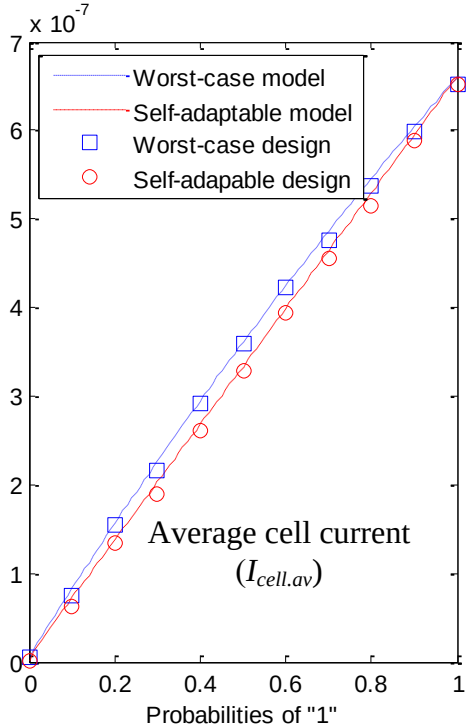
- Worst case design
  - Constant β_{opt}/α that made for the worst case data pattern
  - The worst case appears with all stored data of "1"s
  - Excess current consumption and reduced detection margin for non-worst cases

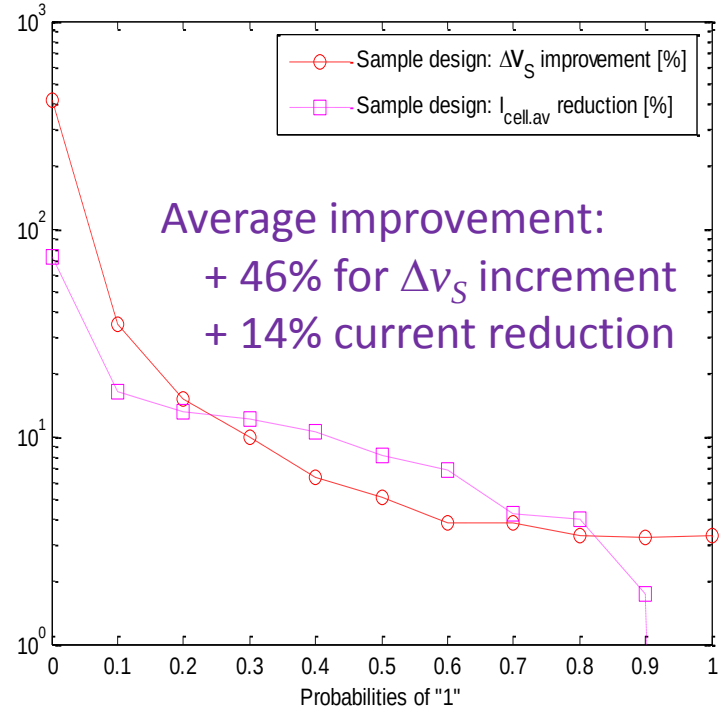
- Self-adaptable design
  - Adaptable β_{opt}/α that made for every data pattern
  - For every data pattern, it provides maximally available detection margin
  - Current consumption can be saved for general non-worst cases.

Performance Comparison

- Worst case vs. self-adaptable design
  - Self-adaptable design shows the larger Δv_S and low $I_{cell.av}$, simultaneously, compared to the worst-case design
  - Especially for low probability cases

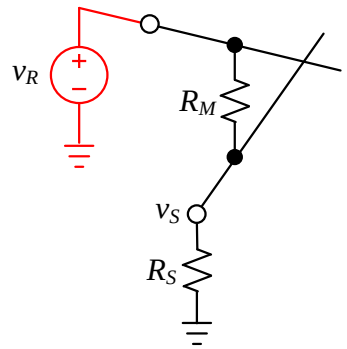
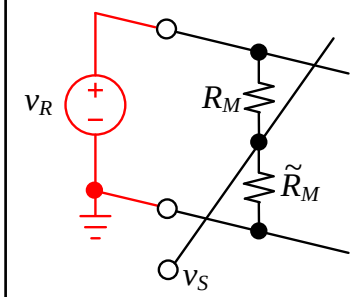






Complementary Memory Cell

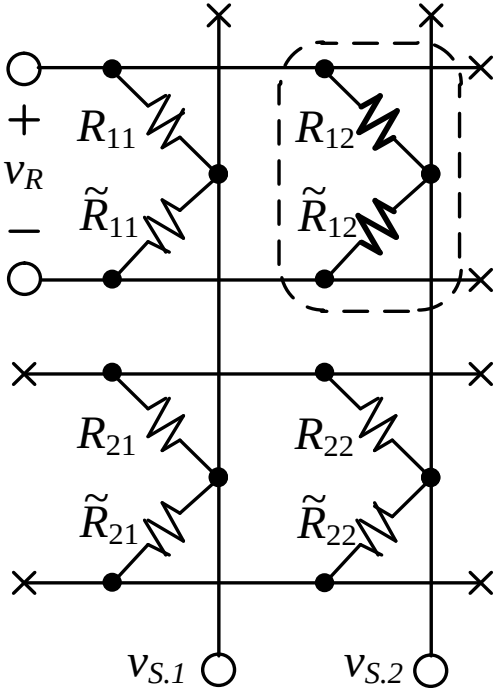
- Complementarily written two devices cell (CR-cell)
  - Provides data-dependent equivalent sense resistance ($R_{S.eq}$)

	1R-cell		CR-cell
Readout circuit configuration			
Sense resistance	$R_{S.opt} = R_{OFF} / \sqrt{\alpha}$	> <	$R_{S.eq} = \tilde{R}_M$
Normalized detection margin	$\Delta V_{S.1R} = \left(\frac{\sqrt{\alpha} - 1}{\sqrt{\alpha} + 1} \right)$	<	$\Delta V_{S.CR} = \left(\frac{\alpha - 1}{\alpha + 1} \right)$
Normalized average current	$I_{S.1R} = g_{OFF} \cdot \frac{\sqrt{\alpha}}{2}$	>	$I_{S.CR} = g_{OFF} \cdot \frac{\alpha}{1 + \alpha}$

$\alpha \equiv R_{OFF} / R_{ON}$

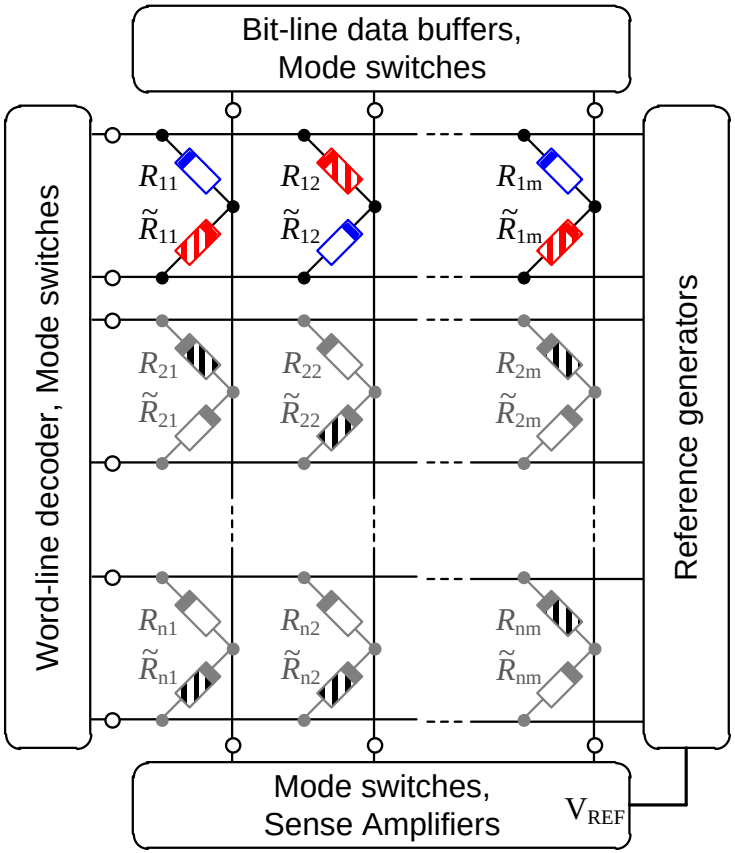
Array Properties of CR-cell Array

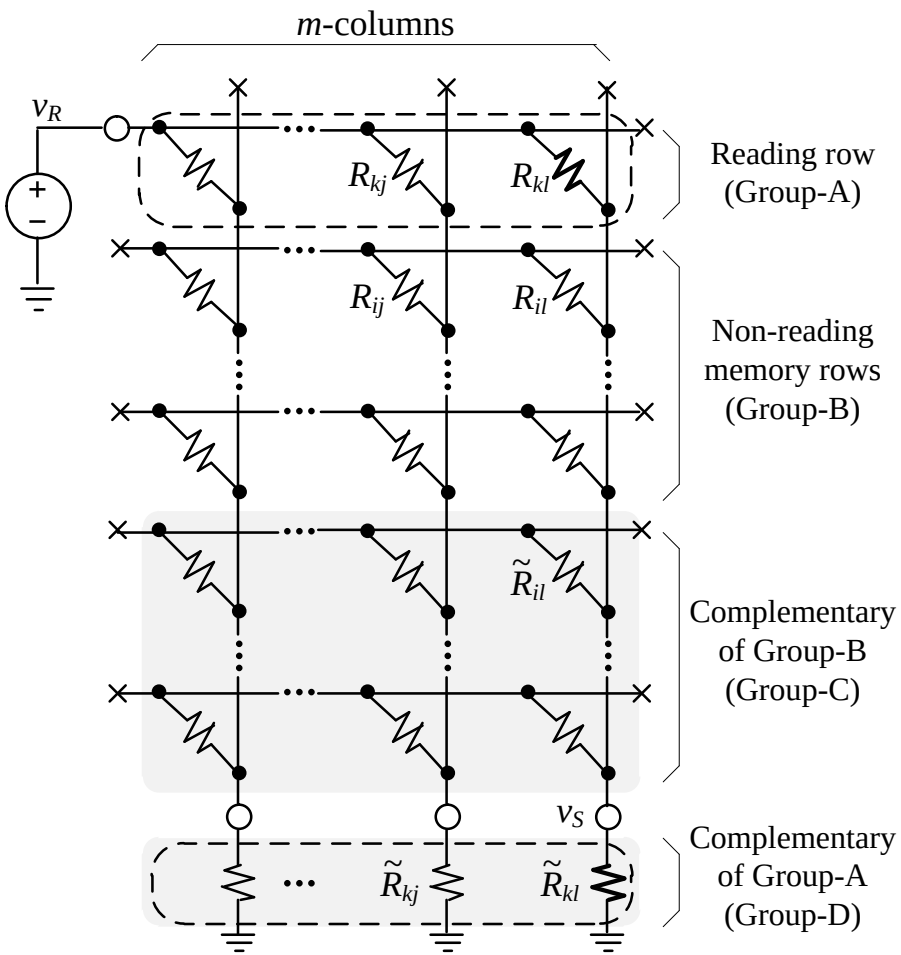
- Features
  - Lower design complexity
    - With no optimization process on R_S
  - Data-dependent equivalent R_S
  - Reduced effective density
  - Doubled number of sneak paths by complementary devices
- Data-pattern dependency
  - Constant detection margin
    - With larger window
  - Regulated readout currents
    - With smaller values



2x2 array of CR-cell memories

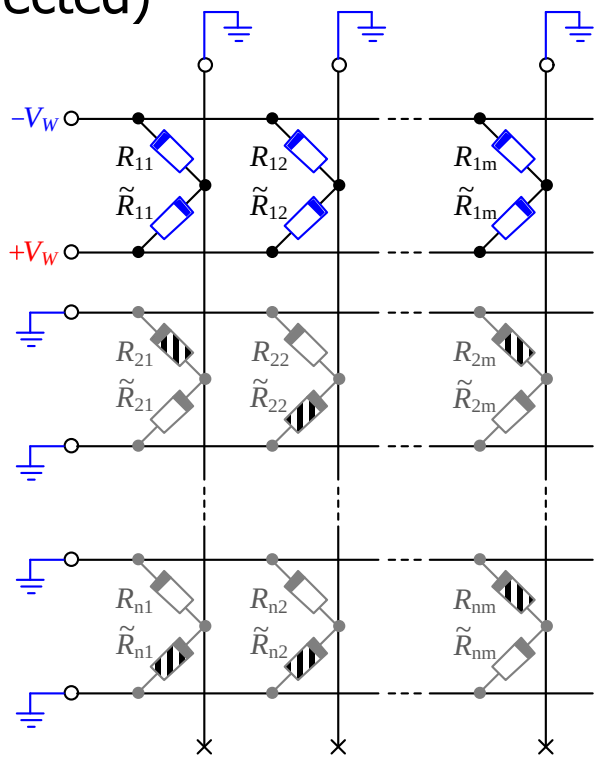
n x *m* Dimensional CR-cell Array



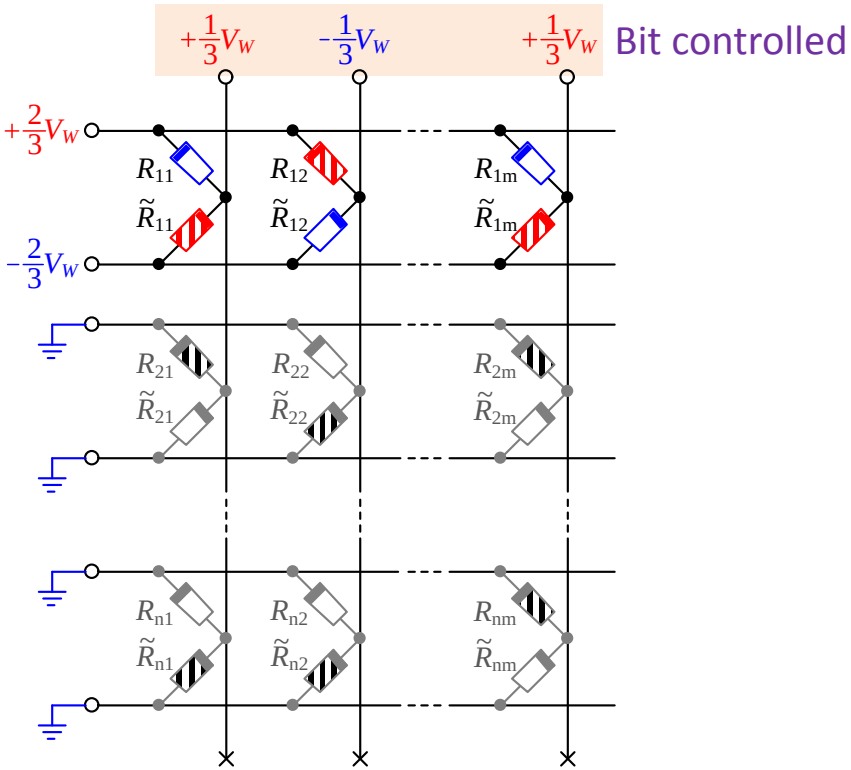


Write-Mode Configuration

- 2-Step 'WORD-wise' Writing
  - Step-1: RESET for all devices of a selected word line
  - Step-2: SET for selected bit devices (other devices are halfway selected)



Step-1: RESET



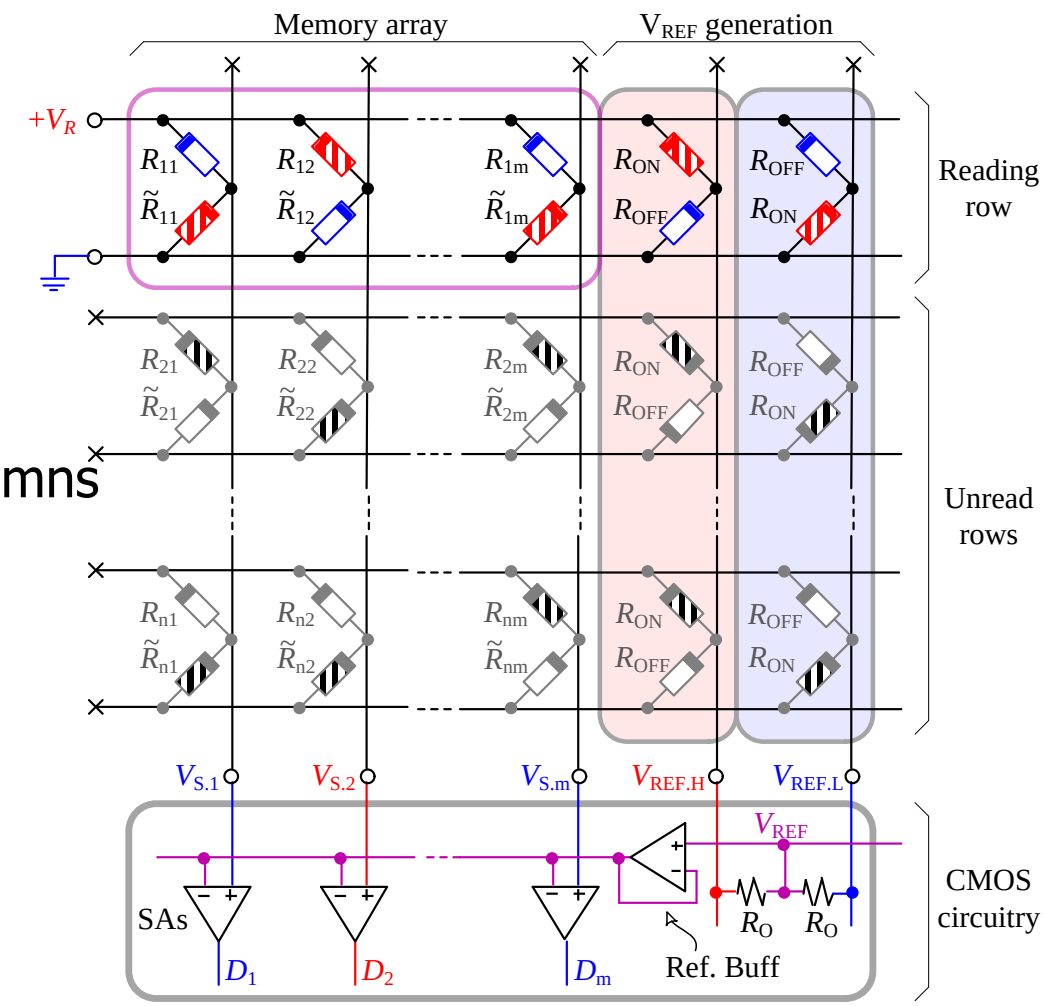
Step-2: Selective SET

Read-Mode Configuration

- 'WORD-wise' READ
  - Comparison V_S with V_{REF}
- Reference generation
  - Desirable to be data-dependent
  - Finding median V_S by dedicated R_{OFF} & R_{ON} columns

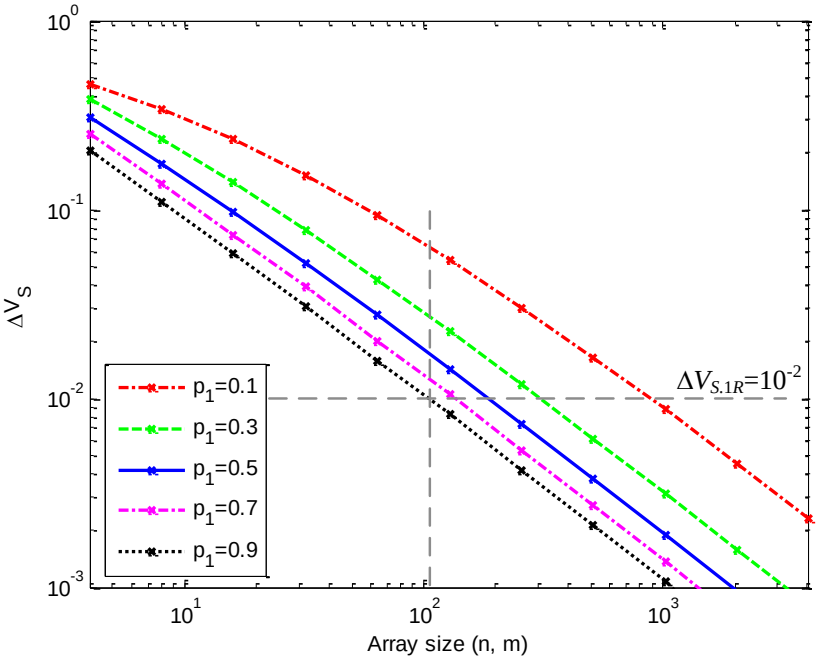
$$V_{REF} = \left(V_{REF.H} + V_{REF.L}\right)/2$$

  - Each REF cell has complementary devices (p_{III}=0.5)
  - Reference buffer isolates capacitances of SAs

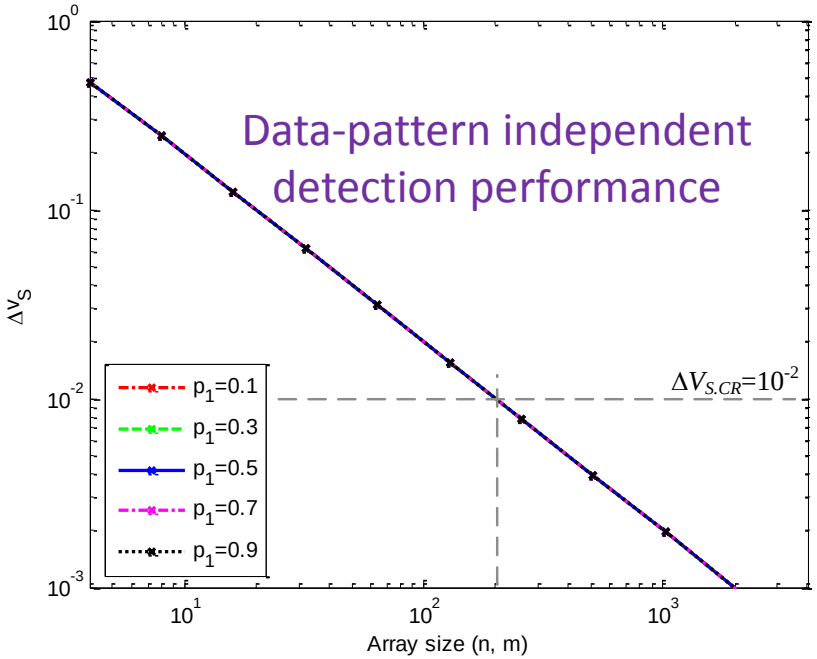


Performance Comparison (I)

- Array size dependency
  - Optimally designed 1R-cell array vs. CR-cell array
  - CR-cell memory is capable of ~4x larger size



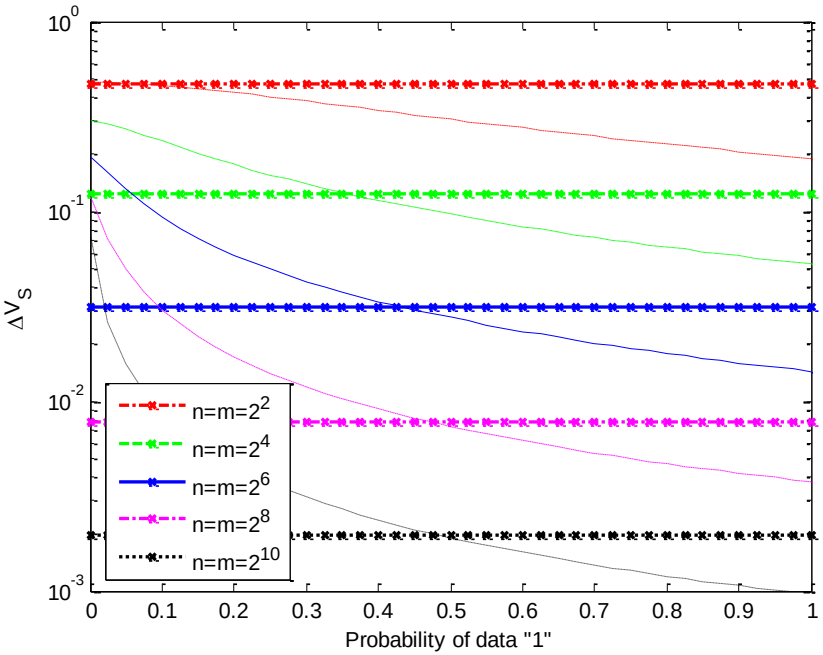
1R-cell RRAM



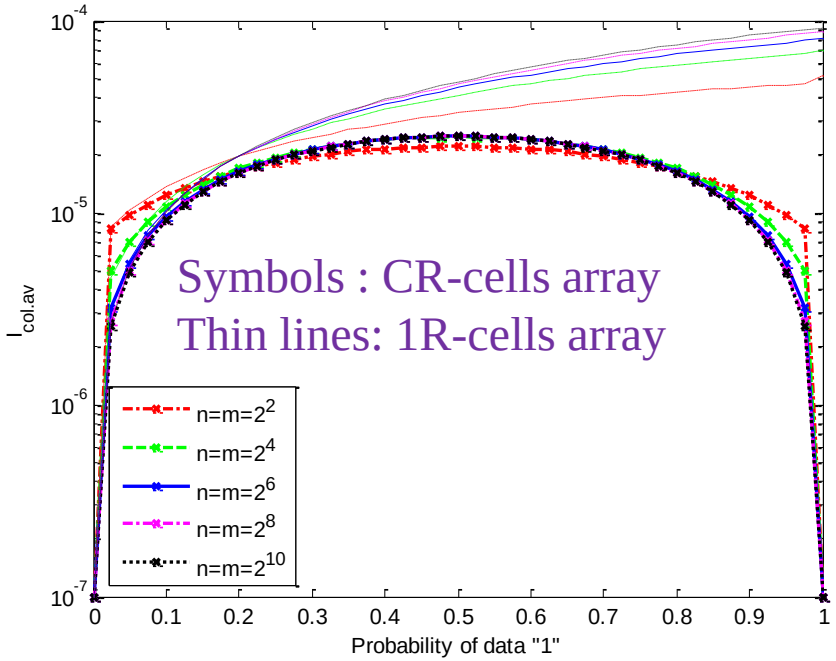
CR-cell RRAM

Performance Comparison (II)

- Data-pattern Dependency
  - Optimally designed 1R-cell array vs. CR-cell array
  - Lower current consumption for all cases
  - Data-independent detection performance



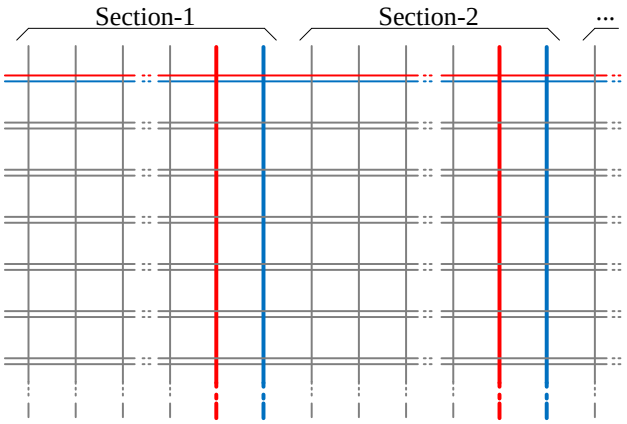
Voltage Detection Window

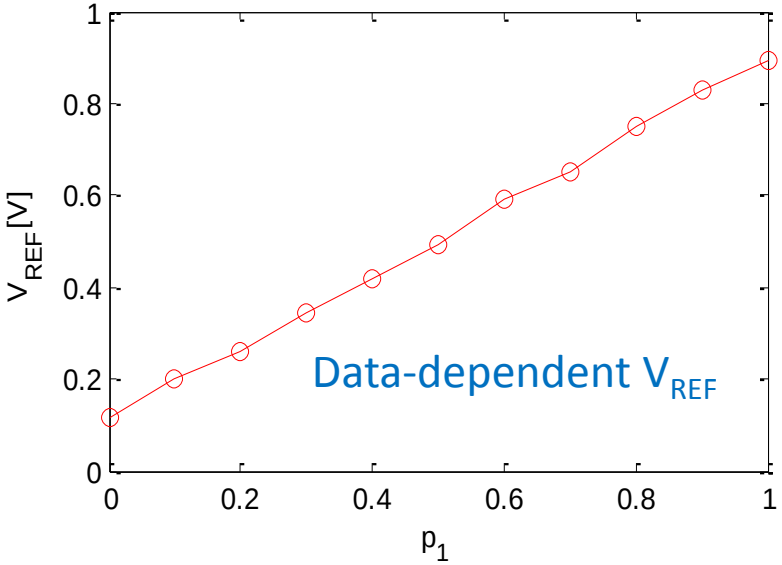


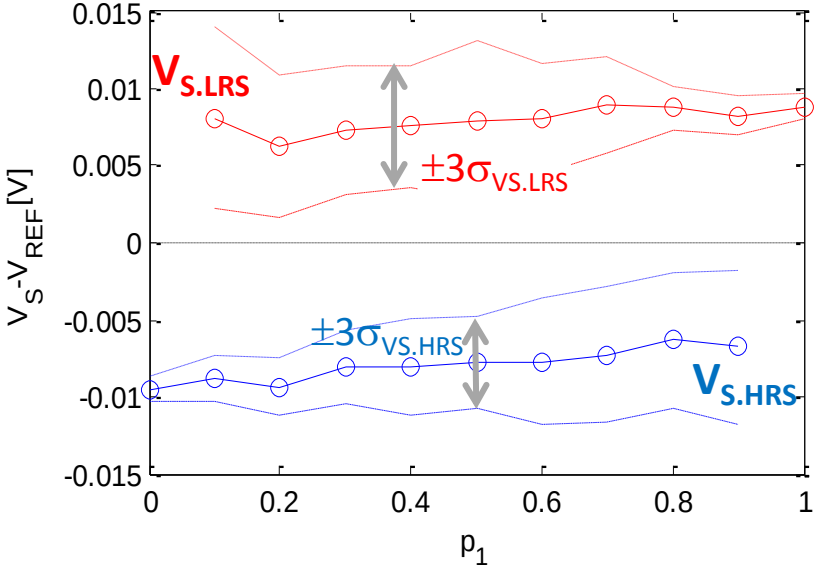
Sensing Current

Variability Effect on Read Performance

- For a 128x128 array:
  - Resistances: log-N dist. w/i σ=20%
  - $R_{ON.0}$=10kΩ, $R_{OFF.0}$=10MΩ
  - Array size=128x128
  - REF sections for every 8-bits







Summary

- Computation efficient RRAM model
  - Data-dependent 2x2 equivalent circuit model
  - Provides optimal design parameters for any random data
- Complementarily written RRAM cell (CR-cell) has been presented
  - Data-pattern independent sensing performance
  - Larger voltage sensing window, Regulated lower sensing current

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