People who did the work:

Over 60 current and former members of the QSR Research group and 40 members of other HP orgs

esp. Greg Snider, Duncan Stewart, Dimitri Strukov, Matthew Pickett, Julien Borghetti, and Jianhua Yang

Our partners at UCLA & Caltech,

Our partners at LBNL and NIST

Supported in part by DARPA & IARPA
The nanotechnology dilemma

We say that nanotech is different, but then we try to build familiar objects with nano dimensions... We say that nanotech is interdisciplinary, but do we just work with the usual suspects? We say that nano is new – but have we forgotten old lessons?

Overview of Presentation

• What is a Memristor?
• How do you make them?
• What are they good for?
  – Configurable rectifiers and switches
  – Crosspoint Memories
  – Sequential Implication Logic
  – Synaptic computation
3 fundamental passive linear circuit elements

Resistor – 1827
Georg Ohm

Resistor: $v = R \ i$

Capacitor – 1745
Volta / von Kleist & van Musschenbroek
Benjamin Franklin

Capacitor: $q = C \ v$

Inductor – 1831
Michael Faraday
Joseph Henry

Inductor: $\phi = L \ i$

1960’s – Leon Chua generalizes circuit theory to nonlinear systems of equations

Resistor: $dv = R \ di$

Capacitor: $dq = C \ dv$

Inductor: $d\phi = L \ di$

And sees that there is a hole where an obvious relation seems to be missing
Realm of nonlinear circuits

Danger! Chaos!

Realm of nonlinear circuits
Nanoelectronics will be nonlinear

Opportunity!

Danger! Chaos!
In 1971, Chua postulates the memristor, but states that there is no known example.


Four Fundamental Nonlinear Passive Circuit Elements

- **Resistor**
  \[ dv = R \, di \]
  - Voltage
  - Current

- **Capacitor**
  \[ dq = C \, dv \]
  - Voltage
  - Charge

- **Inductor**
  \[ d\phi = L \, di \]
  - Voltage
  - Magnetic Flux

- **Memristor**
  \[ d\phi = M \, dq \]
  - Voltage
  - Magnetic Flux

- **Memristive Systems**

\[ v = R(w) \, i \]

\[ \frac{dw}{dt} = f(i) \]
Current vs. Time for Sinusoidal Voltage Bias

Years of research looking for “molecular switches”

switching... with sharp thresholds
O vacancy drift model for TiO$_2$-x switch

As fabricated

Positive voltage drifts oxygen vacancies left to increase total conductivity

Reducedoxidized

Simplified Theory of Memristance

Two coupled equations of motion –
One for the charged vacancies
One for the electronic transport
(both versions of Ohm’s law)

Look at current-voltage plots of the model

Comparison between Theory and Experiment:
Pt : TiO₂ : Pt Memristor!
Ionic Memristive Device
(Hard Boundary Conditions)

\[ R_{\text{OFF}}/R_{\text{ON}} = 125 \]

\[ V_0 = 1 \text{ V} \]

\[ R_{\text{OFF}}/R_{\text{ON}} = 50 \]

\[ V_0 = 2 \text{ V} \]

no window function but w is not changing beyond [0, D]

Metal Oxide Resistive Switches

“Memory effects” in oxides have been known for a while:

G. Deamaley et al., Rev. Prog. Phys. (1970) a review with 150+ references

Just a few recent references:

- S. Seo et al., APL (2003) Ni
- B. J. Choi et al., JAP (2005) Ti
- D. Lee et al., EDL (2005) Zr
- A. Chen et al., IEDM’05 Cu
- M. Kund et al., IEDM’05 Ag
- D. C. Kim et al., APL (2006) Nb
- N. Banno et al., IEICE TE (2006) Cu2O
- T.-N. Fang et al., ICMTD’07 Cu
- L. Courtade et al., ICMTD’07 Ni
- W. Guan et al., APL (2007) Zr
- S.-W. Kim & Y. Nishi, NVMTS’07 Cu(S)
- D. Stewart, NVMTS’07 Ti
- K.-C. Liu et al., NVMTS’07 Hf
- D. Lee et al., APL (2007) Mo

With time, data are becoming more reproducible:

slide courtesy K. Likharev
Semiconductor memristance is coupled ion-electron motion

Slightly More Advanced Theory - Ions

\[ J_{\text{ION}} = J_{\text{drift}}^{\text{ION}} + J_{\text{solute diffusion}}^{\text{ION}} \]

\[ J_{\text{drift}}^{\text{ION}} = q \mu_0 E_0 \sinh\left( \frac{E}{E_0} \right) \]

\[ J_{\text{solute diffusion}}^{\text{ION}} = q D \frac{\partial N}{\partial x} \]

\[ D \approx f a^2 \exp\left[ -U_A / (k_B T) \right] / (1 - Na^3) \]

\[ N \frac{t}{J_{\text{ION}}} = -J_{\text{ION}} \frac{J_{\text{ION}}(x = 0) = J_{\text{ION}}(x = L) = 0}{x} \]

\[ N' = N \left( 1 - \left( 1 + \frac{1}{g} \exp\left( \frac{E_D - E_F - e\phi}{k_B T} \right) \right)^{-1} \right) \]
Slightly More Advanced Theory – e-s

\[ J_{\text{ELECTRON}} = e\mu_{\text{EL}} n_{\text{EL}} \frac{\partial E_F(x)}{\partial x} \]

\[ n_{\text{EL}} = N_C F \left( \frac{E_F - E_C + e\phi}{k_B T} \right) \exp \left( \frac{E_F - E_C + e\phi}{k_B T} \right) \approx N_C \exp \left( \frac{E_F - E_C + e\phi}{k_B T} \right) \]

\[ -\varepsilon\varepsilon_0 \nabla^2 \phi = ezN' - en_{EL} \]
Drift-Diffusion Model: Memristance

Voltage $v/v_0 = 120 \sin[2\pi (t/t_0)/0.01]$
50 nanometer Pt/TiOx/Pt devices

Switch ON ~10 ns, state is stable for (10^6?) years

Vacancy location controls switch polarity
Conclusions on Memristors

- The switching mechanism for the devices is field induced drift of positively charged O vacancies in TiO$_2$ that controls the resistance of the film
- This is the first experimental realization and physical model for a memristor – the fourth nonlinear passive circuit element that has been ‘missing’ for nearly 40 years
- We see that memristance arises naturally in systems where atomic and electronic equations of motion are coupled – this is far more likely to be observed at the nanoscale

What might memristors be used for?

- Non-volatile RAM
- Config Bits
- New forms of logic
- Electronic Synapse

But need hybrid circuits!
CMOS FPGAs

The good:
- Massive parallelism
- Defect tolerant
- Simple design

The bad:
- 80%-90% area is wires/configuration
- High capacitance → high power

The ugly:
- Defect characterization
- Compilation

SNIC Strategy

Start with CMOS FPGA
SNIC Strategy

1. Remove interconnect and configuration bits

2. Compress logic

3. Add nano interconnect and configuration
SNIC Strategy

1. Remove interconnect and configuration bits
2. Compress logic
3. Add nano interconnect and configuration

• Inexpensive CMOS design
• Inexpensive process (nanoimprint)
• Nano redundancy → defect tolerance
• Small size, high yield → low cost
• Low energy

SNIC: Chip Demo

Nanowire layer 2
Switching layer
Nanowire layer
CMOS layer

A) Bottom layer daughter mold
B) Top layer daughter mold

Courtesy Qiangfei Xia