Cation-based resistive memory

Emerging Non-Volatile Memory Technologies Symposium

San Francisco Bay Area Nanotechnology Council
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- **Introduction to ionic memory**
- **Cation memory *(PMC, CBRAM, ECM…)***
  - **Physics**
  - **Operation**
- **Conducting link morphology**
- **Active and passive arrays**
- **The way ahead**

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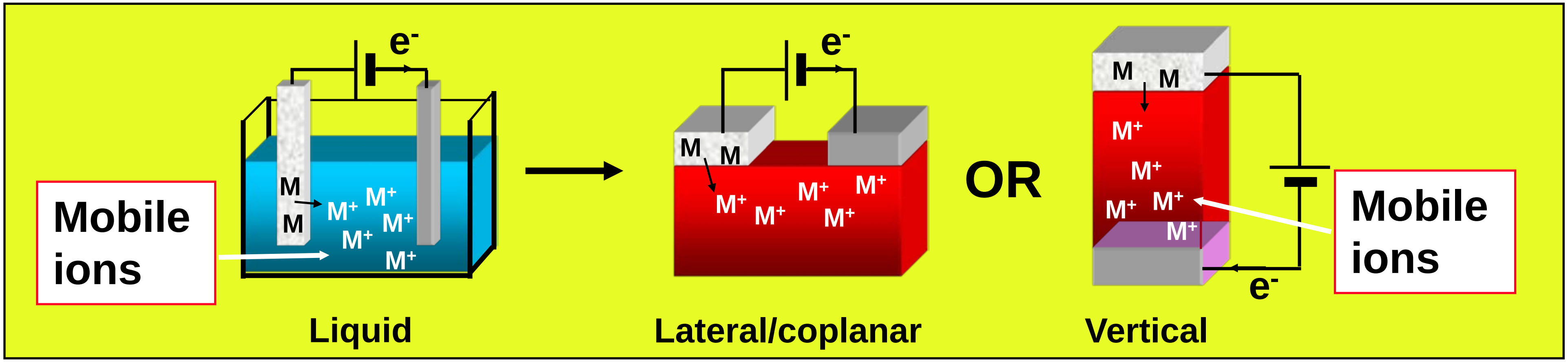
Solid electrolytes

- ***Solid electrolytes*** **behave like liquid electrolytes…**



- **Ions move under the influence of an electric field and *electrochemical reactions* are possible**

cathode (conductor): $M^+ + e^- \rightarrow M$ *reduction*

anode (with excess M): $M \rightarrow M^+ + e^-$ *oxidation*

…occurs at a *few 100 mV*

Physical changes in materials

- **"Heine Rohrer showed five examples of where, if the space becomes small, new phenomena happen… if the distance is very short, diffusion, atomic or ionic motion, is very fast."**

Interview with Masakazu Aono, ACS Nano, Vol. 1, No. 5, 379-383 (2007)

- **Physical changes can result in highly stable, widely-spaced resistance states**
  - **inherently non-volatile resistance levels**
  - **small # of atoms can lead to large macroscopic effects**
- **Filamentary processes are scalable as on-state resistance is independent of device area**
  - **filaments can have *atomic* radius (!?)**

Nanoionics-based resistive switching memories

Rainer Waser and Masakazu Aono

nature materials | VOL 6 | NOVEMBER 2007 | www.nature.com/naturematerials

…**ion-migration** effects are coupled to **redox processes** which cause the **change in resistance**. They are subdivided into **cation-migration** cells, based on the electrochemical **growth and dissolution of metallic filaments**, and **anion-migration** cells, typically realized with transition metal oxides as the insulator, in which **electronically conducting paths of sub-oxides are formed and removed**…

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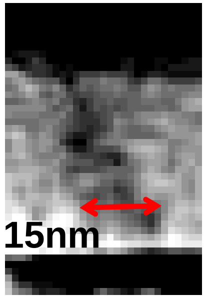
Cation-based *PMC* or *CBRAM* device

Cryo-TEM image of filament



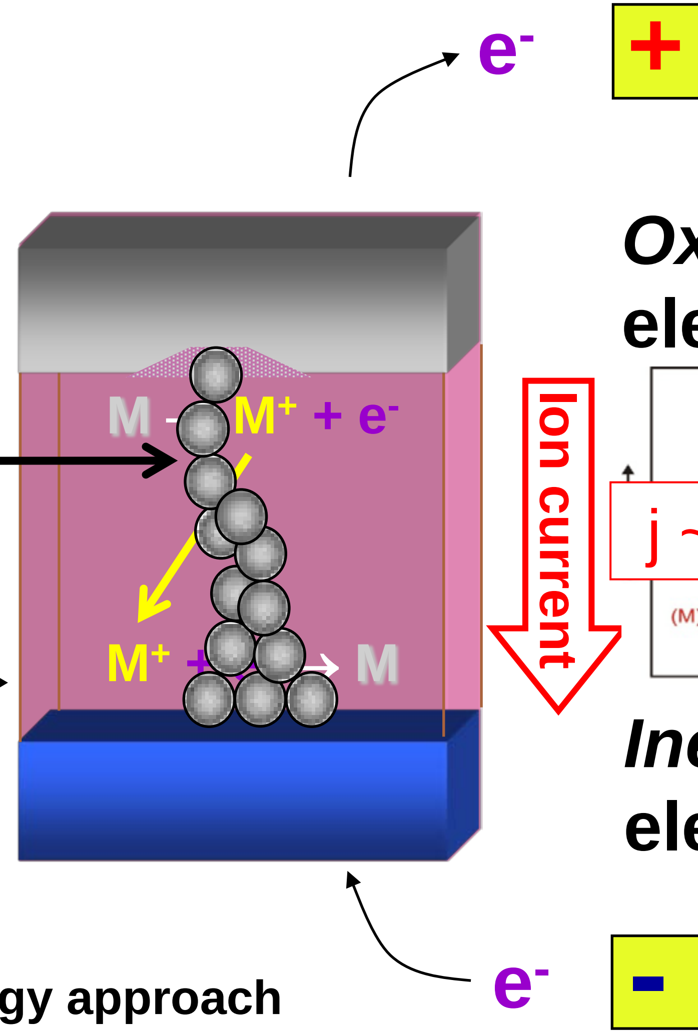
Metallic electrodeposit

low resistance

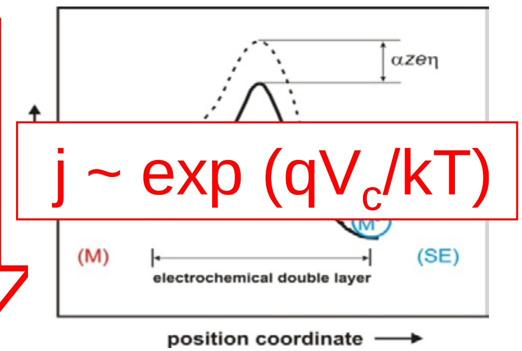
Glassy electrolyte

high resistance

Mobile ions added during processing or via *electroforming*



Oxidizable electrode



Inert electrode

Low energy approach

High energy approach

Reverse bias or high forward current dissolves electrodeposit

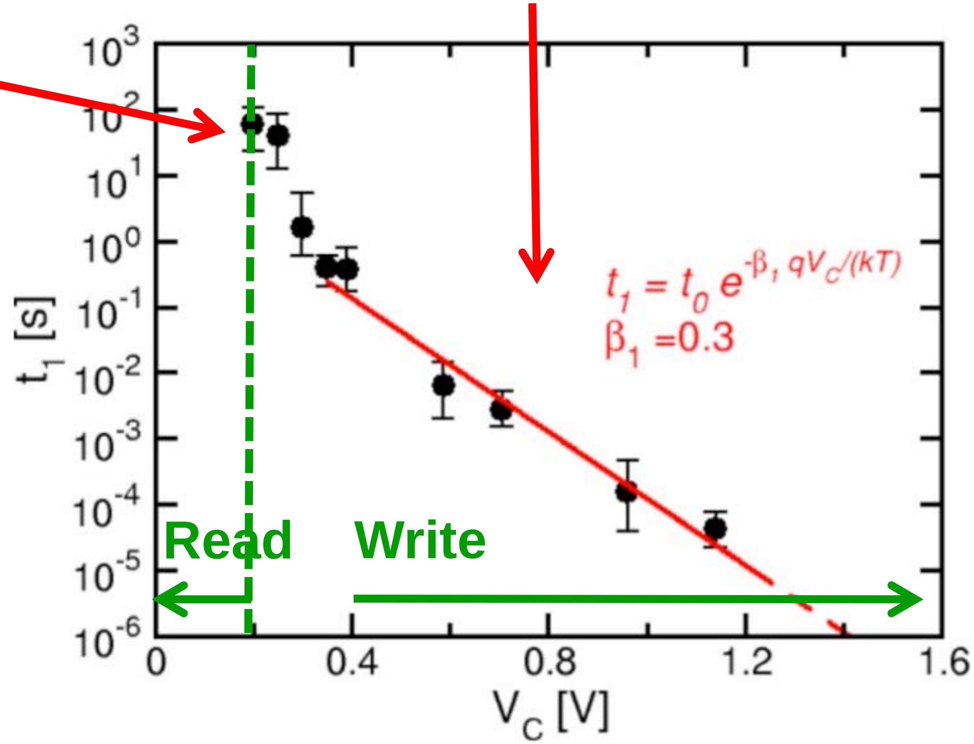
Note: Programmable Metallization Cell (PMC) is a platform technology for a variety of mass transport applications. Conductive Bridging Random Access Memory (CBRAM) is the term generally applied to memory applications of PMC.

Building a filament: voltage, time & charge

- **Total charge transferred in time t is** $Q_0 = jtA$
  - **A is the effective area of the electrodeposit**
  - $\mathbf{j} = j_0 \exp(\alpha q V_c / kT)$

$$t_{prog} = Q_0 / [\, j_0 \exp(\alpha q V_c / kT)\, A \,]$$

Saturation at low voltage (nucleation overpotential, work function difference, etc.?)



Q_0 is in the fC range (from electrodeposit volume) - gives programming energy in the order of fJ…

j_0=exchange current density, α =transfer coefficient, q=cation charge, V_c= cell voltage

U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, and M.N. Kozicki, "Study of Multilevel Programming in Programmable Metallization Cell (PMC) Memory," IEEE Transactions on Electron Devices, Vol. 56, 1040 – 1047 (2009).

Materials - electrolytes & electrodes

Electrolyte	Electrode metals	
	Ag anode	Cu anode
Ge_xS_y	*W*	*W*
Ge_xSe_y	*W, Ni, Pt*	*W*
Ge-Te	*TiW*	*TaN*
GST	*Mo*	
As-S	*Au*	
$Zn_xCd_{1-x}S$	*Pt*	
Cu_2S		*Pt, Ti*
Ta_2O_5		*Pt, Ru*
SiO_2	*Co*	*W, Pt, Ir*
WO_3	*W*	*W*
TiO_2	*Pt*	
ZrO_2	*Au*	
MSQ (SiO_2)	*Pt*	
CuTe/GdOx		*W*
Ge_xSe_y/SiO_x		*Pt*
Ge_xSe_y/Ta_2O_5		*W*
Cu_xS/Cu_xO		*Pt*
Cu_xS/SiO_2		*Pt*

I. Valov, R. Waser, John R. Jameson and M.N. Kozicki, "Electrochemical metallization memories—fundamentals, applications, prospects," Nanotechnology, vol. 22 (2011) doi:10.1088/0957-4484/22/25/254003

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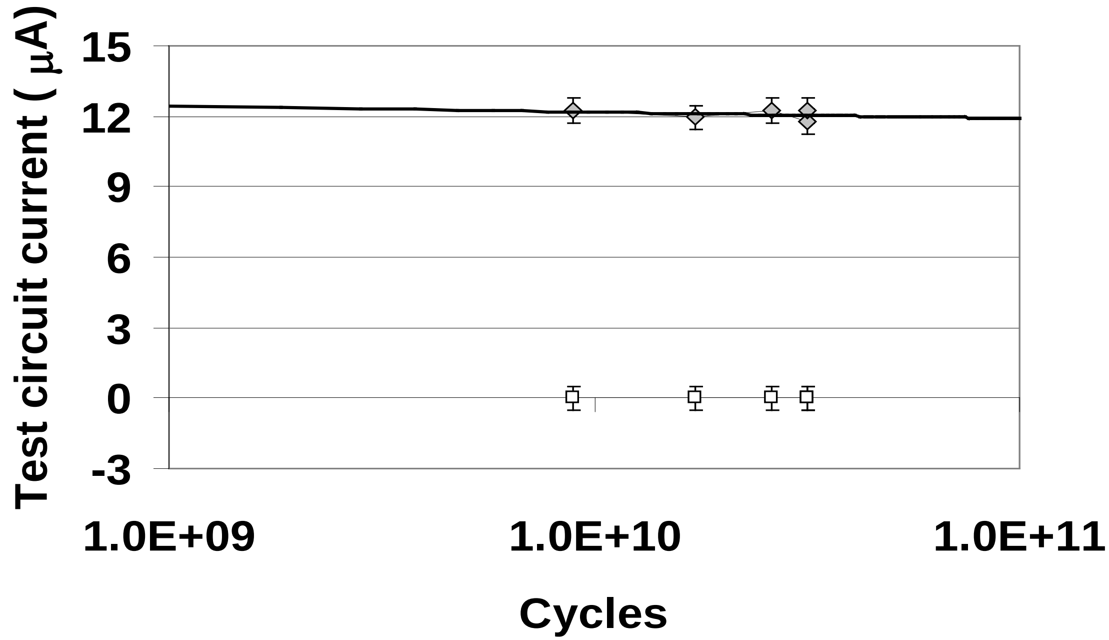
Endurance and retention

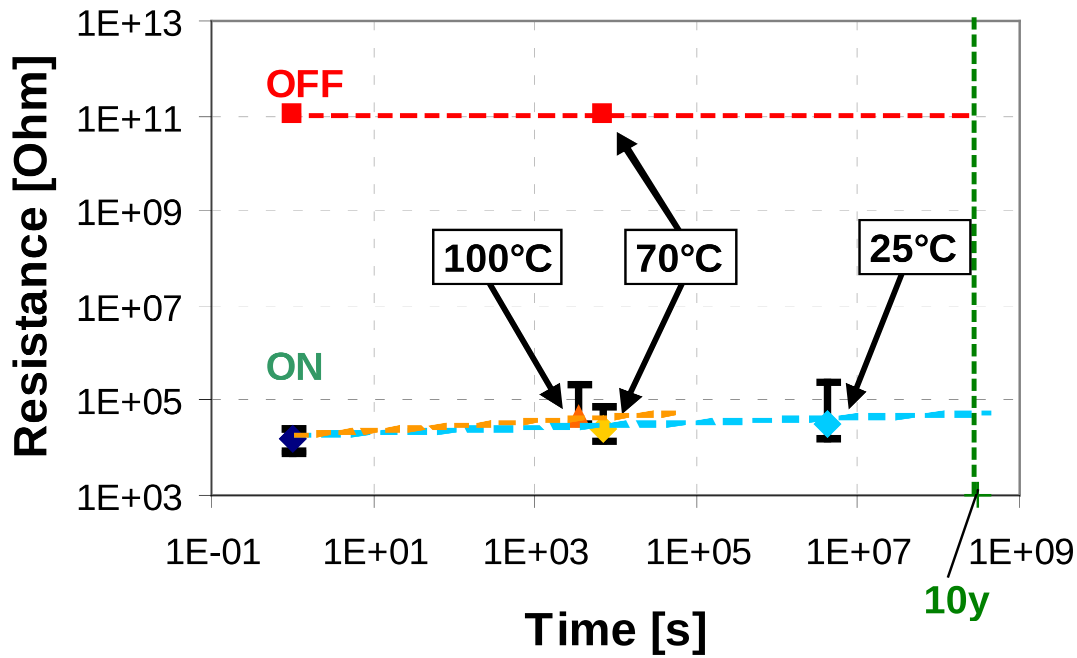
Endurance >10^{10} cycles with no degradation evident for 75 nm Ag-Ge-Se device (I_{prog}= 12 μA)

M.N. Kozicki, M. Park, and M. Mitkova, "Nanoscale Memory Elements Based on Solid-State Electrolytes," IEEE Trans. Nanotechnology, vol. 4, 331-338 (2005).

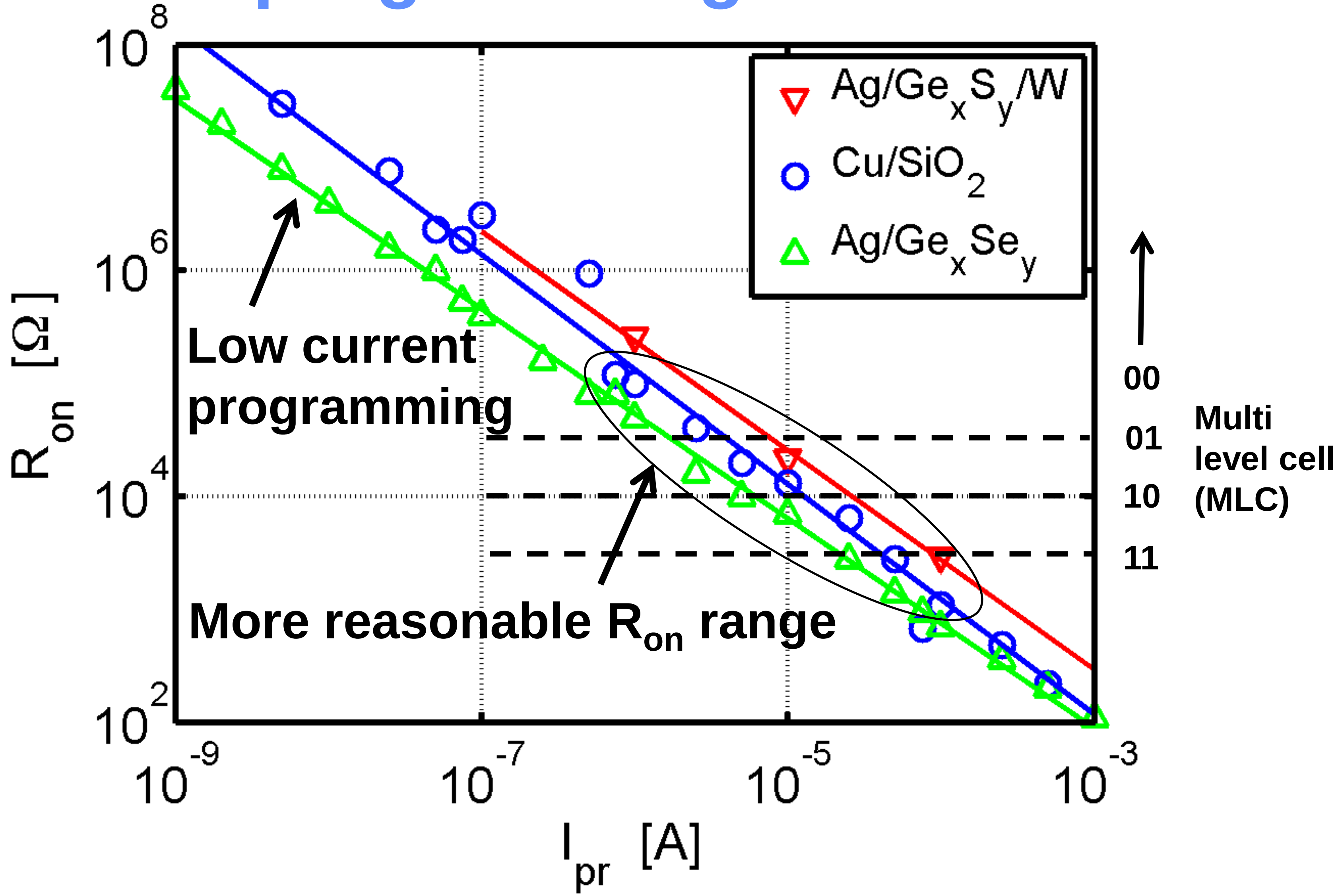


Retention >10 yrs at 100ºC for 90 nm Ag-Ge-S device (full wafer results)

R. Symanczyk, „Conductive Bridging Memory Development from Single Cells to 2Mbit Memory Arrays", 8th Non-Volatile Memory Technology Symposium, 2007.

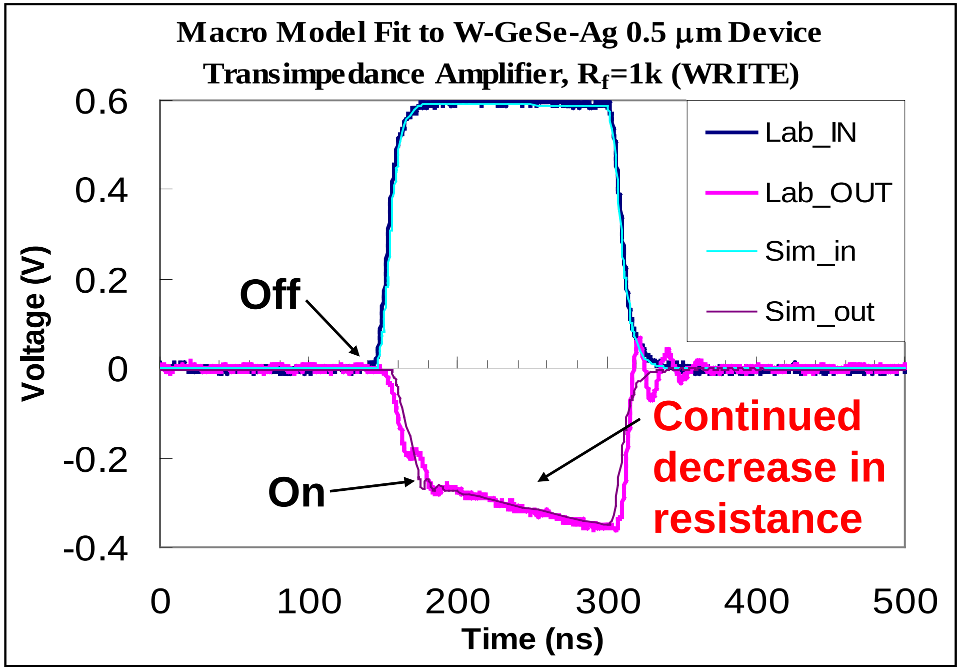


On-state resistance vs. programming current

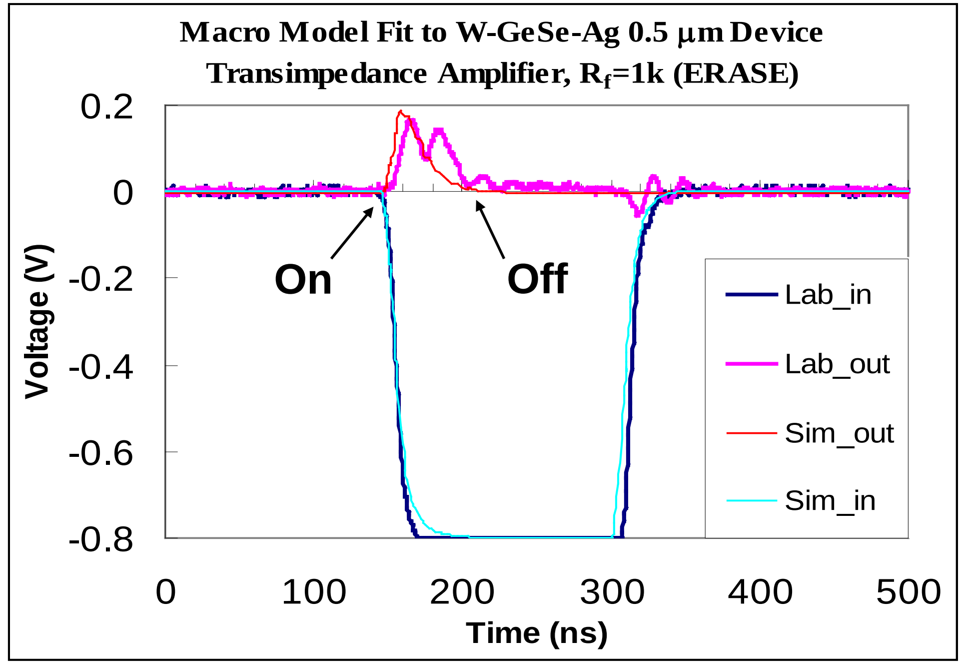


Data compiled by John Jameson, Adesto Technologies. Some data taken from R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges", Adv. Mater., Vol. 21, 2632–2663 (2009).

Dynamic programming of Ag-Ge-Se (fast) devices



Write

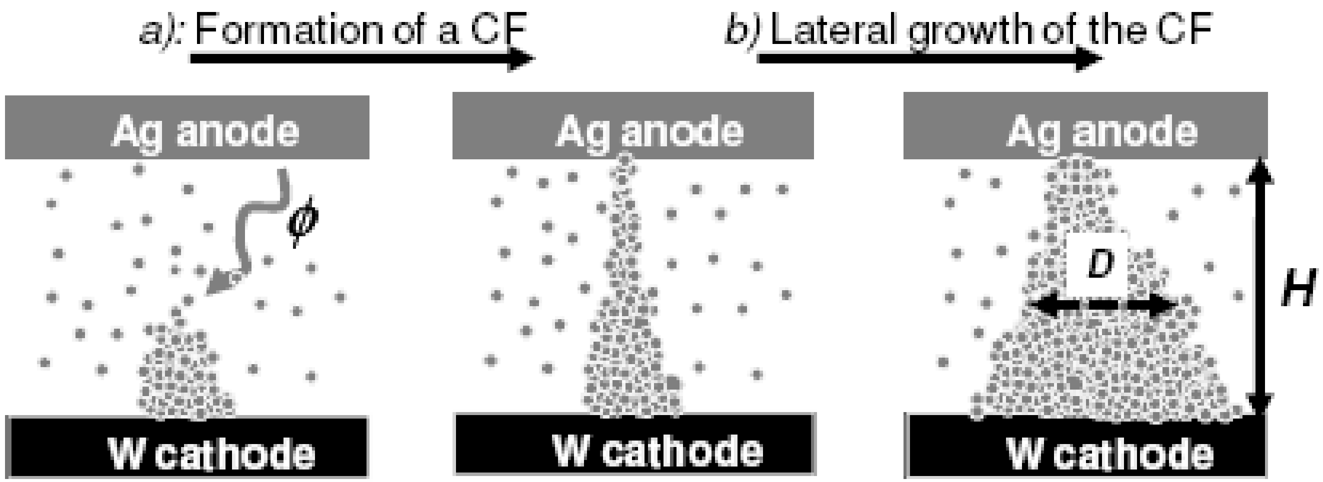


Erase

Output signal is via a transimpedance amplifier so that increasing voltage magnitude means increasing current (or decreasing device resistance)

N. Gilbert, C. Gopalan, and M. N. Kozicki, “A Macro model of Programmable Metallization Cell Devices,” Solid State Electronics, vol. 49, 1813-1819 (2005).

Schematic diagram of two-stage conducting filament formation process

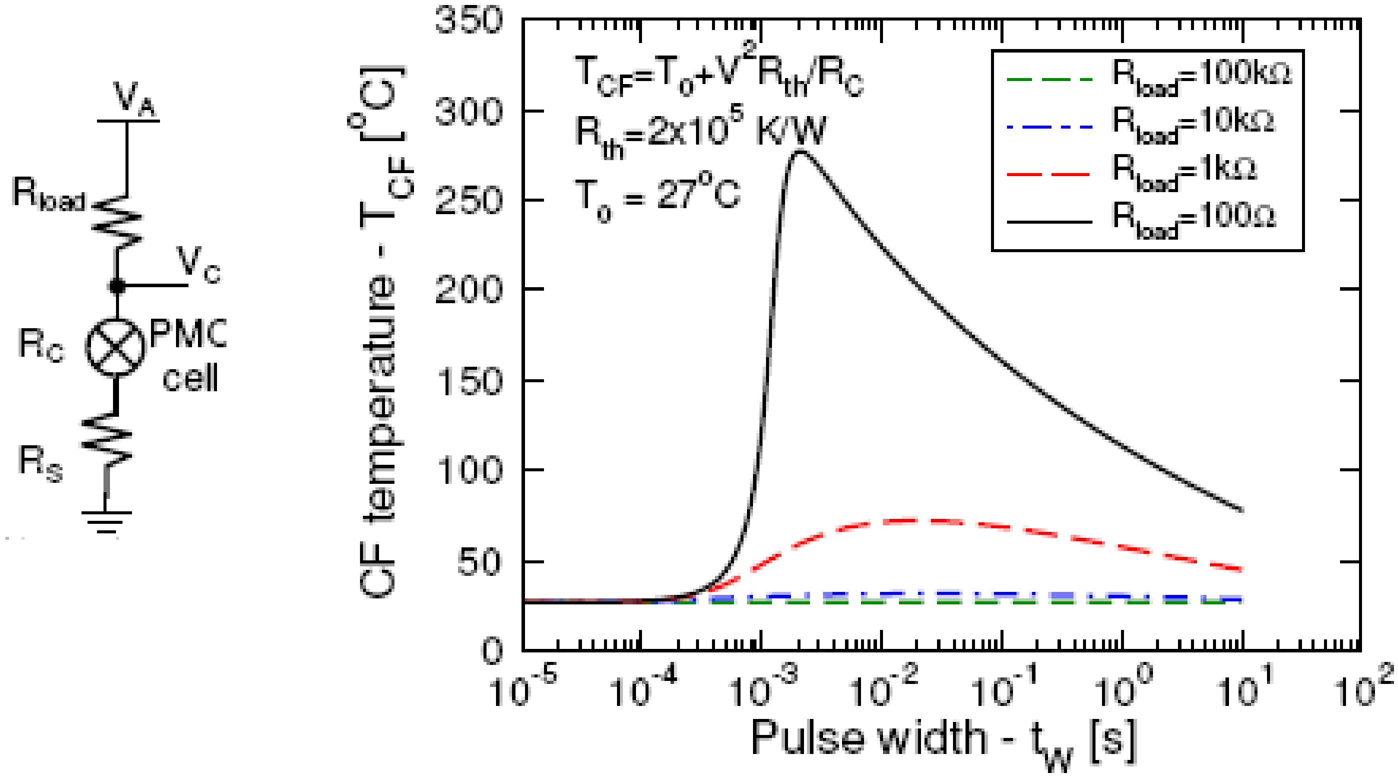


Both the *initial formation* and *radial growth* are driven by ion migration

But… is this everything?

U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, and M.N. Kozicki, "Study of Multilevel Programming in Programmable Metallization Cell (PMC) Memory," IEEE Transactions on Electron Devices, Vol. 56, 1040 – 1047 (2009).

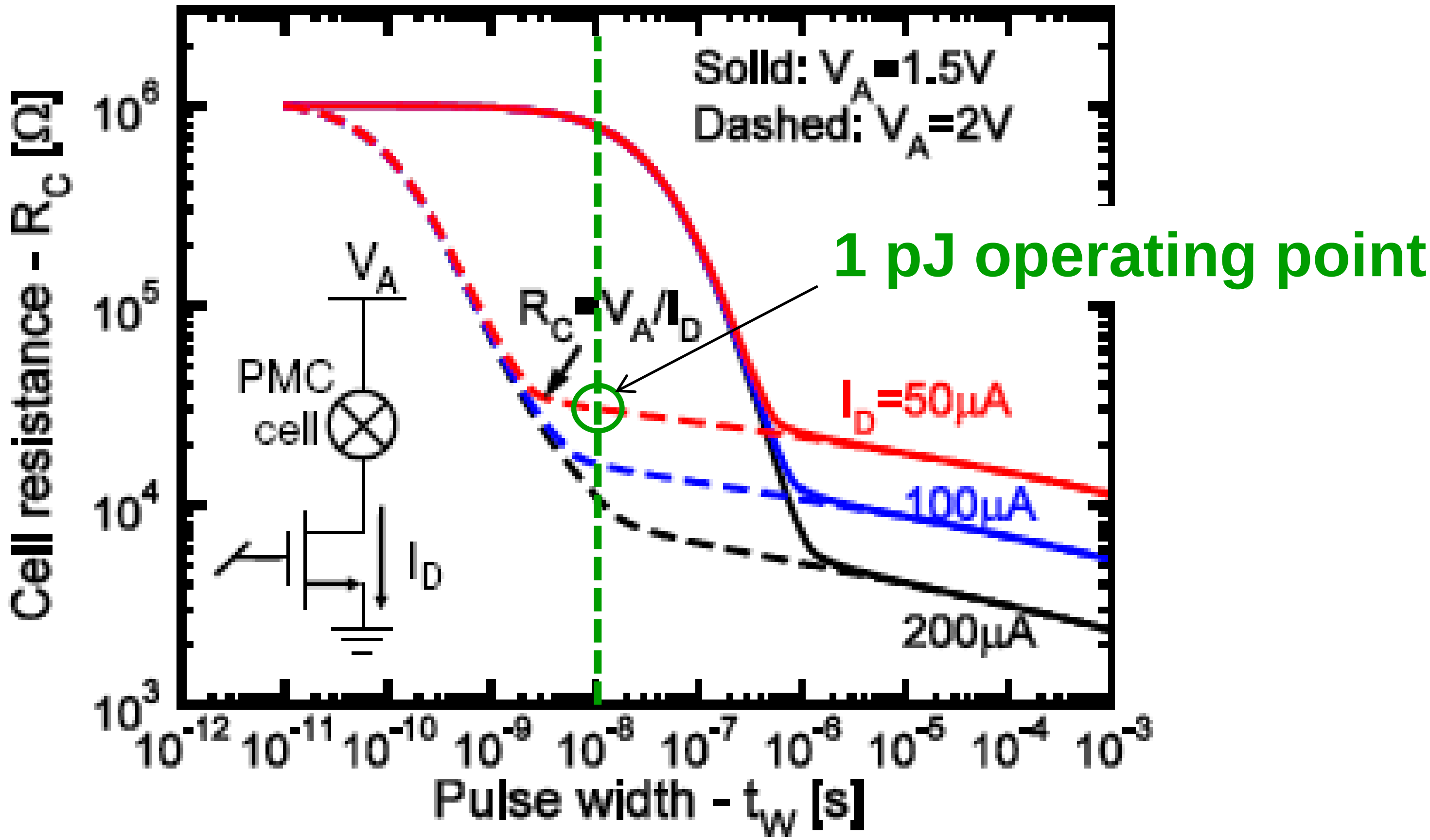
Joule heating during programming with high currents



- **Joule heating is evident at low R_{load}/high current**
- **Maximum temperature rise for 1 kΩ load is 40ºC**

U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, and M.N. Kozicki, “Study of Multilevel Programming in Programmable Metallization Cell (PMC) Memory,” IEEE Transactions on Electron Devices, Vol. 56, 1040 – 1047 (2009).

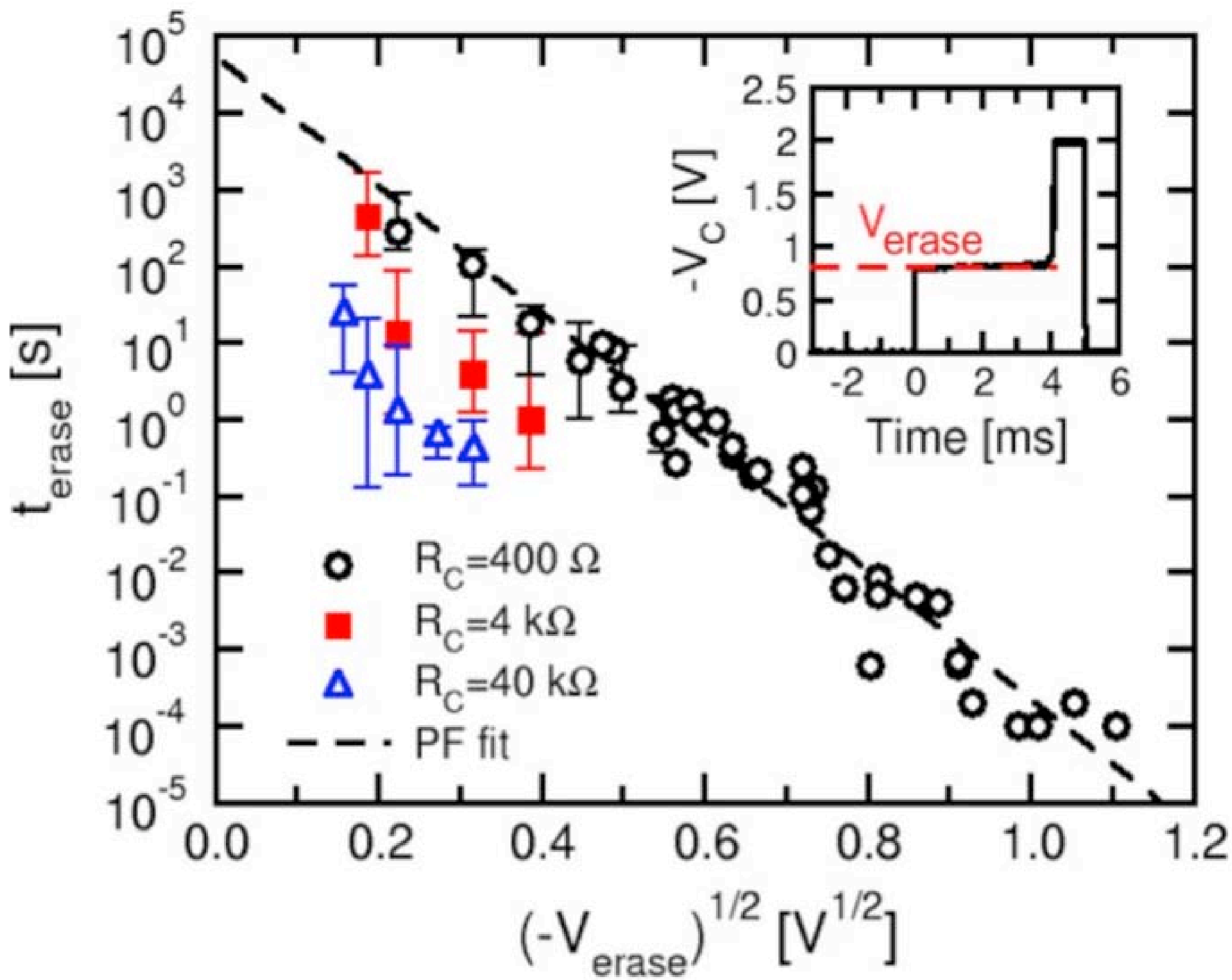
Conservative programming model



Model is based on a Ag/Ag-Ge-S/W 1T-1R cell and includes transistor load and Joule heating effects

U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, and M.N. Kozicki, “Study of Multilevel Programming in Programmable Metallization Cell (PMC) Memory,” IEEE Transactions on Electron Devices, Vol. 56, 1040 – 1047 (2009).

Dissolution kinetics



Erase time defined by 10x increase in resistance

D. Kamalanathan, U. Russo, D. Ielmini, and M.N. Kozicki, "Voltage-Driven On–Off Transition and Tradeoff With Program and Erase Current in Programmable Metallization Cell (PMC) Memory," IEEE Electron Device Letters, Vol. 30, 553 – 555 (2009).

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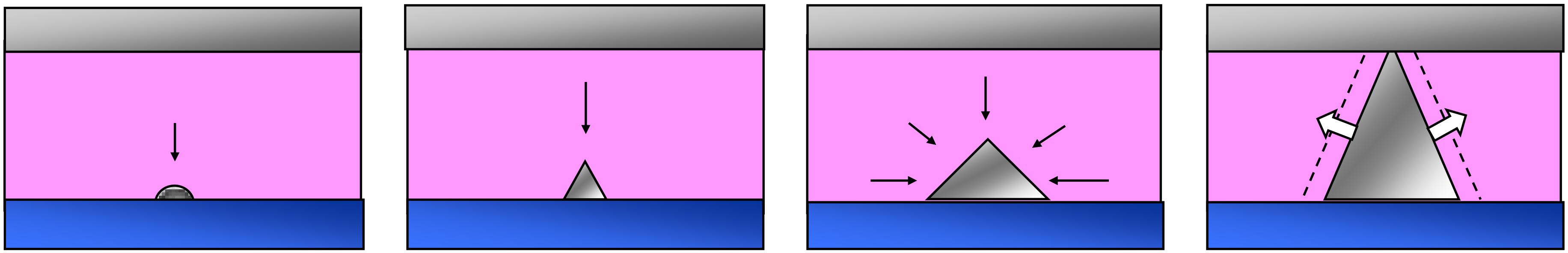
Photo: Chakku Gopalan

Electrodeposit evolution in a homogeneous solid electrolyte



1,2D nucleation | **Outward growth** | **3D growth** | **Radial growth**

Growth speed of a (cylindrical) nanofilament

$$\dot{h}[\text{cm/s}] = \frac{M_{\text{A}}}{\pi r^2 z N_{\text{A}} e_0 \rho} I[\text{A}]$$

M_A=atomic mass
N_A=Avogadro's #
Ze_0=charge on ion
ρ=filament density
r=filament radius

Example: Ag filament of 10nm diameter at *I* = 1 μA

$$\rightarrow \dot{h} \sim 1.3\,\text{m/s}$$

From *ion velocity* considerations, v = μ.Ɛ = 5 x 10^{-8} m^2/Vs . 2 x 10^7 V/m = 1 m/s

Where do the metallic filaments form?

Jaakko Akola
University of Jyväskylä and Tampere Technological University, Finland

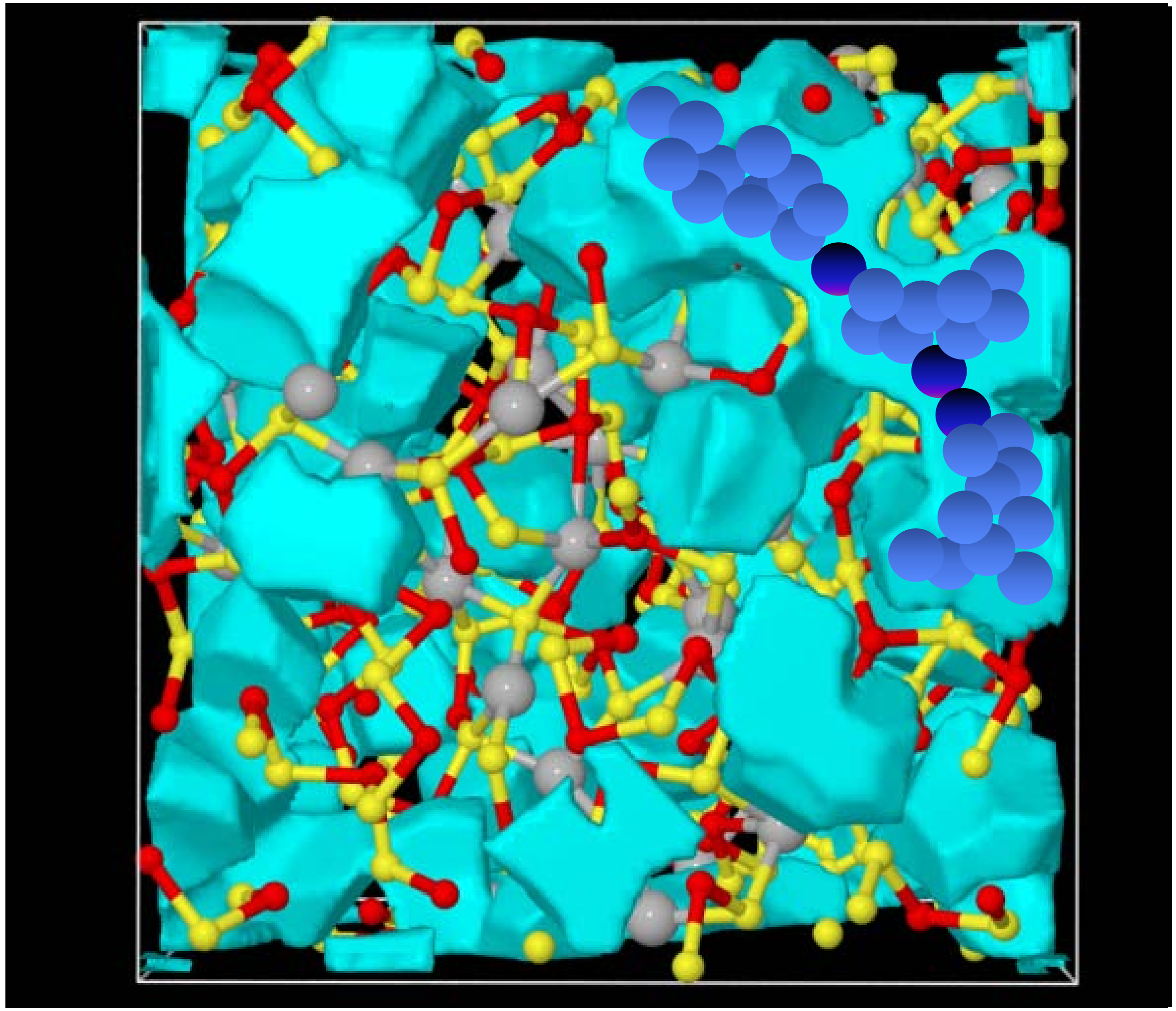
Bob Jones
Jülich Research Center, Germay

Tomas Wagner
University of Pardubice, Czech Republic

Techniques:

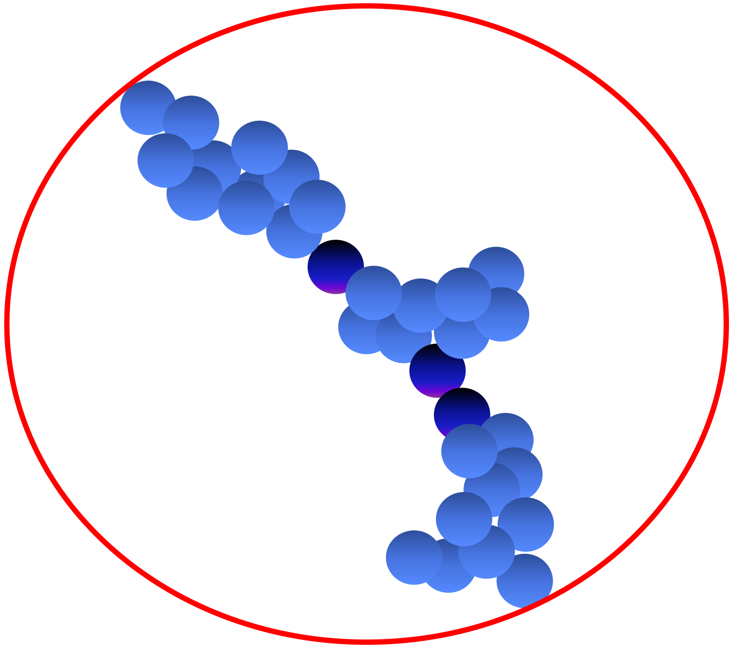
Full DFT, 500 atom system

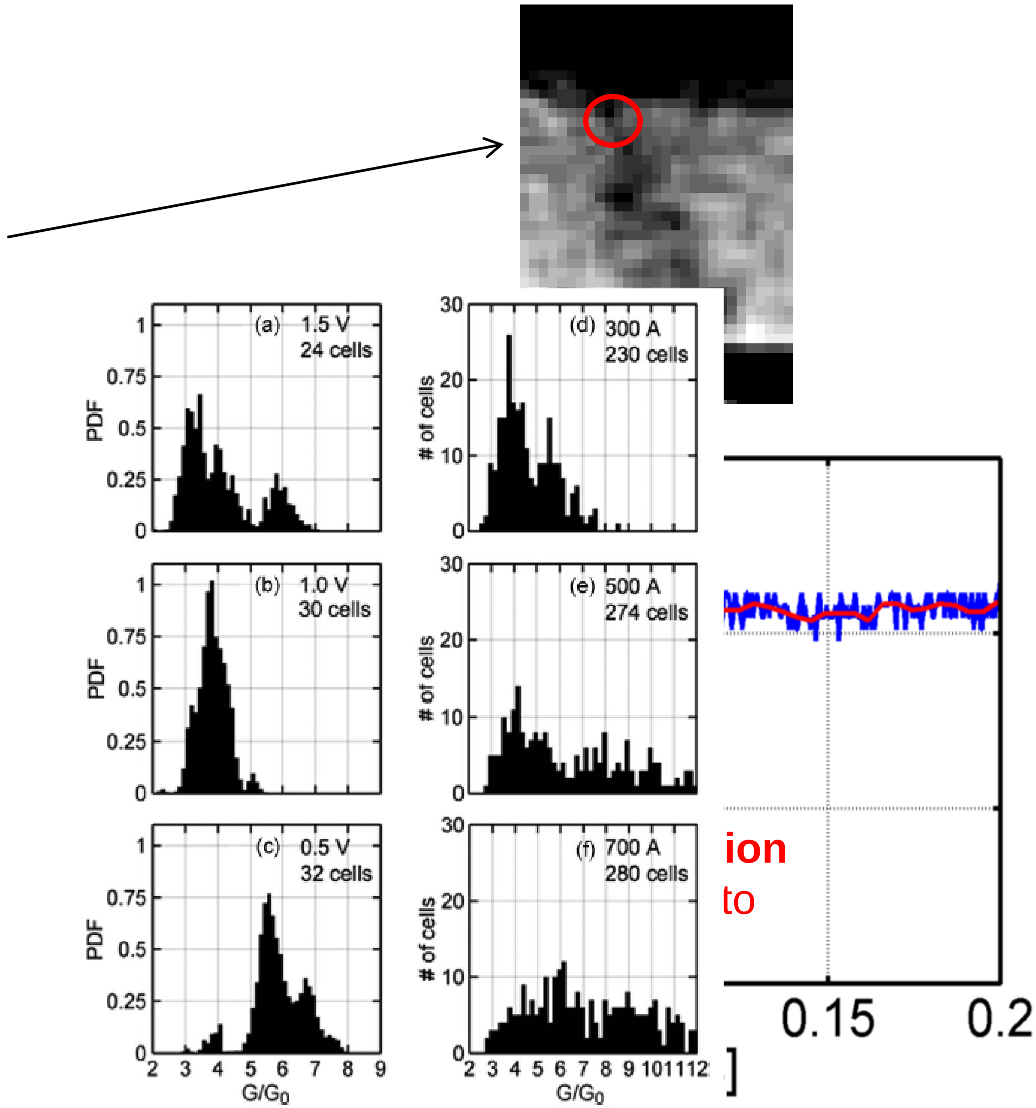
X-ray diffraction, neutron scattering, EXAFS



Cavities comprise 24% of the volume of $Ag_{12}As_{35}S_{53}$

Filament morphology





Full filament is probably composed of few to many *nano-filaments* in series/parallel bundles.

J.R. Jameson, N. Gilbert, F. Koushan, J. Saenz, J. Wang, S. Hollmer, M. Kozicki, and N. Derhacobian., *"Quantized Conductance in Ag/GeS_2/W Conductive-Bridge Memory Cells,"* IEEE Elec. Dev. Lett., vol. 33, 256-259 (2012).

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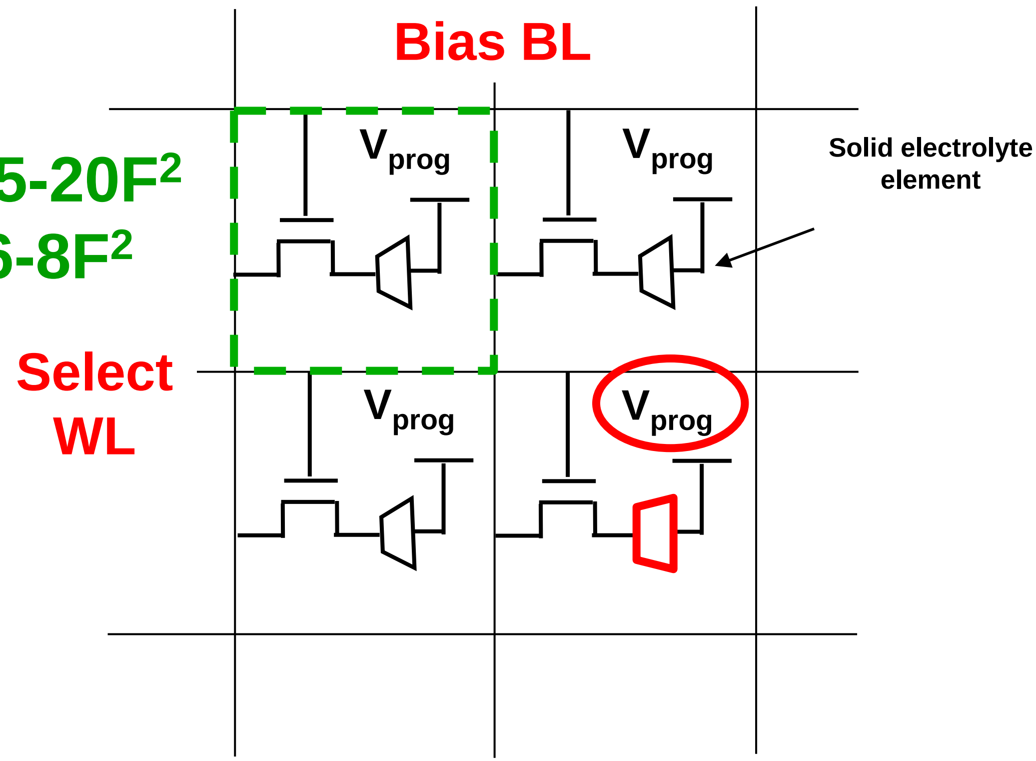
Array options

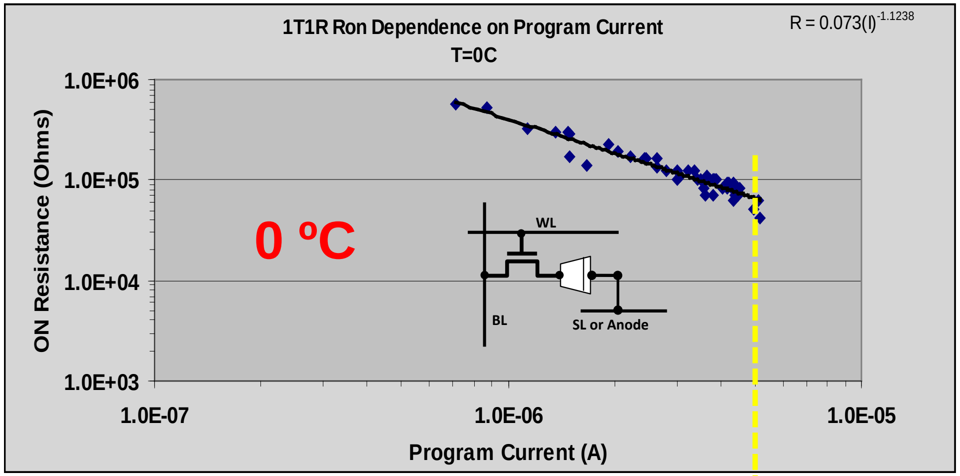
Active (1T-1R)

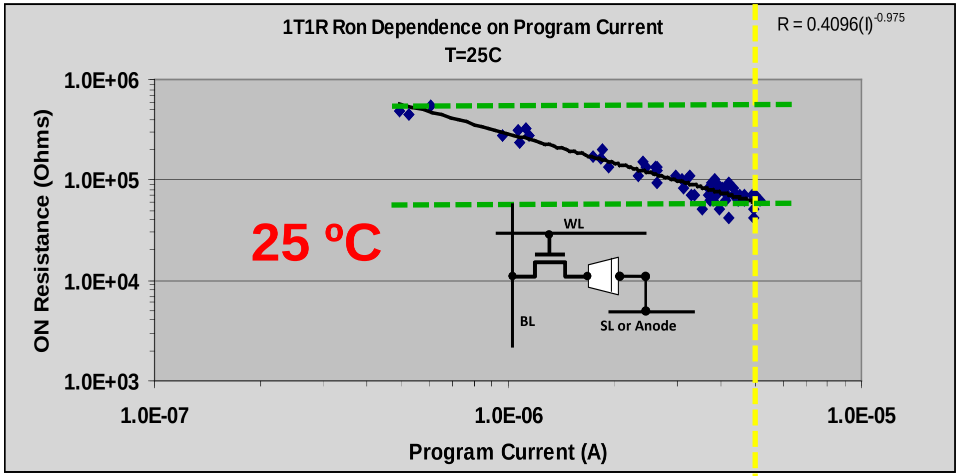
Logic 15-20F^2
DRAM 6-8F^2

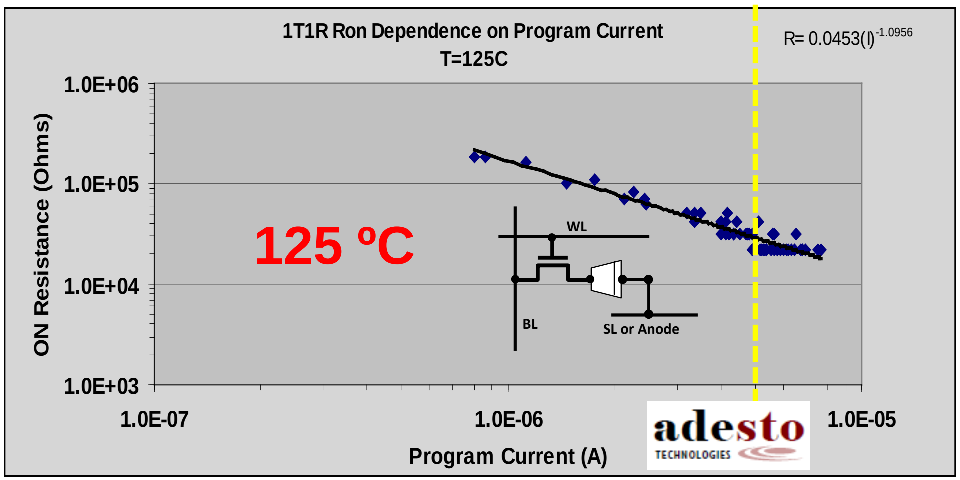


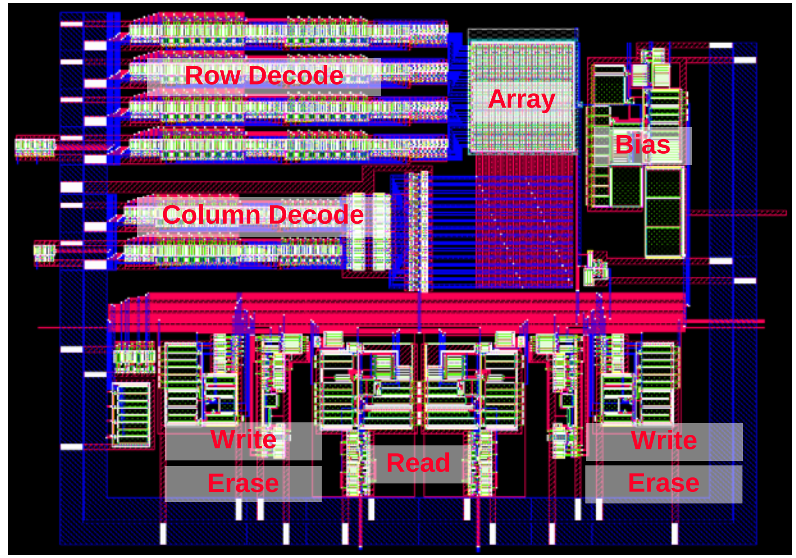
V_{prog} is above or below transistor drain voltage to program or erase selected cell, programming current via bit line (BL)

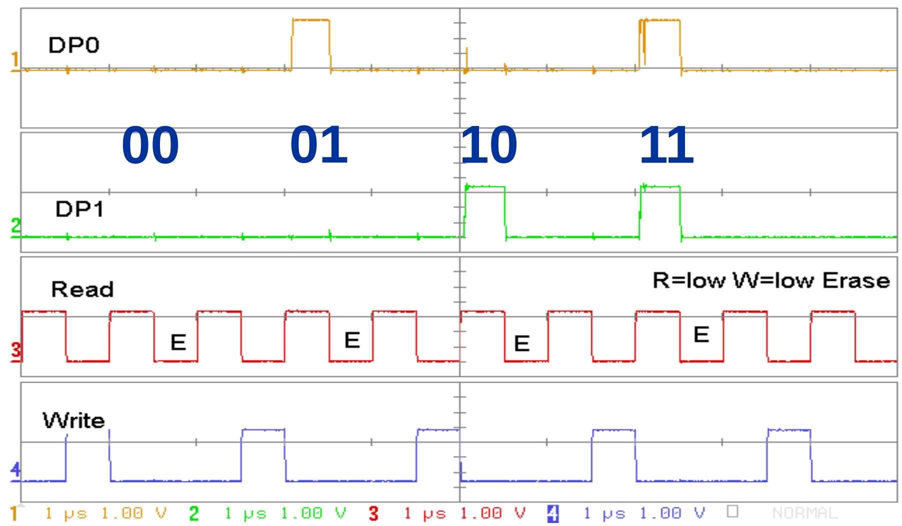
MLC storage in 1T-1R arrays





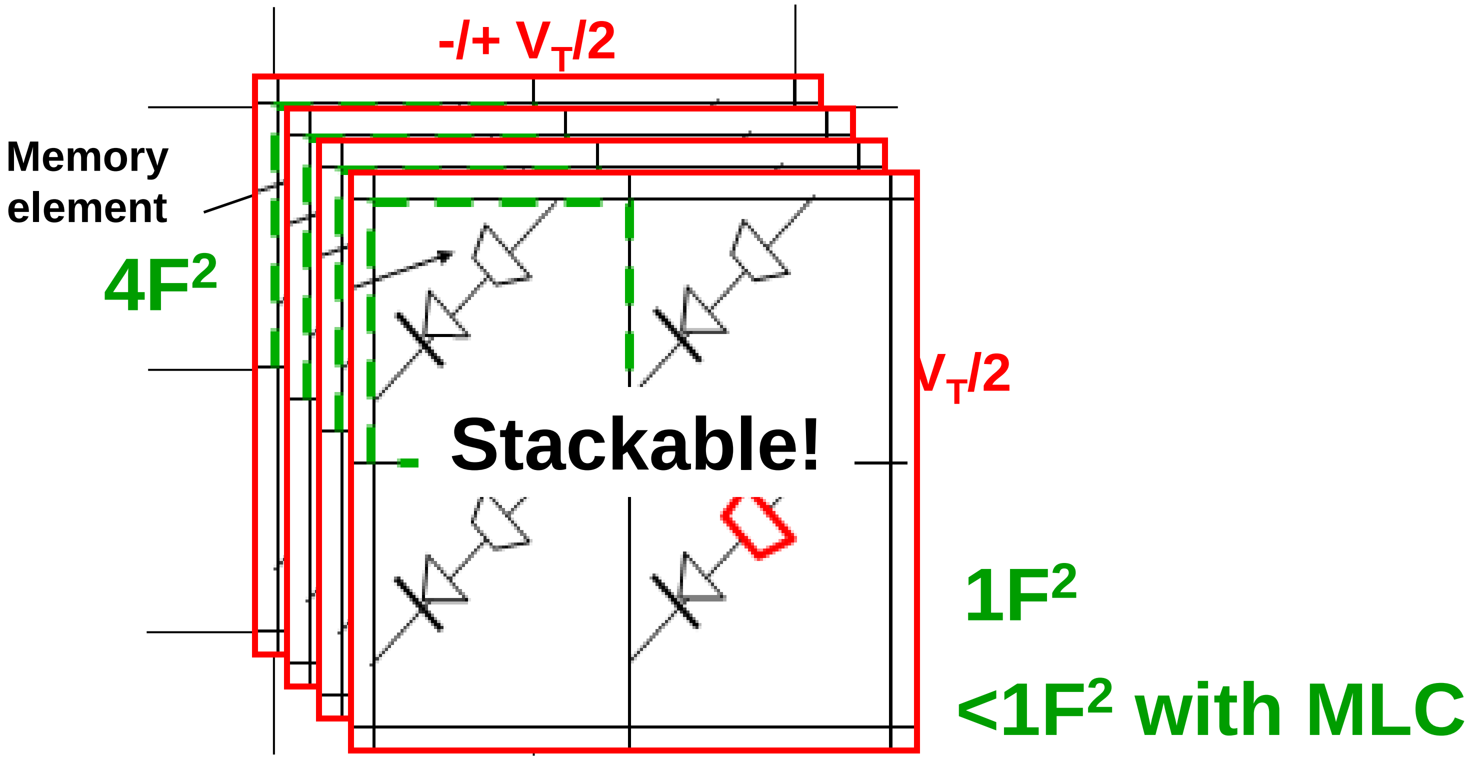






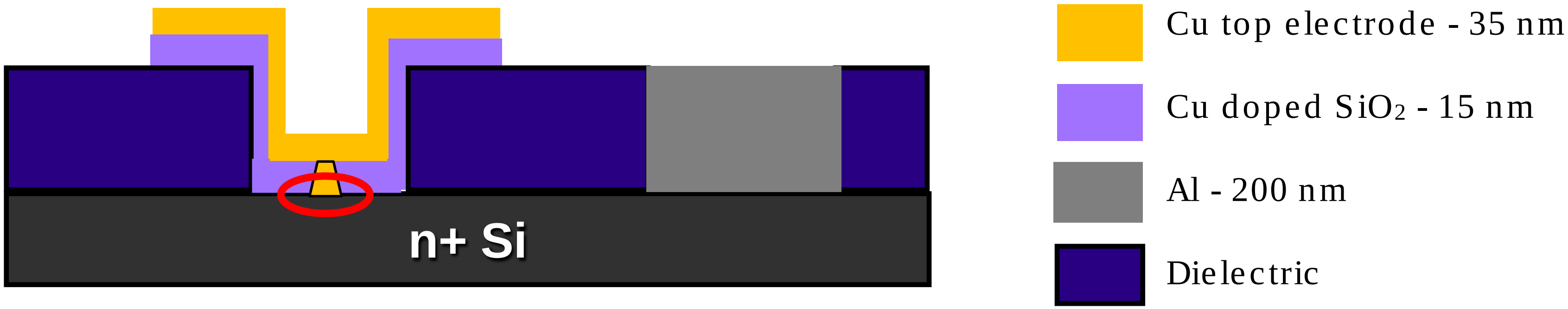
N.E. Gilbert and M.N. Kozicki, *"An Embeddable Multilevel-Cell Solid Electrolyte Memory Array,"* IEEE Journal of Solid-state Circuits, vol. 42, no. 6, pp 1383-1391, June 2007

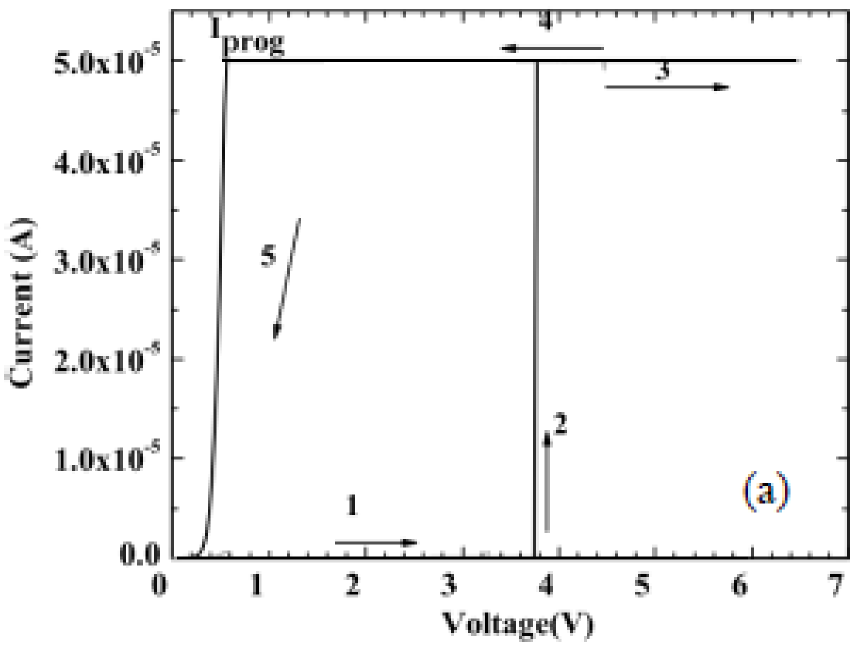
Benefits of passive arrays



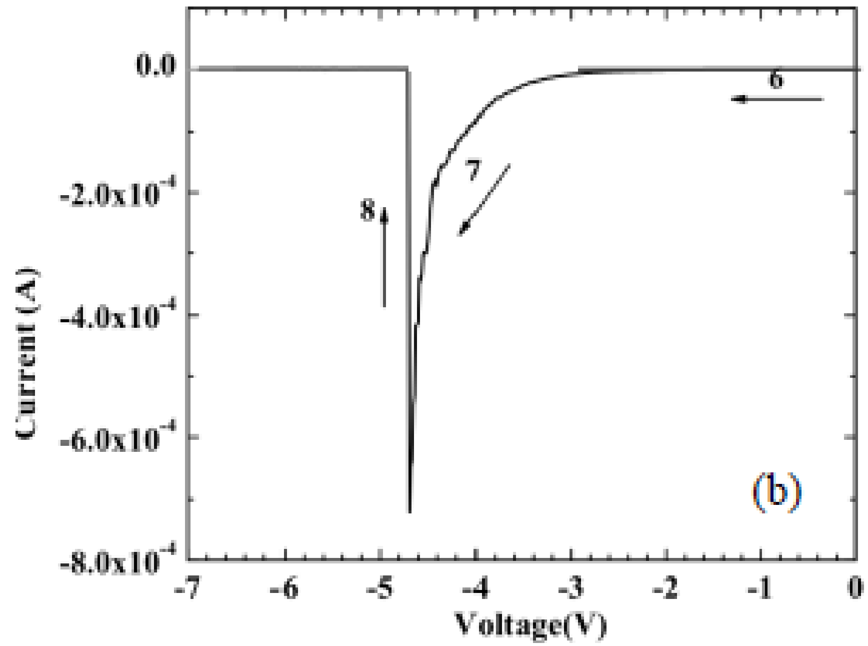
Selected cell has +/-half threshold voltage on row and -/+half on column for write or erase

Integrated diode isolation





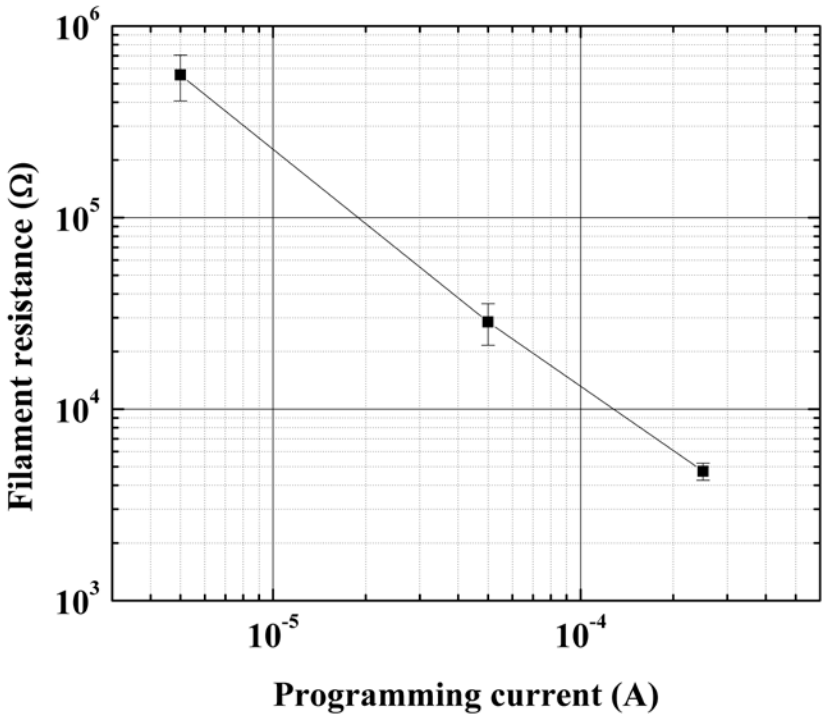
Write

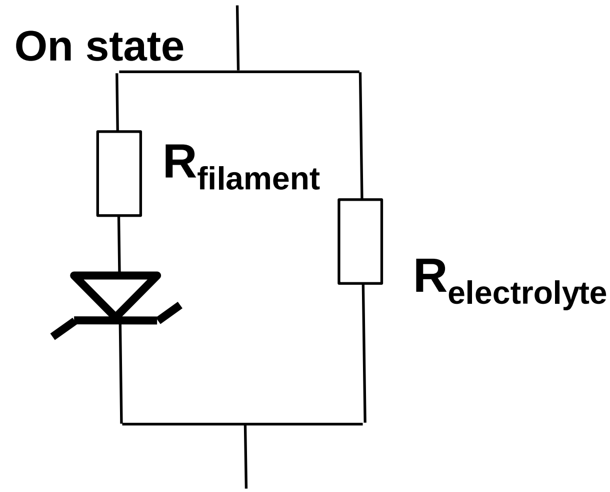


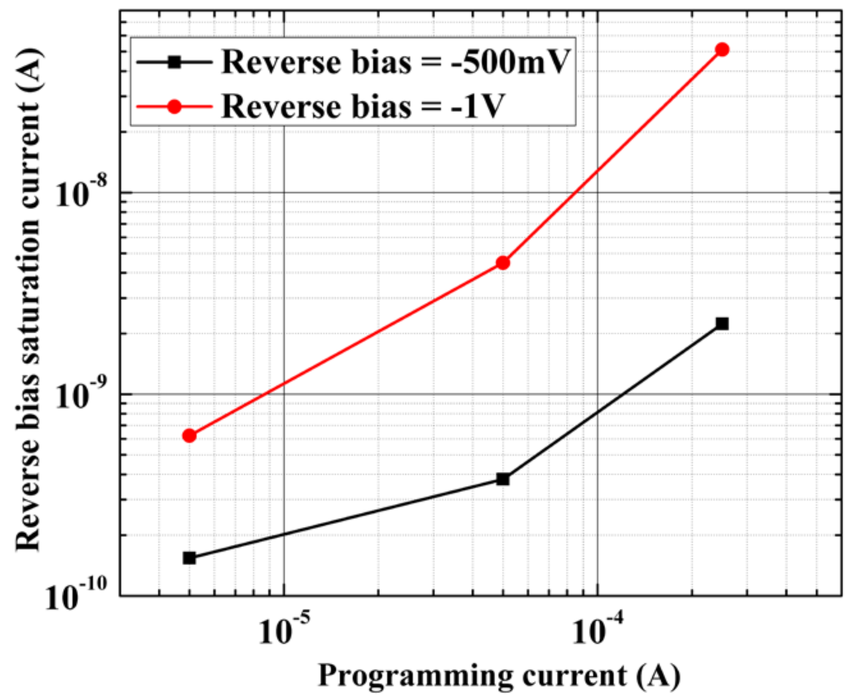
Erase

Sarath C. Puthentheradam, Dieter K. Schroder, and Michael N. Kozicki, “Inherent diode isolation in programmable metallization cell resistive memory elements,” Appl. Phys. A (2011) 102: 817–826.

Diode device characteristics







Saturation current scales with programming current

- ***depends on filament area***

Sarath C. Puthentheradam, Dieter K. Schroder, and Michael N. Kozicki, "Inherent diode isolation in programmable metallization cell resistive memory elements," Appl. Phys. A (2011) 102: 817–826.

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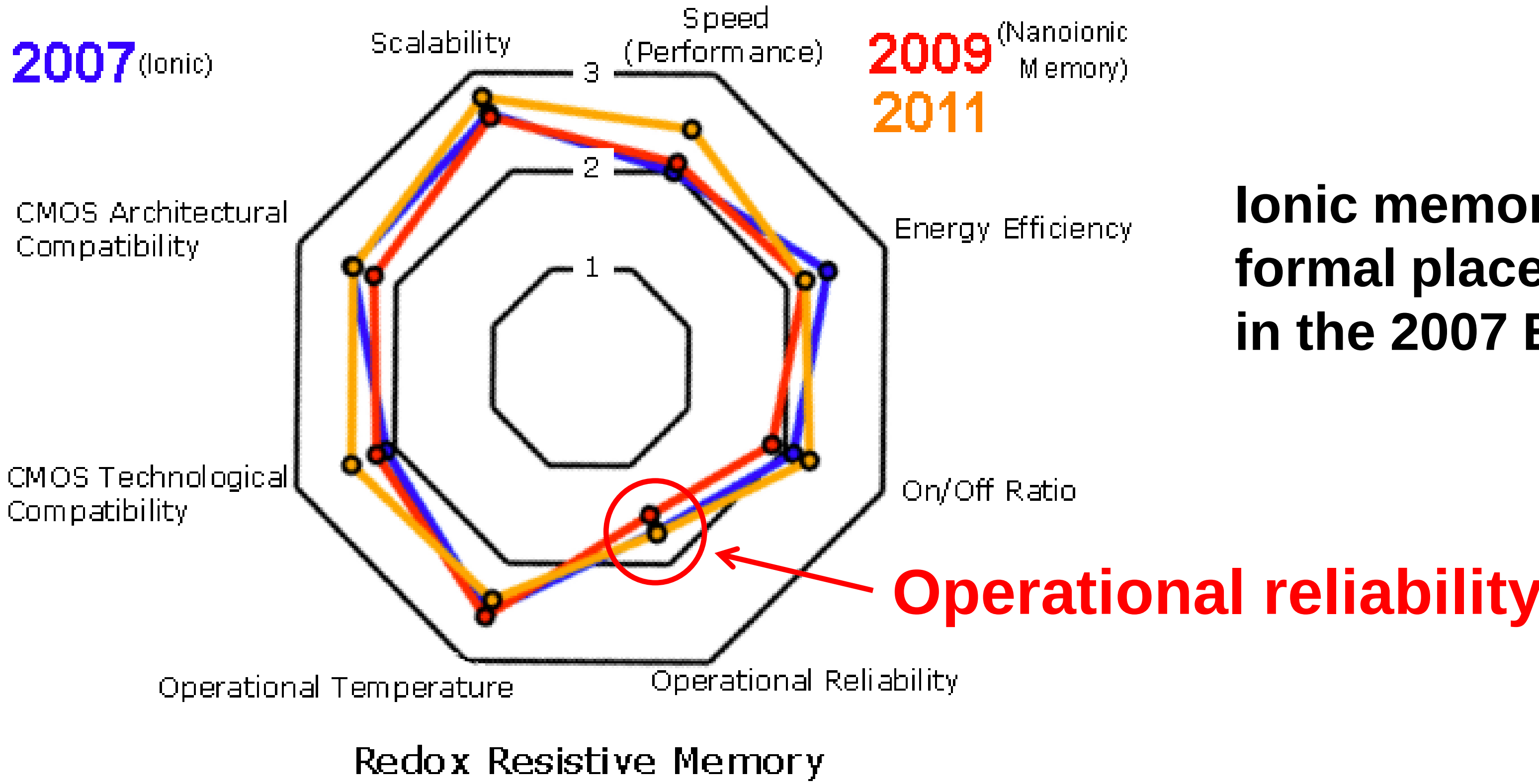
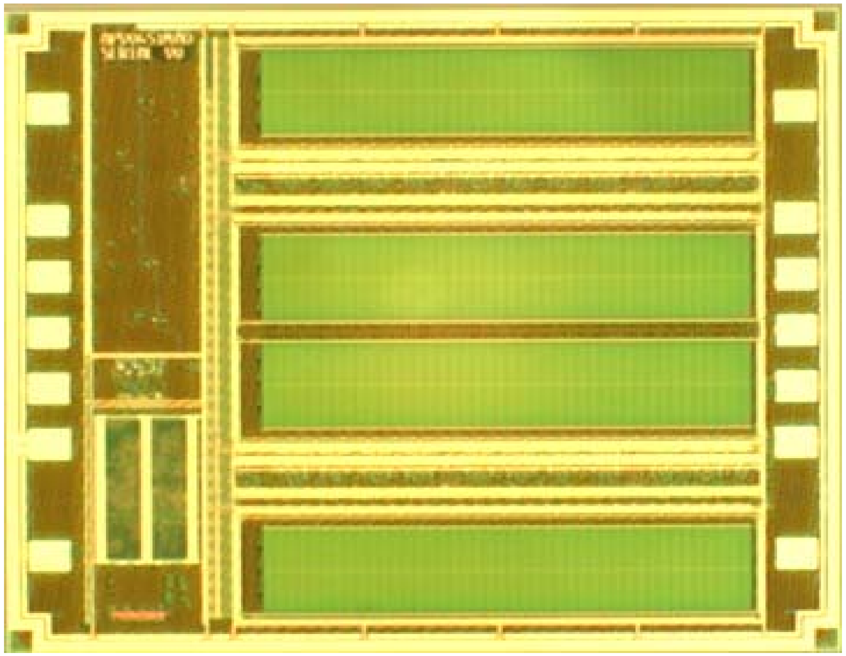
International Technology Roadmap for Semiconductors

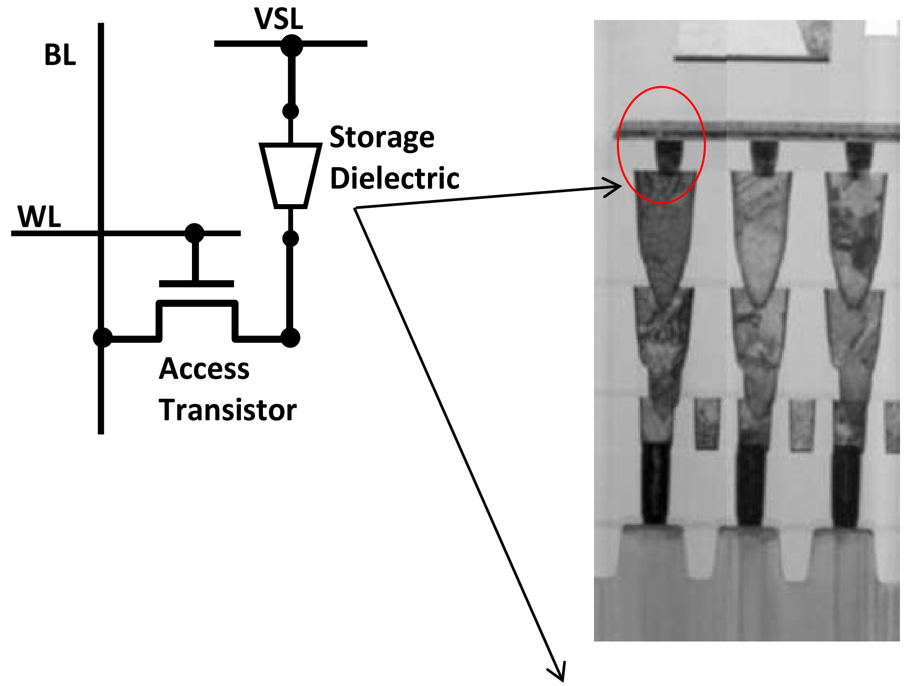


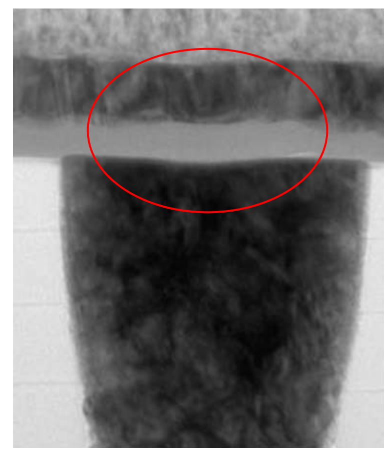
Ionic memory gained a formal place in the ITRS in the 2007 Edition

Many aspects of ionic/redox memory look extremely promising but "operational reliability" has been ranked low since 2007…

1Mb 130nm (Cu BEOL) integration



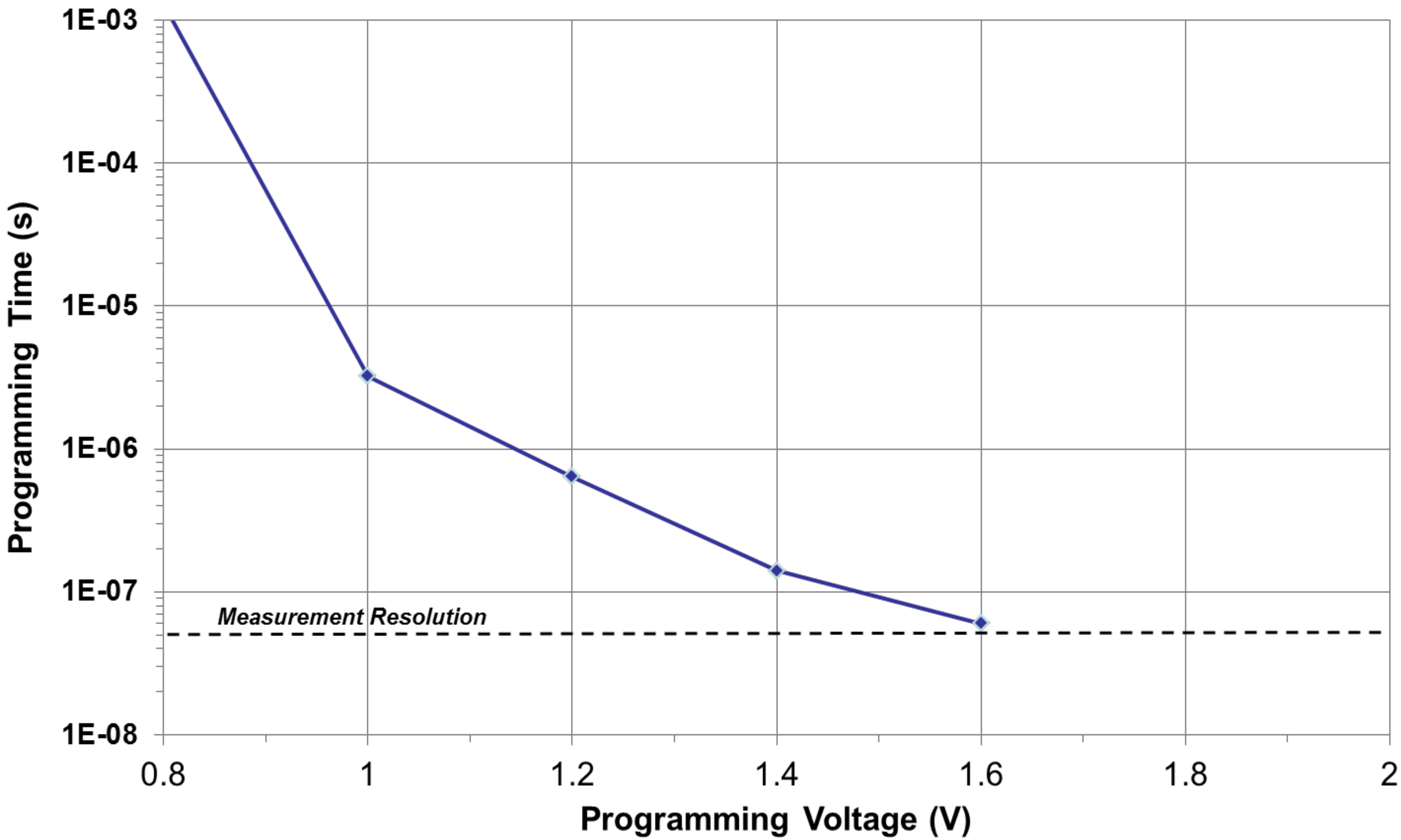




Salient Features:

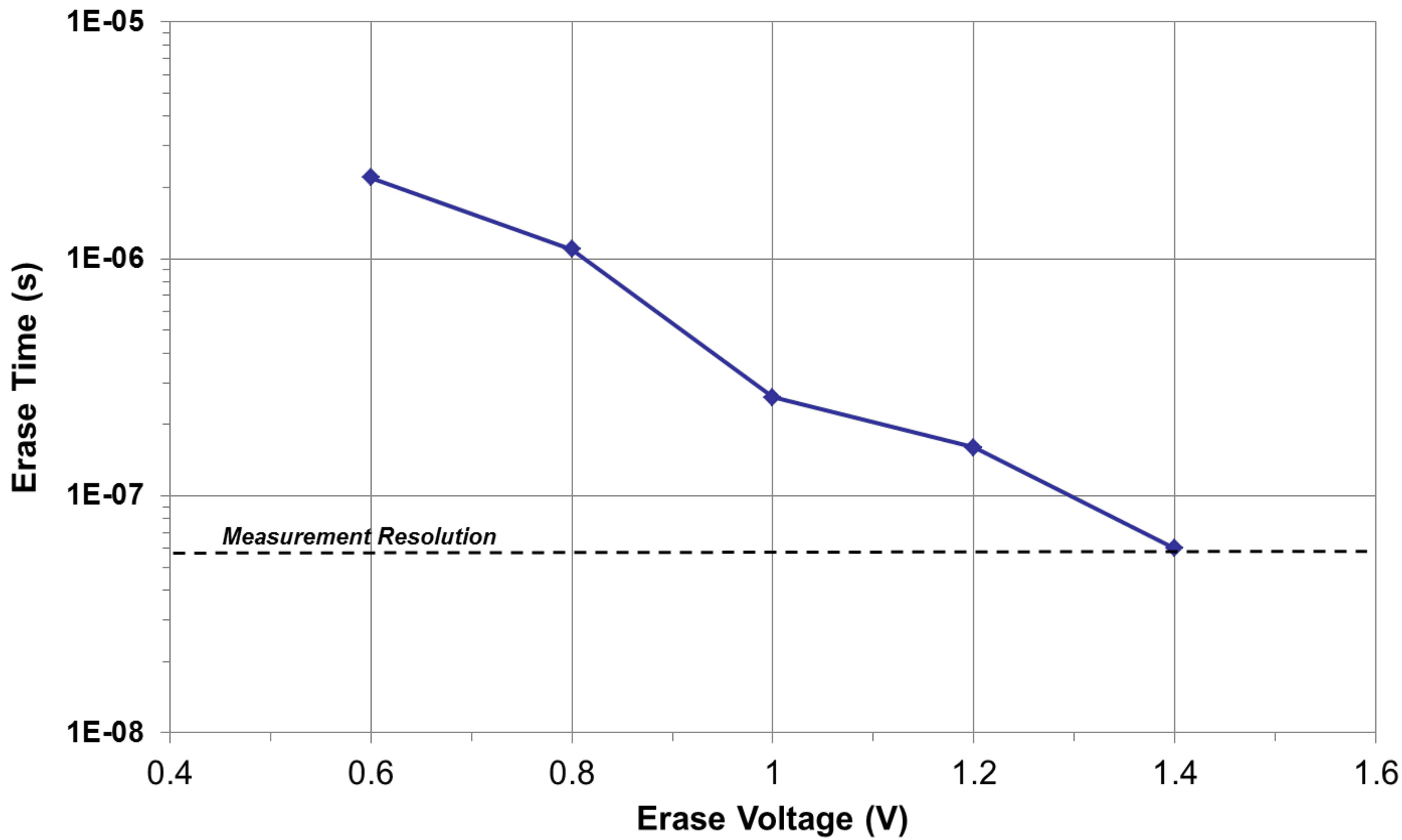
- 1Mb EEPROM/Flash Macro on Standard Foundry 130nm
- Programmable elements requires 2 non critical masks in BEOL flow
- Cell size determined by access device, core cell will scale with CMOS

1Mb program performance capability



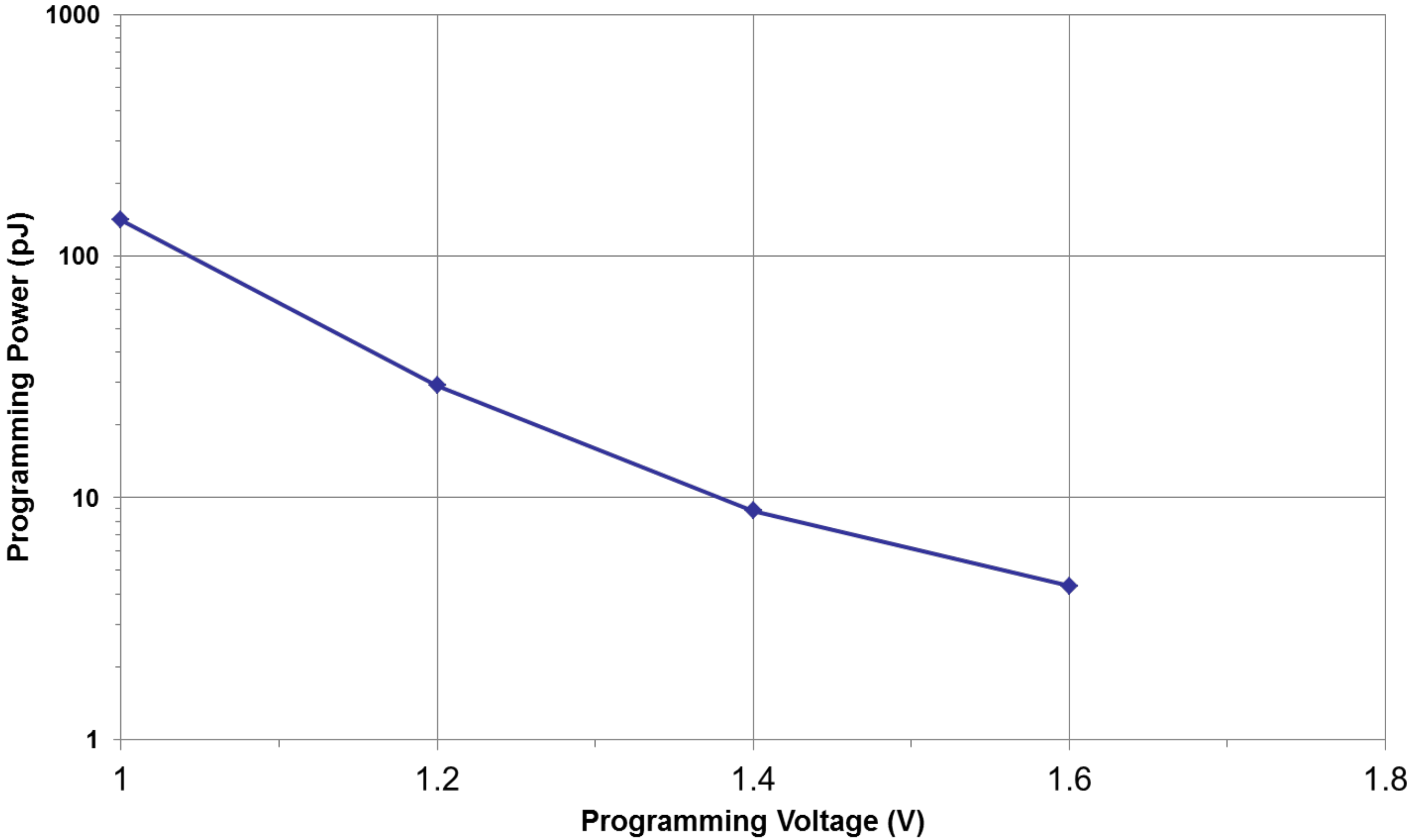
Programming capability to sub-1V regime
Higher speed can be achieved with optimized materials

1Mb erase performance capability



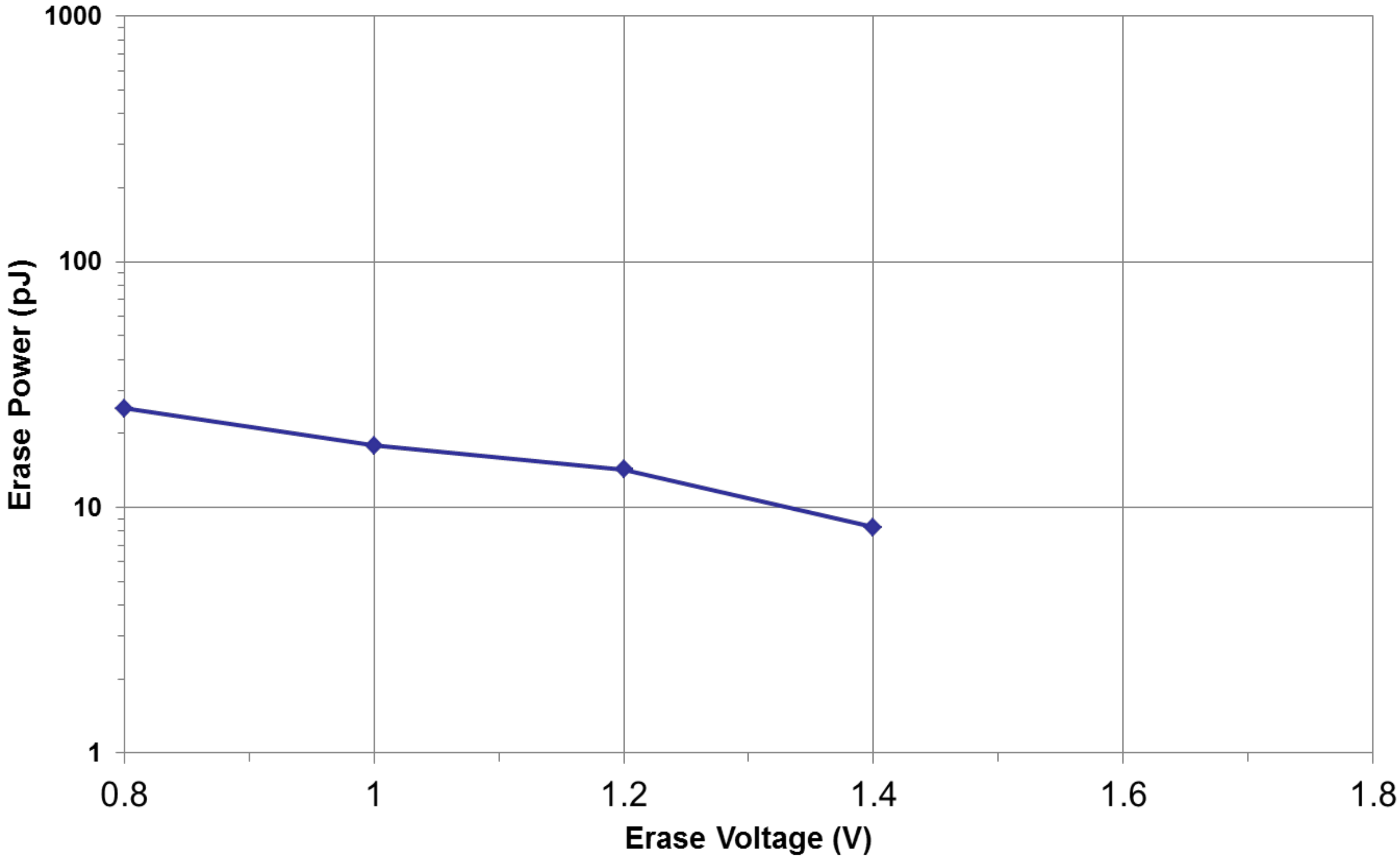
Erase capability to sub-1V regime with sub-μs erase speed

1Mb programming energy



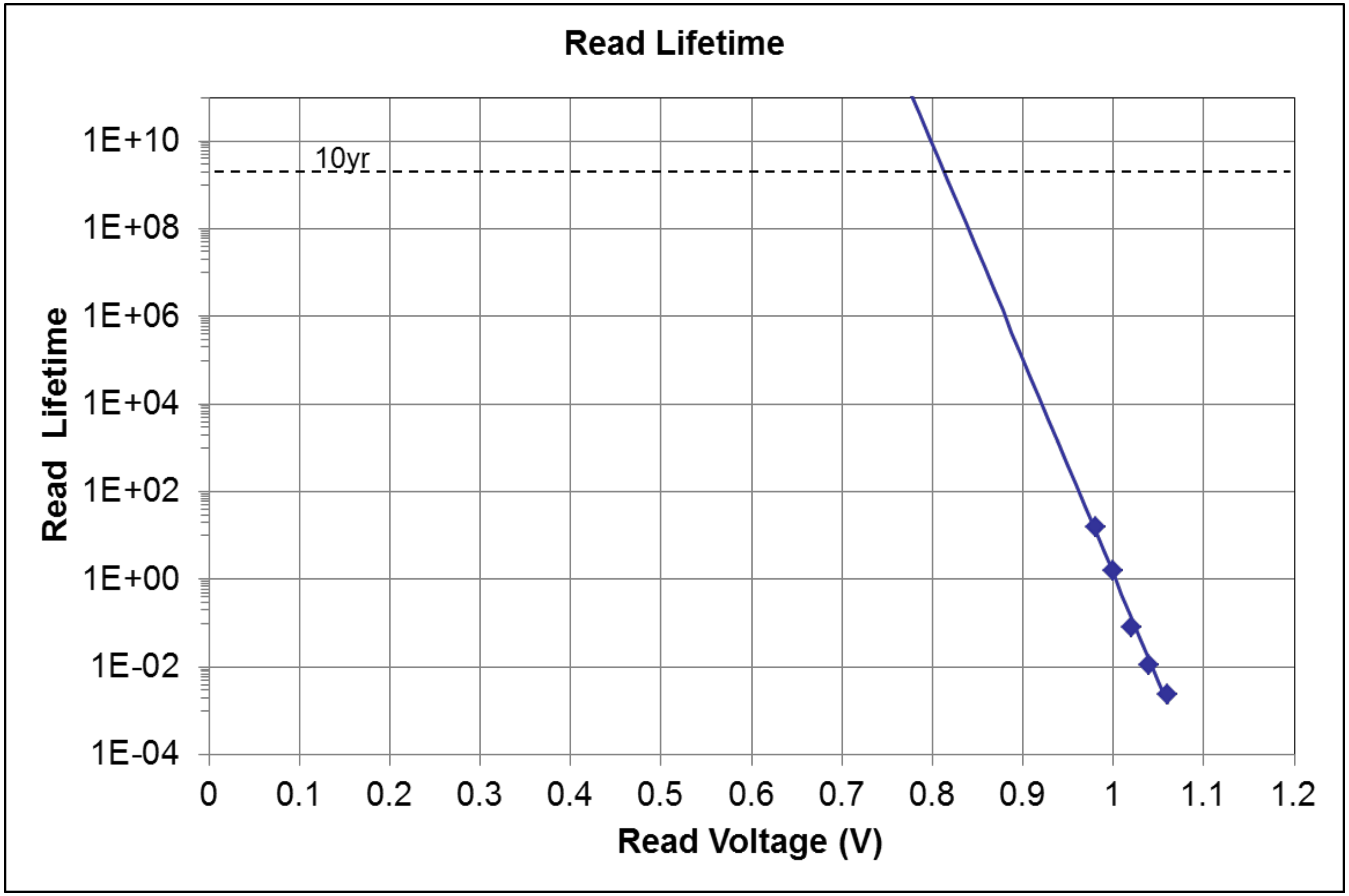
Programming energy capability of 30pJ at 1.2V
Further improvement possible with optimized materials

1Mb erase energy



Erase energy capability of 15pJ per operation at 1.2V

1Mb read stability



Read Lifetime capability of 10 years continuous read possible for less than 0.8V

Thank you!