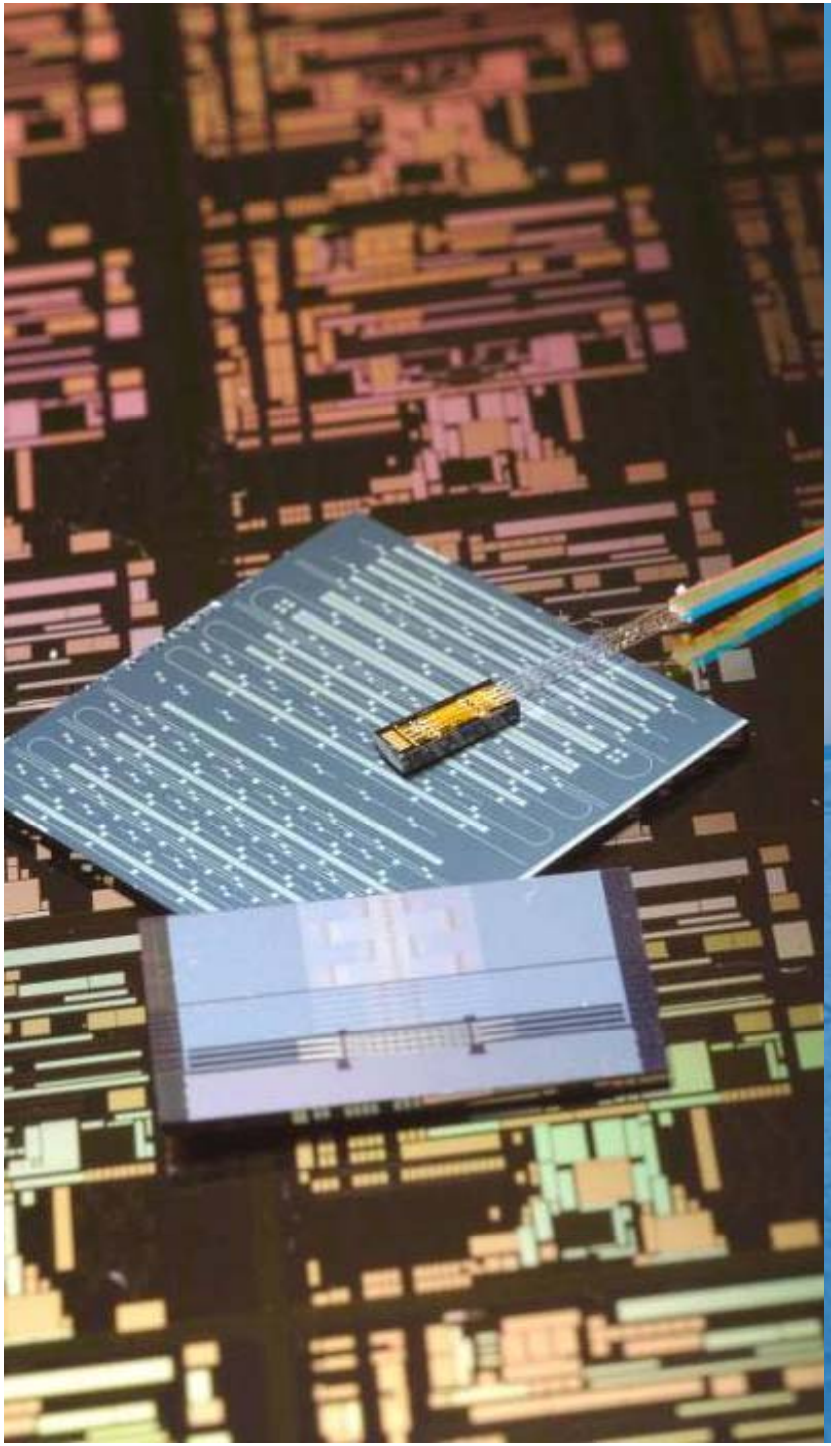


Silicon Photonics

Dr. Mario Paniccia
Intel Fellow
Director, Photonics Technology Lab
Intel Corporation

www.intel.com/go/sp

May 19 2009
IEEE conf

Agenda

Motivation

History & Progress

Intel's Research Program

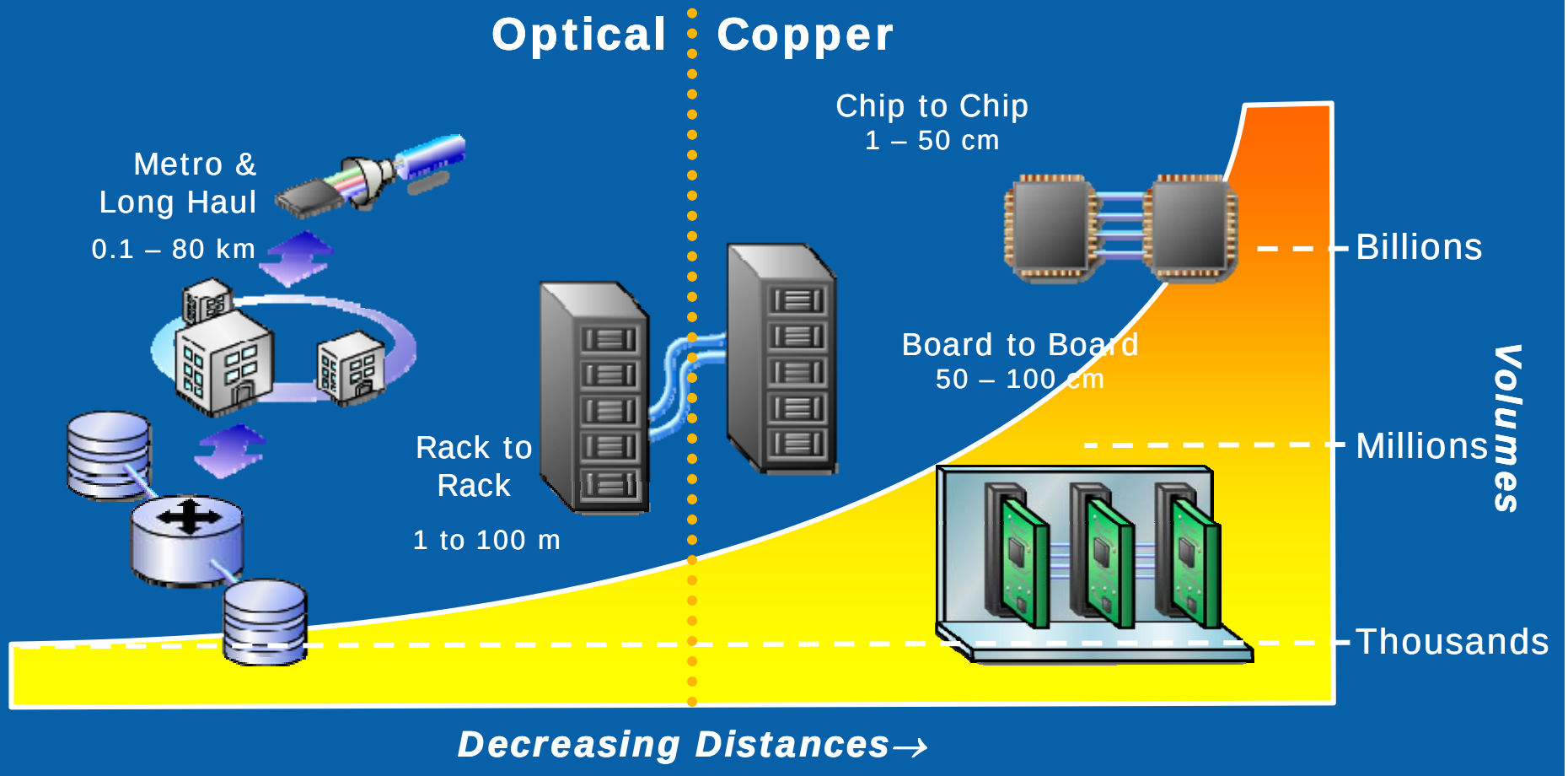
Building Block Results

– Modulator, detector, hybrid laser

Integrated 200Gb/s Test chip

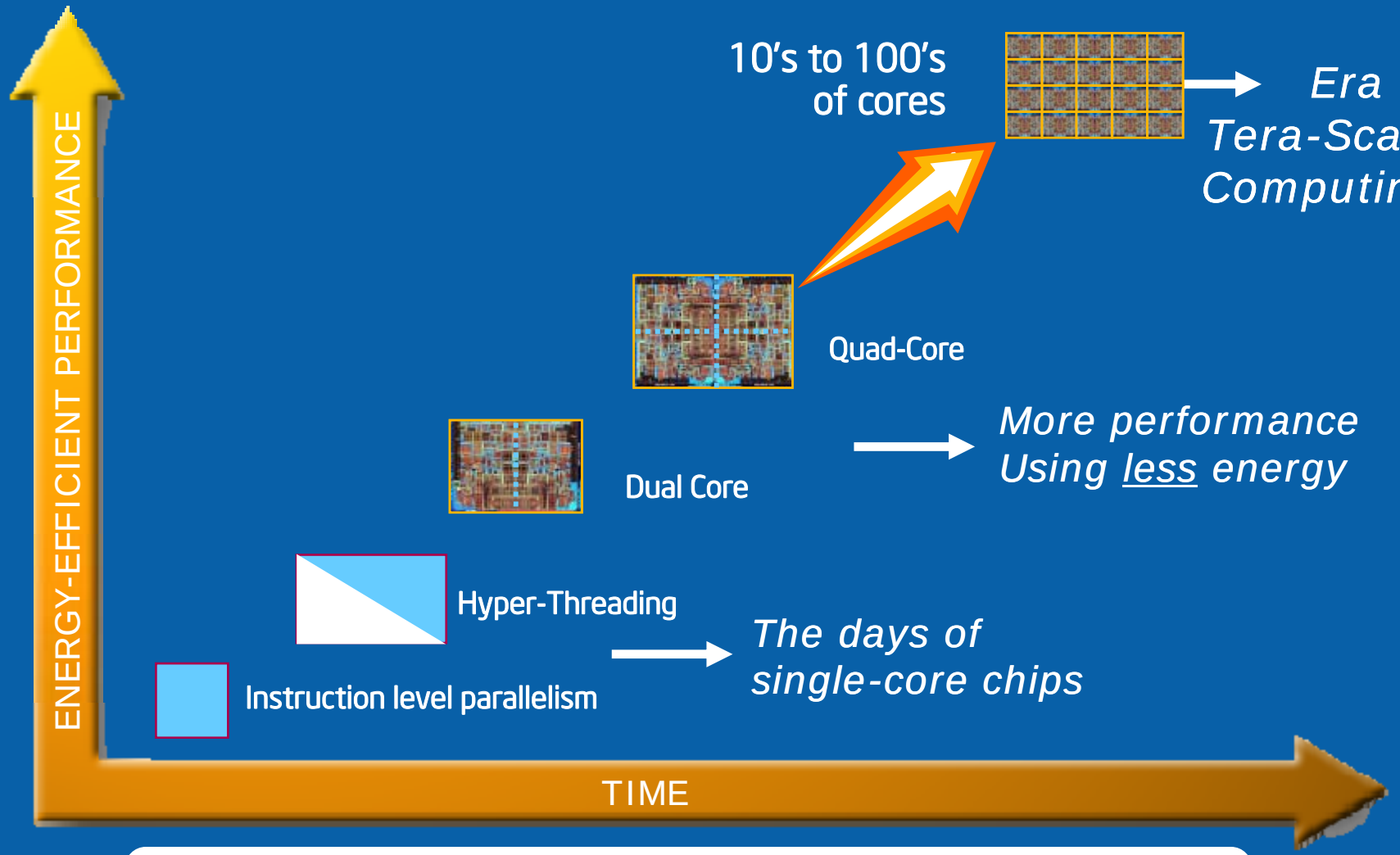
Future work and Summary

Moving to Interconnects



Drive optical to high volumes and low costs

Tera-leap to Parallelism:



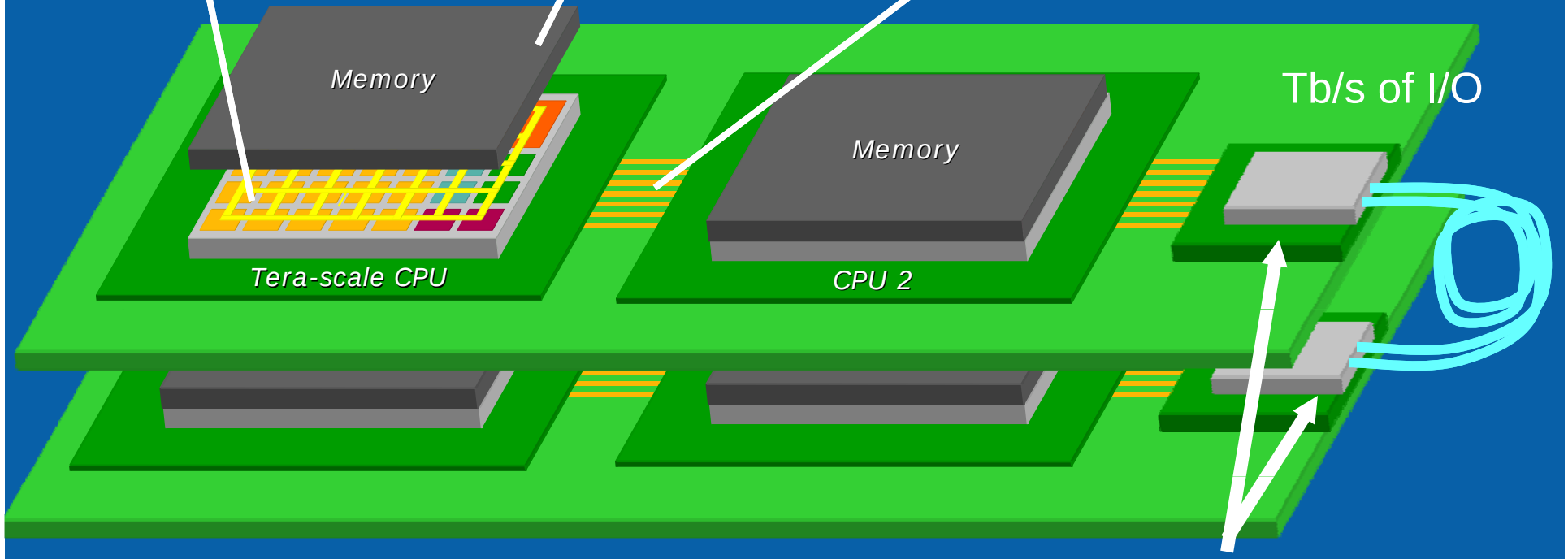
All this compute capability will drive need for high speed optical links

Future Physical I/O for Tera-scale Servers

Core-Core: On Die
Interconnect fabric

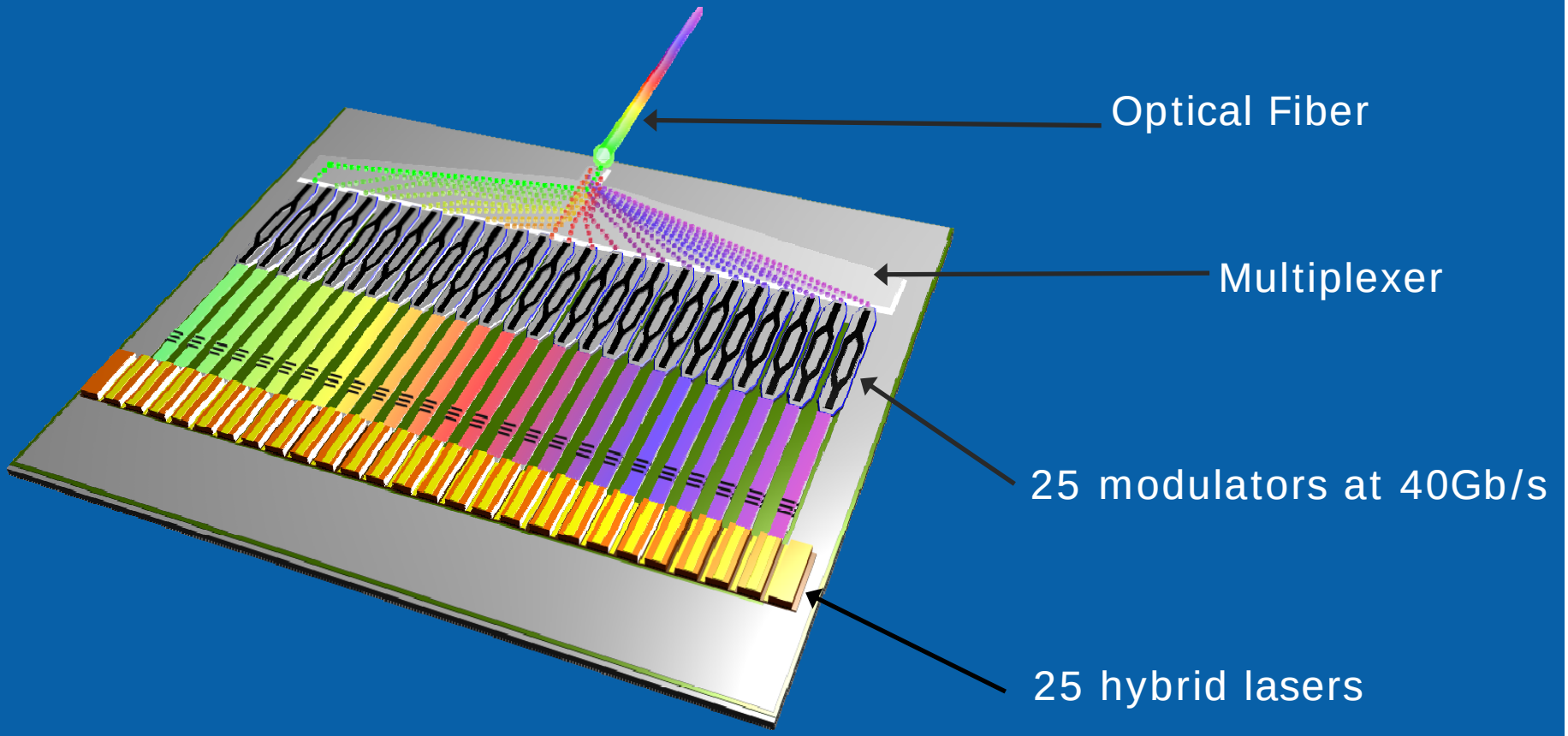
Memory: Package
3D Stacking

Chip-Chip: Fast Copper
FR4 or Flex cables



Integrated Tb/s Optical Chip?

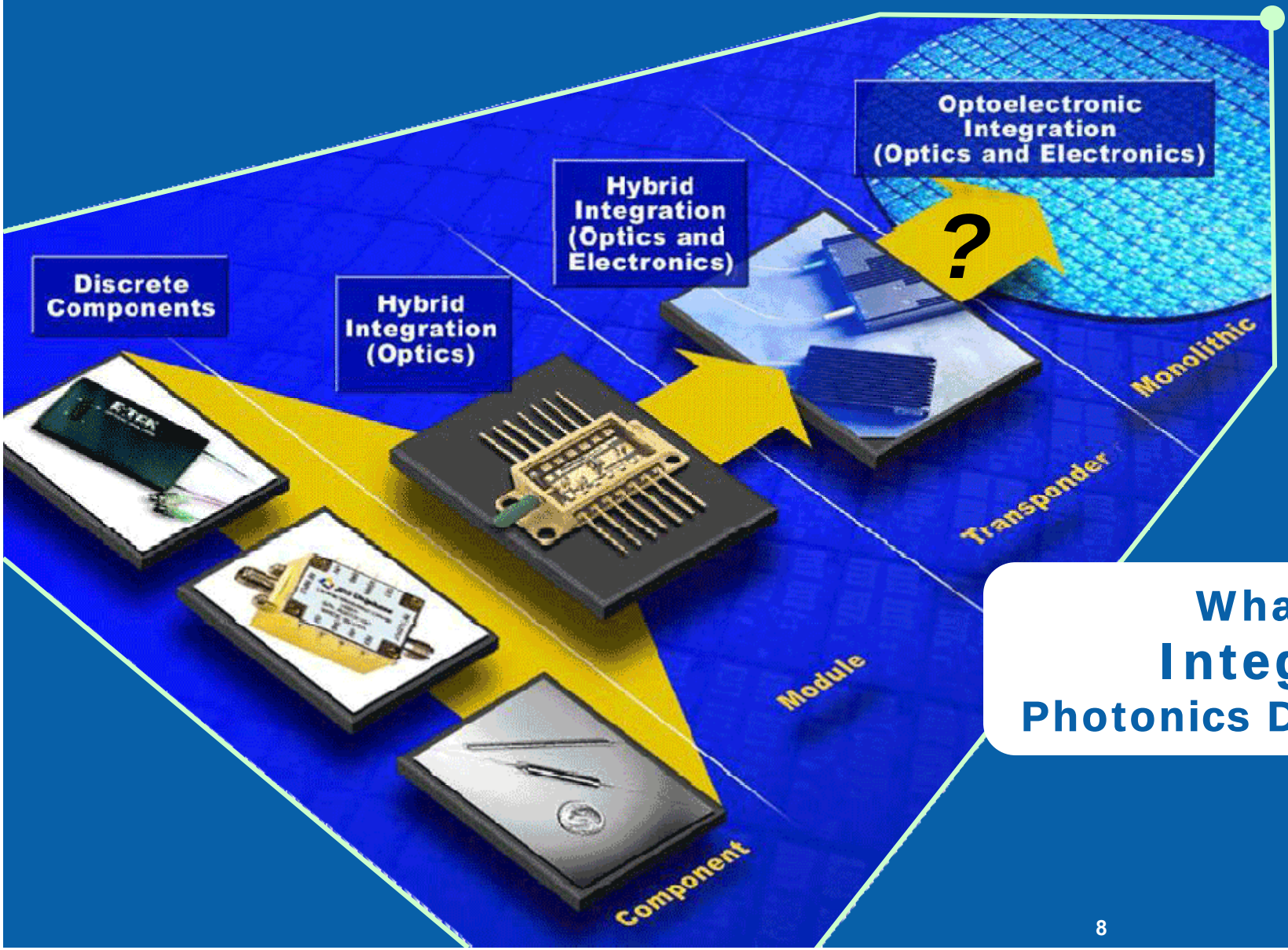
Future: A Terabit Optical Chip



A future integrated terabit per second optical link on a single chip

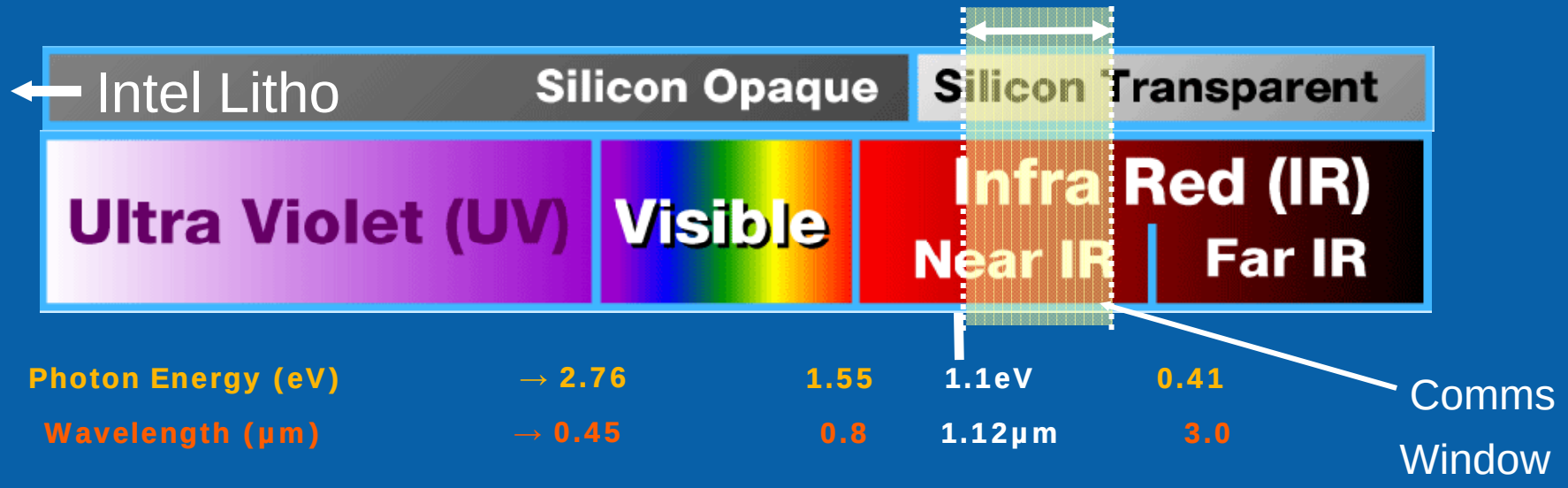
- Motivation
- History & Progress
- Intel's Research Program
- Building Block Results
  - –Modulator, detector, hybrid laser
- Integrated 200Gb/s Test chip
- Future work & Summary

Photonics Evolution



What could Integrated Photonics Deliver?

Silicon as an Optical Material



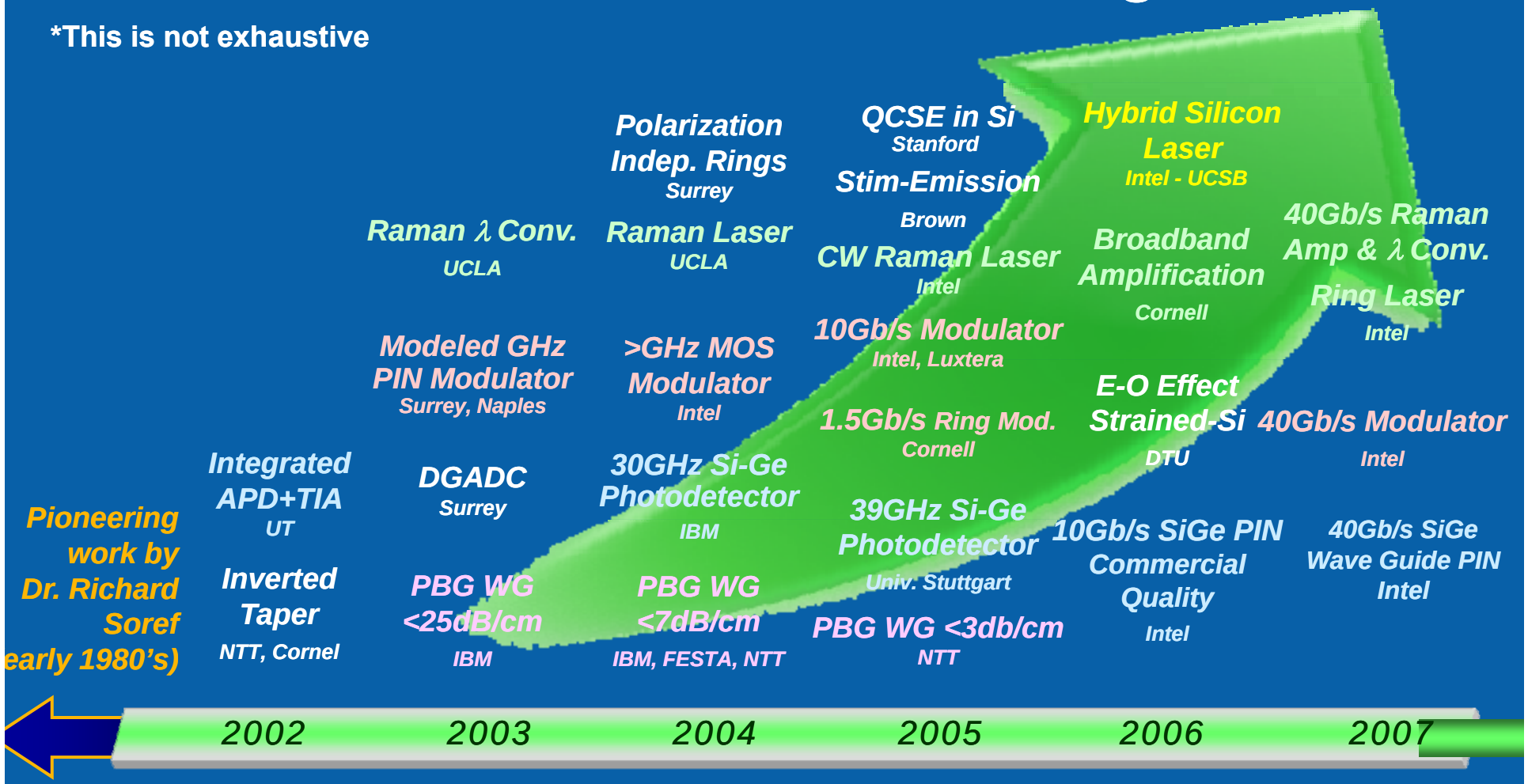
- ✓Transparent > ~1.1 µm
- ✓High index
- ✓CMOS Compatible
- ✓Low cost material

- ☹ Low light emission efficiency
- ☹ No electro-optical effect
- ☹ No detection in 1.3-1.6 µm

Silicon traditionally NOT optical material of choice

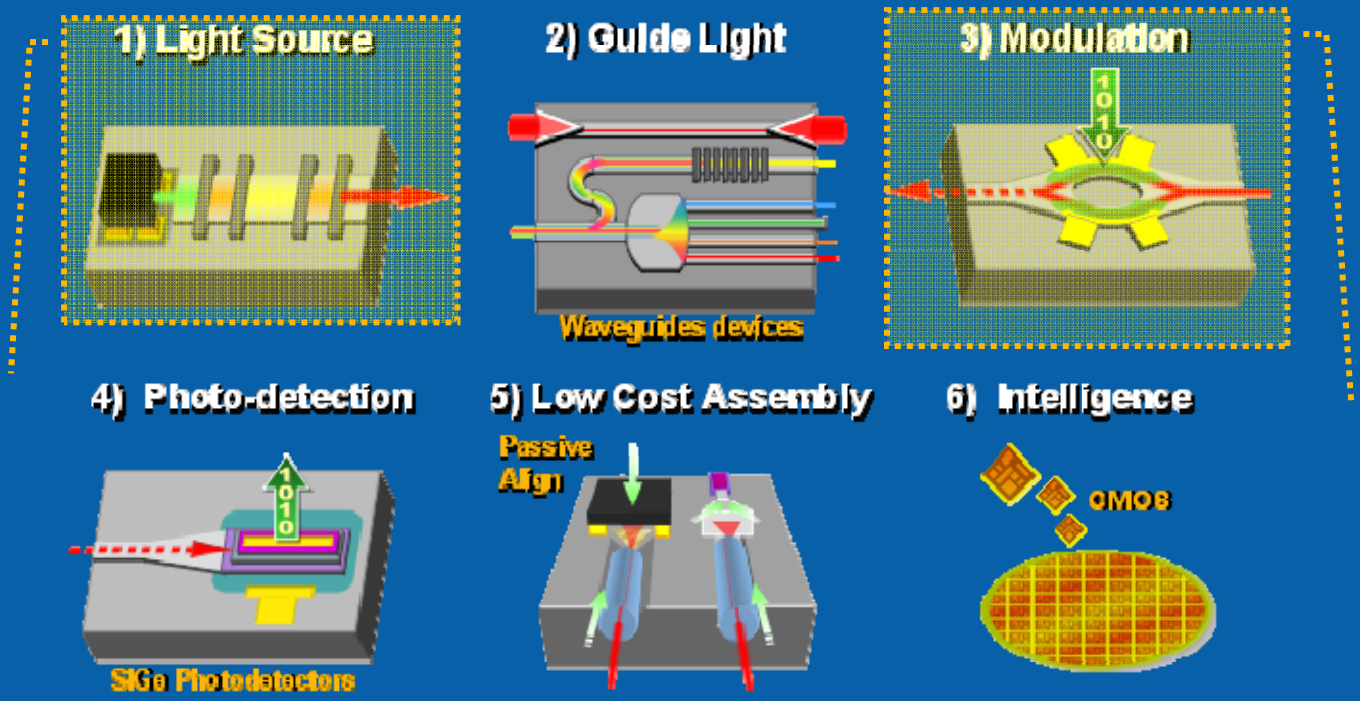
Si Photonics Recent Progress

*This is not exhaustive



Device performance making significant advances

Intel's Silicon Photonics Research



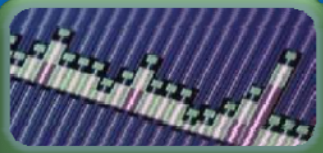
First: Innovate to prove silicon is a viable optical material

Intel's Silicon Photonics Research

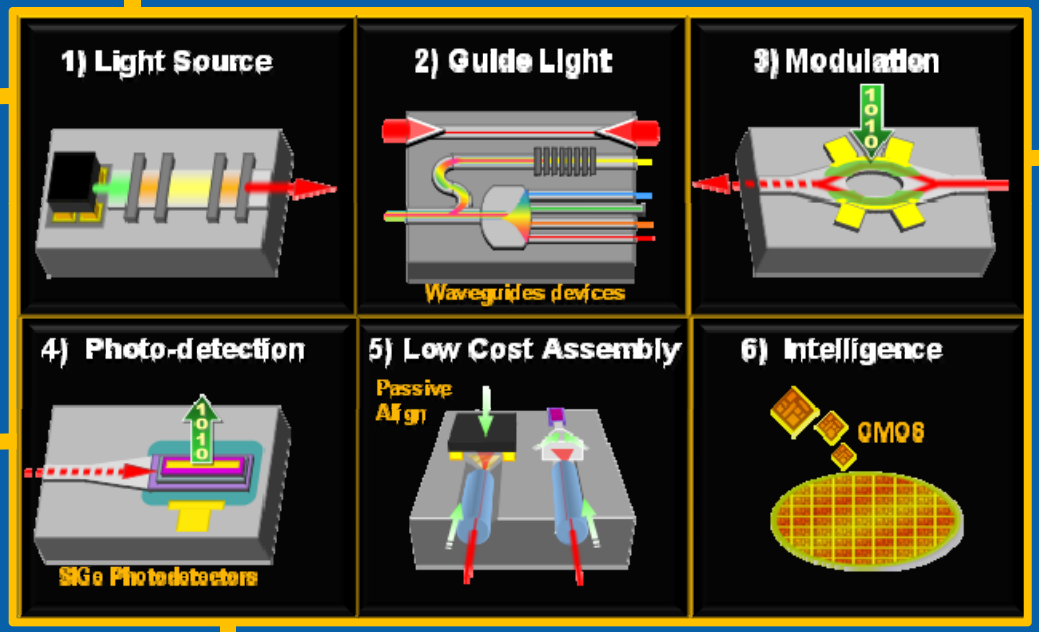
Innovating with low-cost silicon to create new optical devices

1st Continuous Wave Silicon Raman Laser *(Feb '05)*

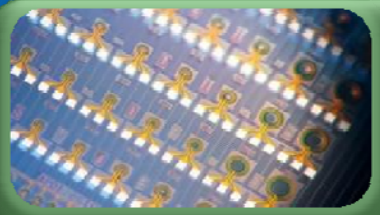
Hybrid Silicon Laser *(Sept. '06)*



40 Gb/s PIN Photodetectors *(Aug. '07)*



Silicon Modulators
1GHz *(Feb '04)*
10 Gb/s *(Apr '05)*
40 Gb/s *(July '07)*
8-channel integrated 200Gb/s *(May '08)*



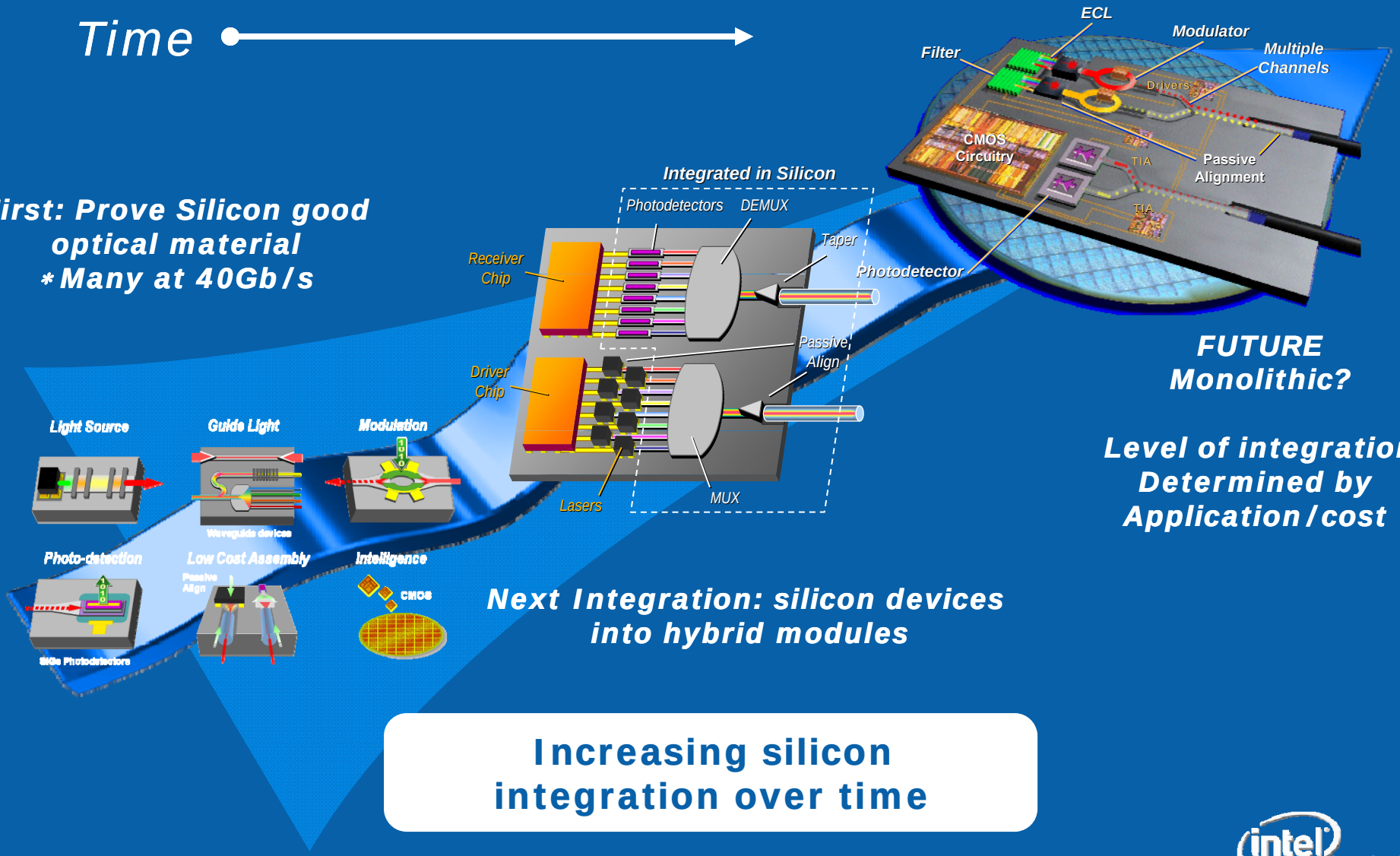
Avalanche Photodetectors with 340 GHz Gain*BW *(Dec 08)*

intel Leap ahead™

Integration Vision

Time

First: Prove Silicon good optical material
*** Many at 40Gb/s**

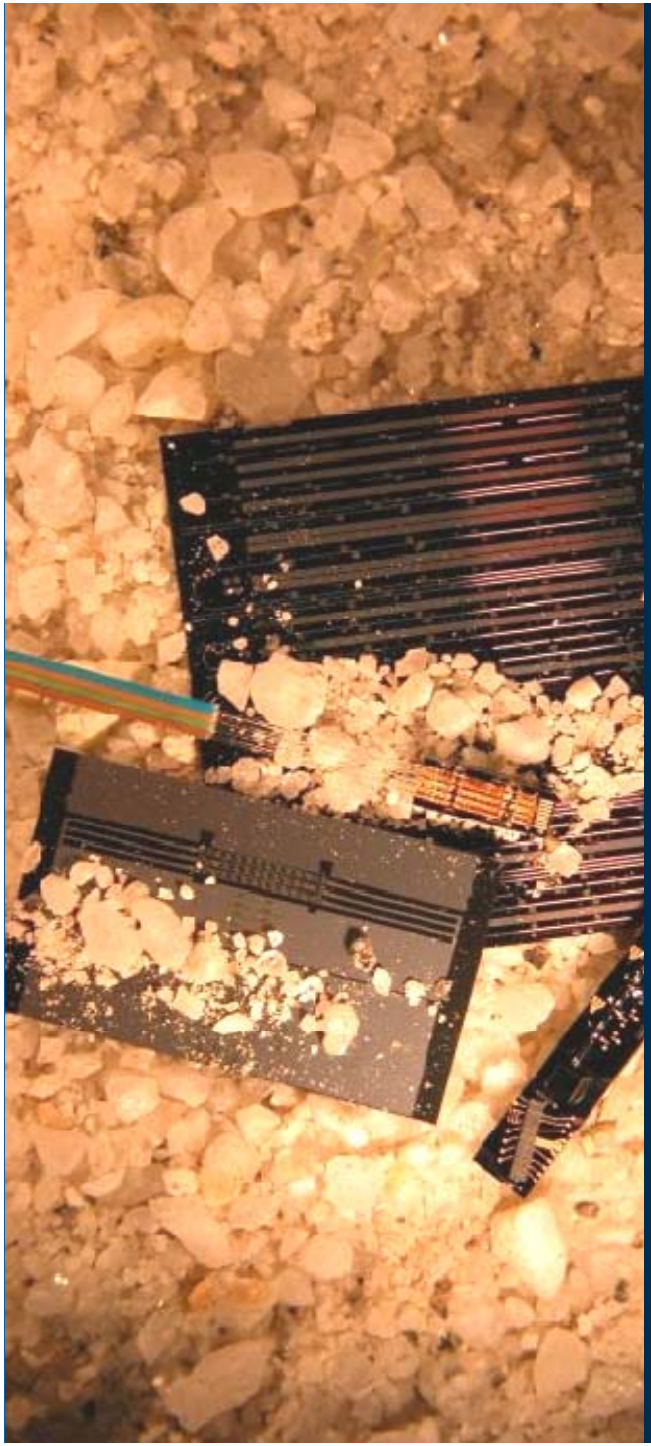


FUTURE Monolithic?

Level of integration Determined by Application/cost

Next Integration: silicon devices into hybrid modules

Increasing silicon integration over time



Motivation

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– Integrated 200Gb/s Test chip

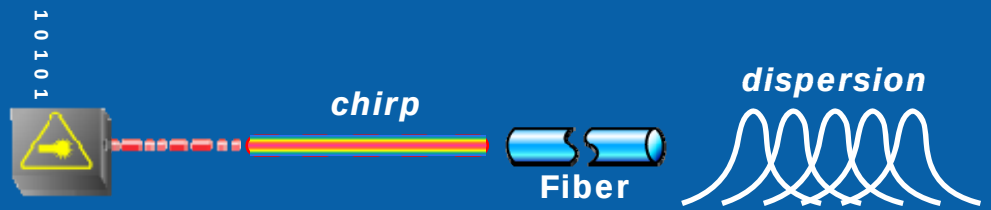
Future work & Summary

Modulation

Direct or External modulation

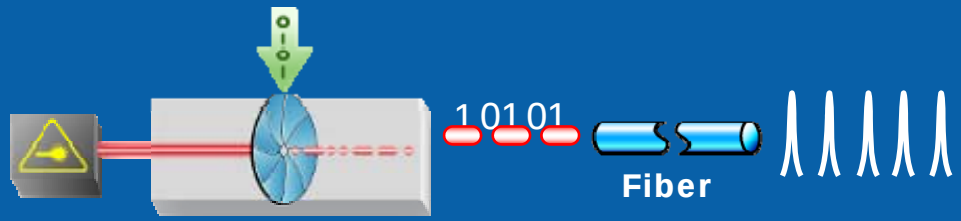
External used for 10G at ~12km+

Direct Modulation



Data rate limited

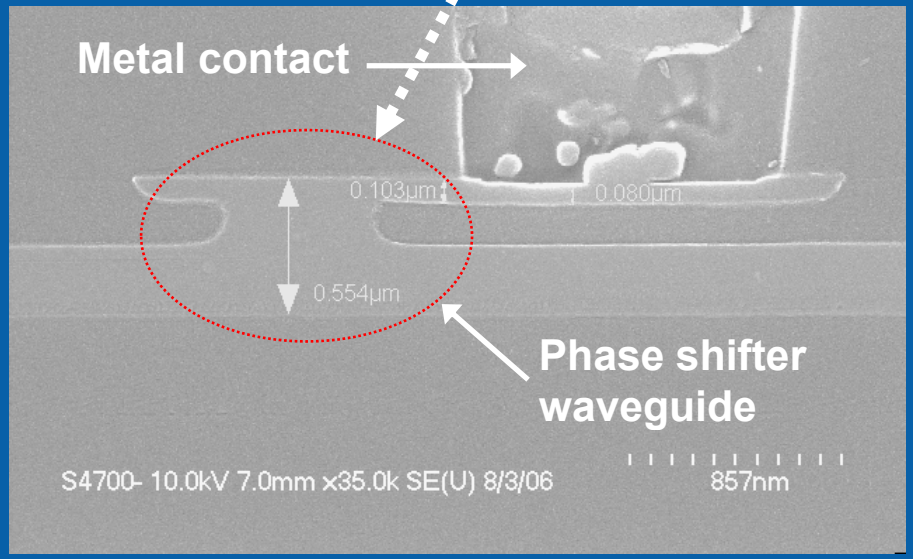
External Modulation



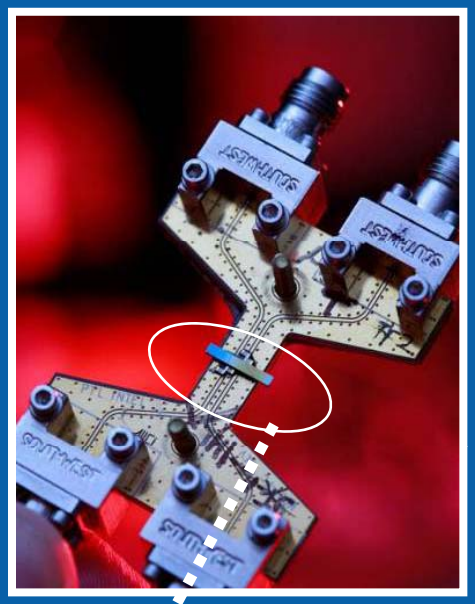
Very $$$

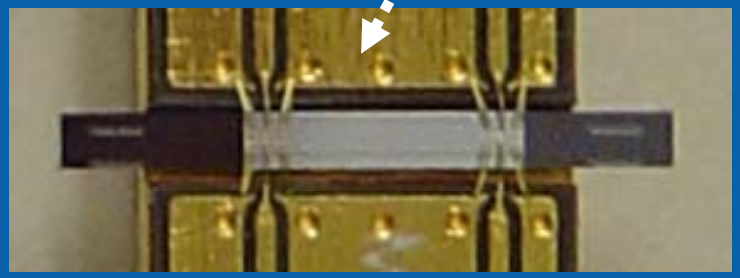
No electro-optic effect
use free carriers

Intel's Second Generation: Silicon Modulator



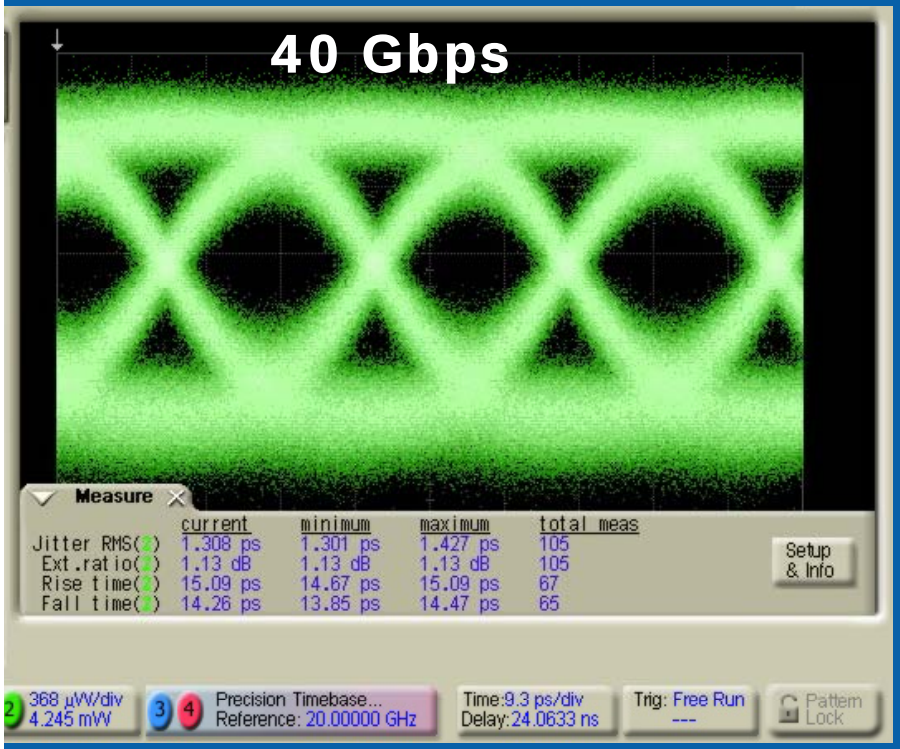
SEM picture of p-n phase shifter

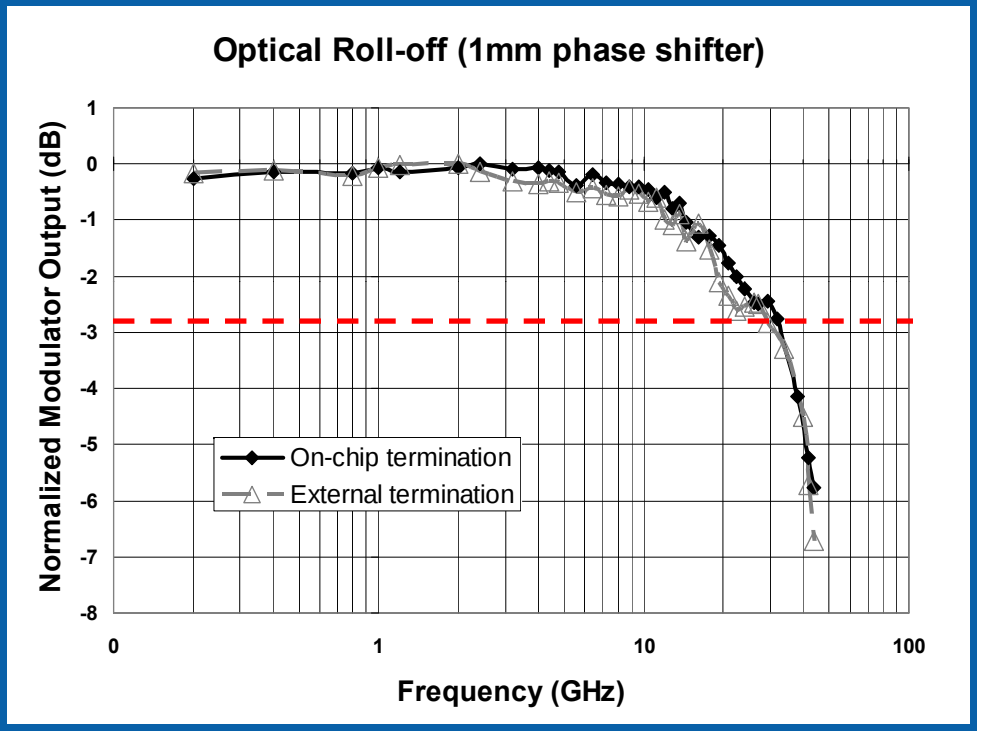




-Based on traveling wave design
-Optimized optical & electrical RF

40 Gbps Data Transmission

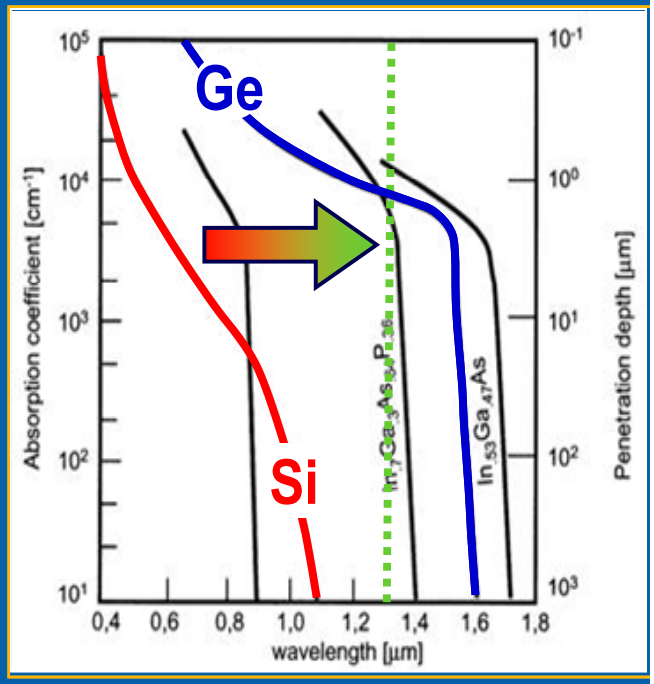


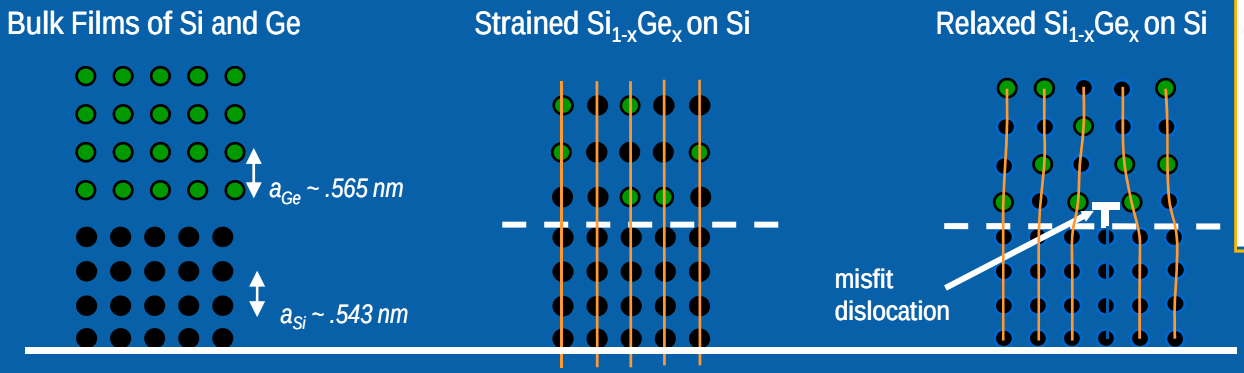


- Optical 3 dB roll off ~30 GHz (parasitic effect included)
- 6 dB electrical roll-off ~ 40 GHz (no parasitic effect included)
- Measured phase efficiency = 3.3 V-cm

Photodetection

- Silicon does not absorb IR well
- Using SiGe to extend to 1.3µm+
- Must overcome lattice mismatch

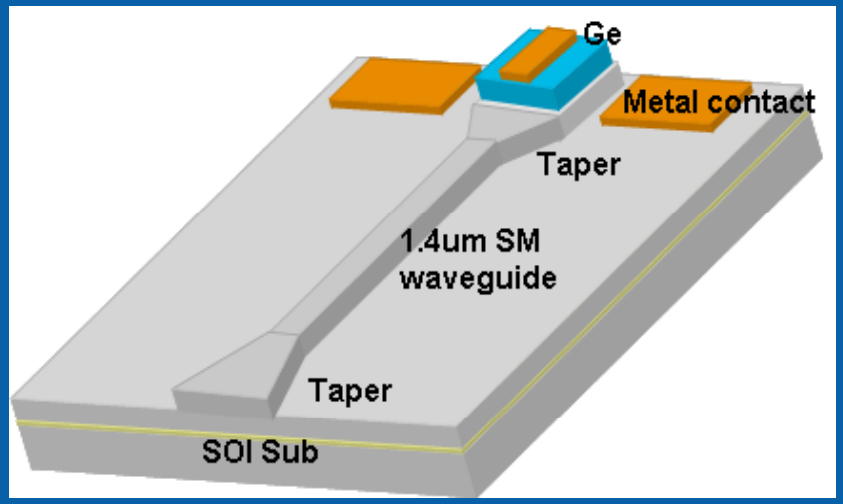


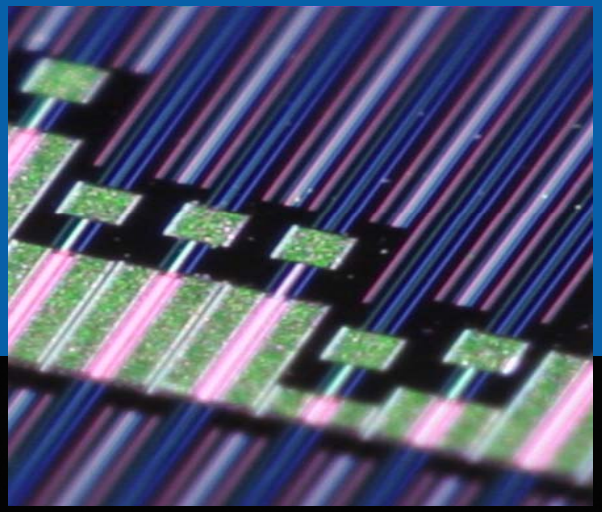


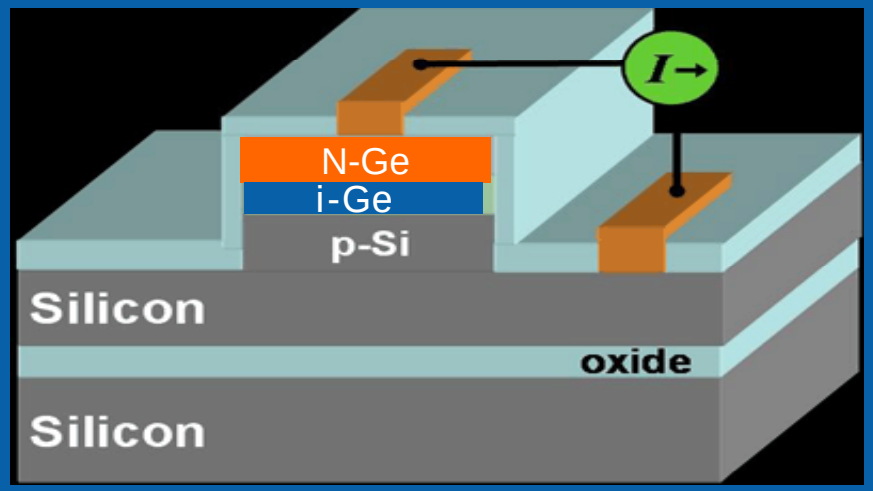
Misfit dislocations typically create threading dislocations which degrade device performance - *dark current (I_{dk}) goes up*.

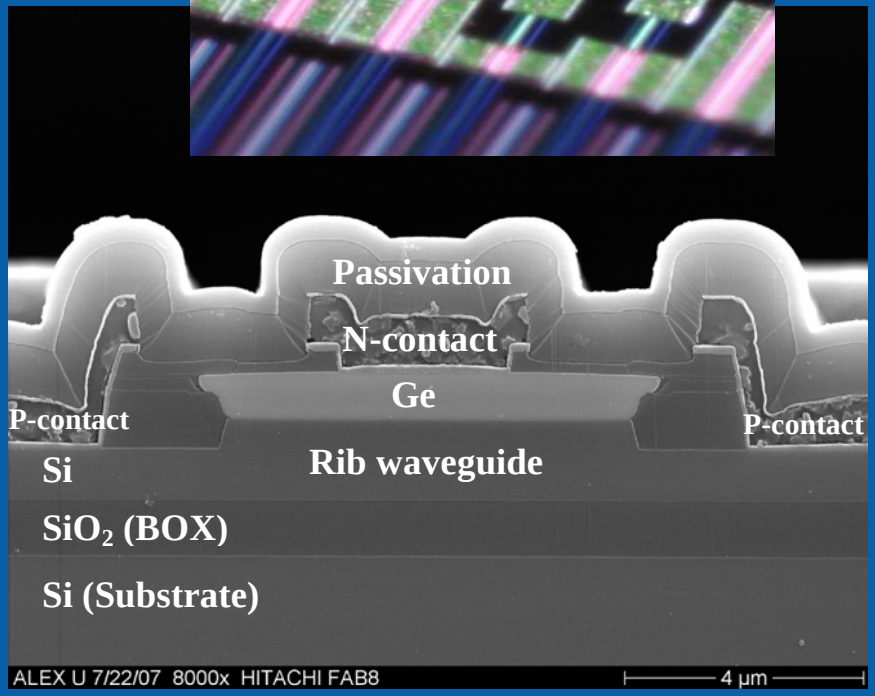
Must simultaneously achieve required speed, responsivity, & dark current.

Waveguide Photodetector Design



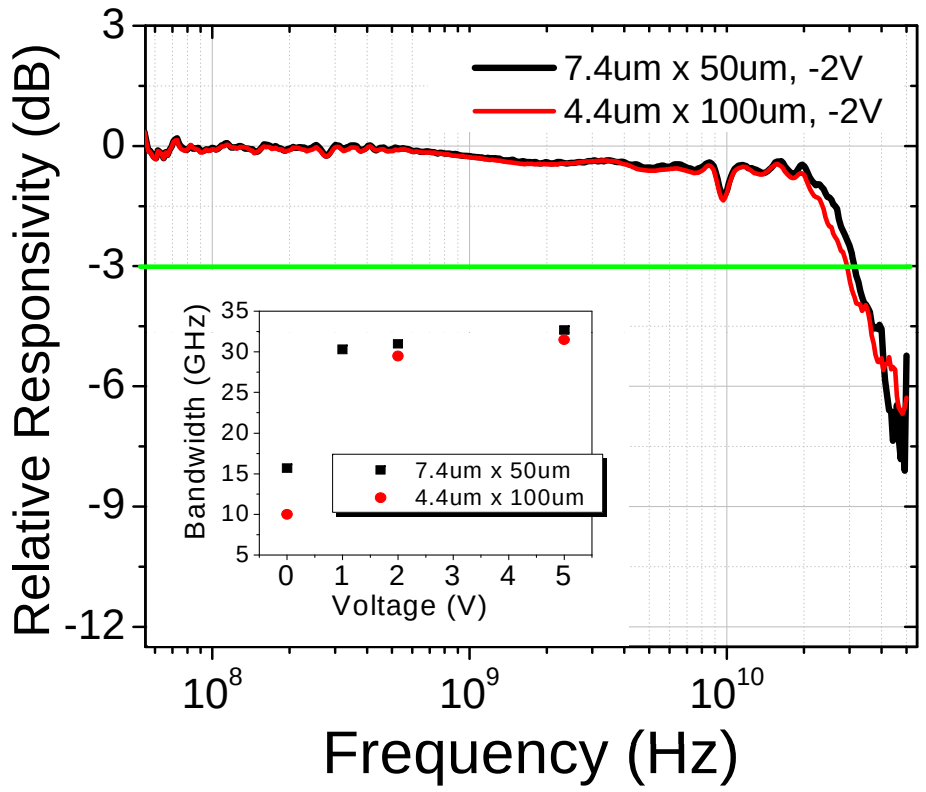




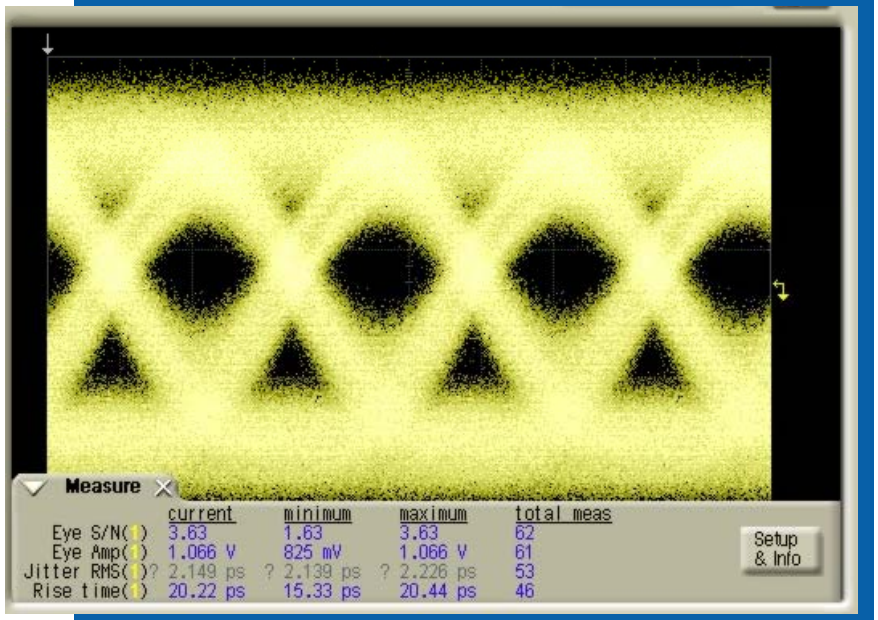


SEM Cross-Section

SiGe WG PIN - High Speed Performance



31 GHz Optical Bandwidth

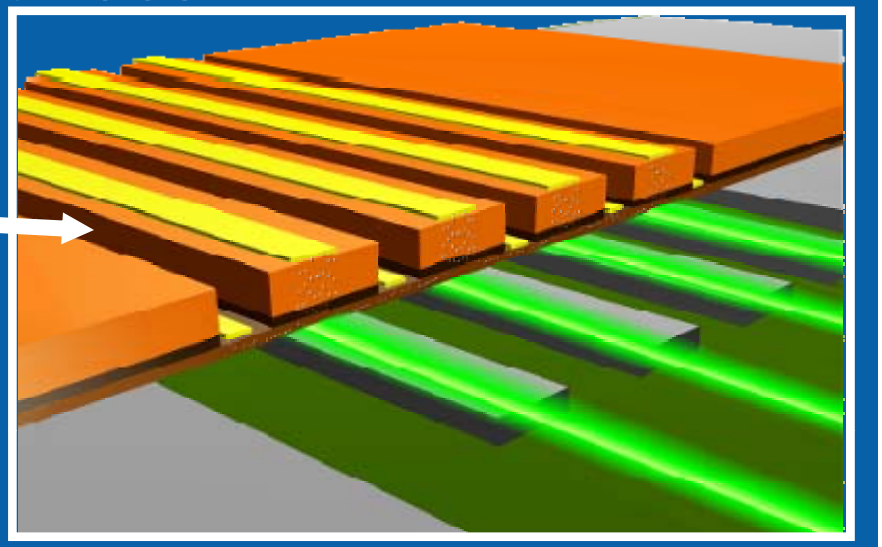


40 Gb/s Eye Diagram

95% Quantum Efficiency
Operating at λ ~1.56um
< 200nA of dark current

Hybrid Silicon Laser
Collaboration with UCSB

The Indium Phosphide emits the light into the silicon waveguide

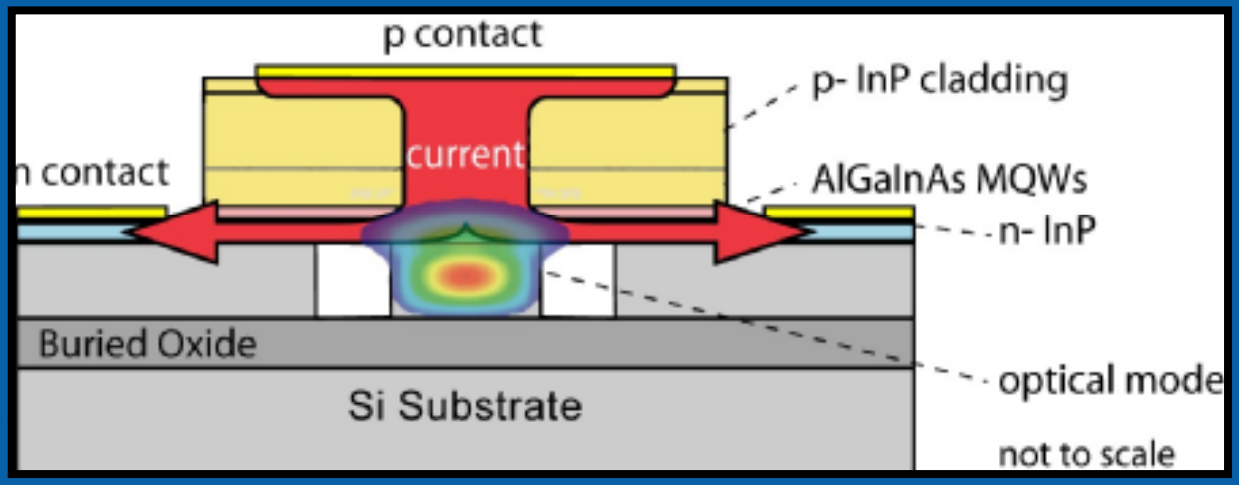


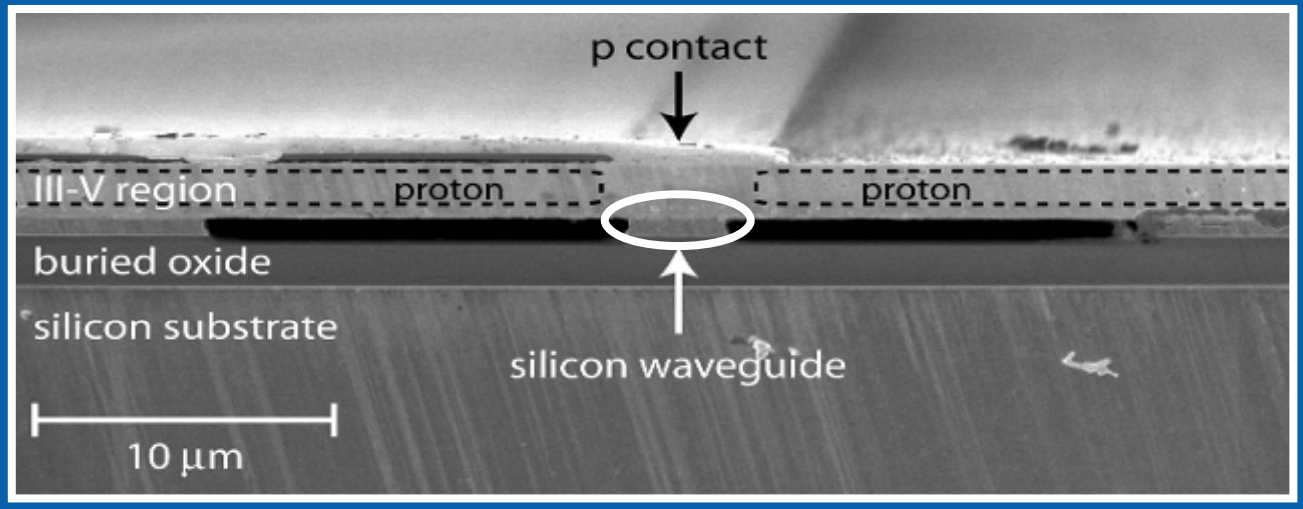
The silicon acts as laser cavity:

- Silicon waveguide routes the light
- Laser performance determined by Silicon waveguide
  - i.e WDM performance determined by etch silicon gratings

No alignment needed
10's if not 100's of lasers with ONE bond
Combines best of both materials

Hybrid Laser Structure

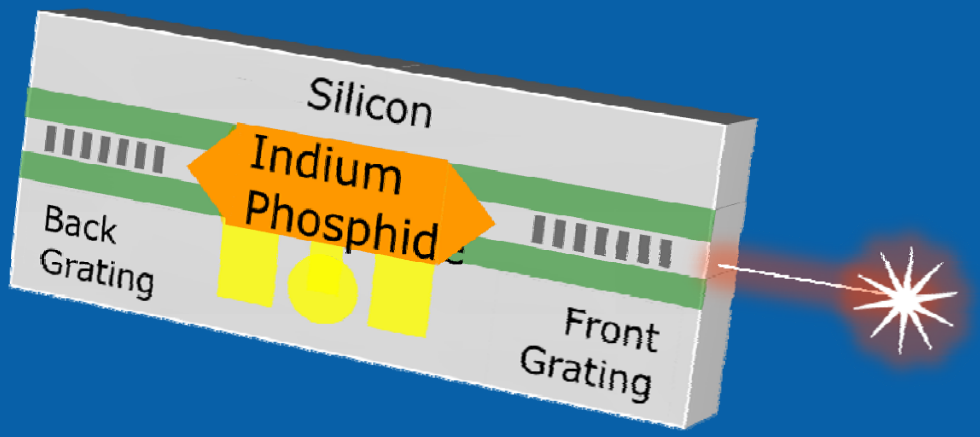


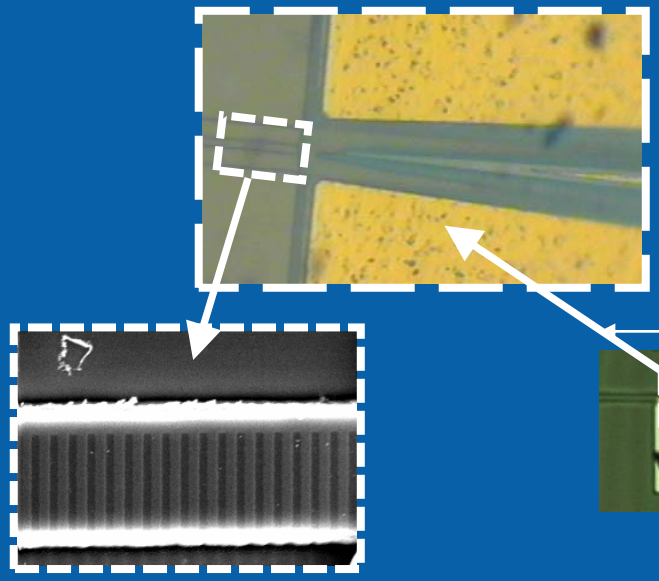


SEM (Scanning Electron Microscope) Photograph

Single Wavelength Hybrid Laser

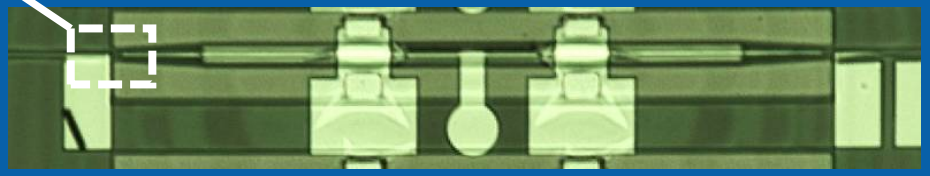
Intel & UCSB integrate grating mirrors in silicon, enabling wavelength-specific laser light output





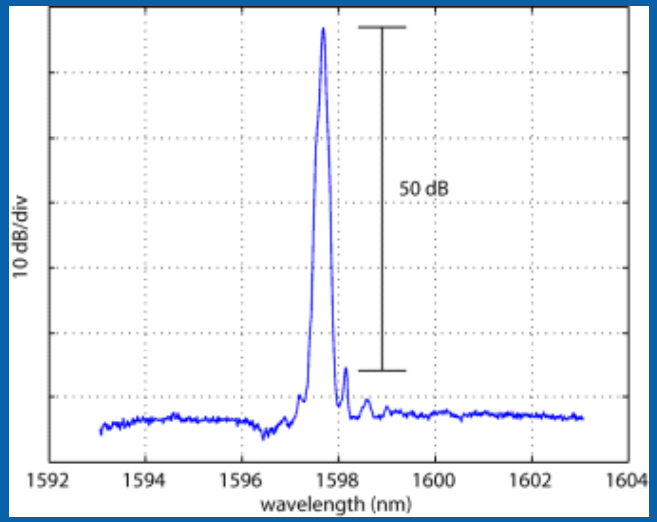
The Device

~1000um

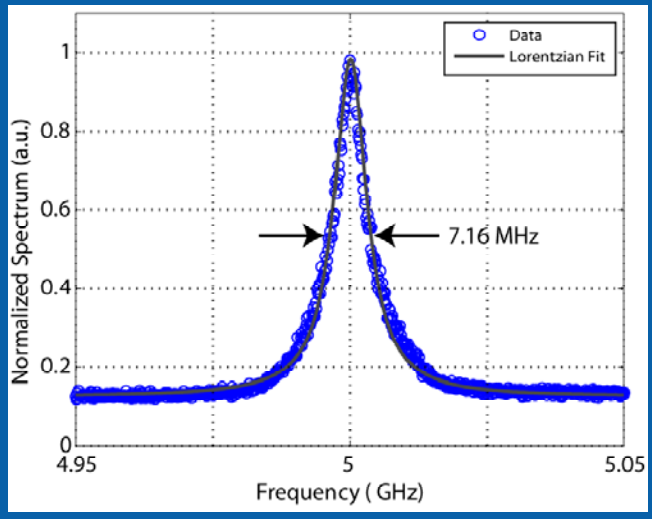


~150 um

Single Wavelength Results

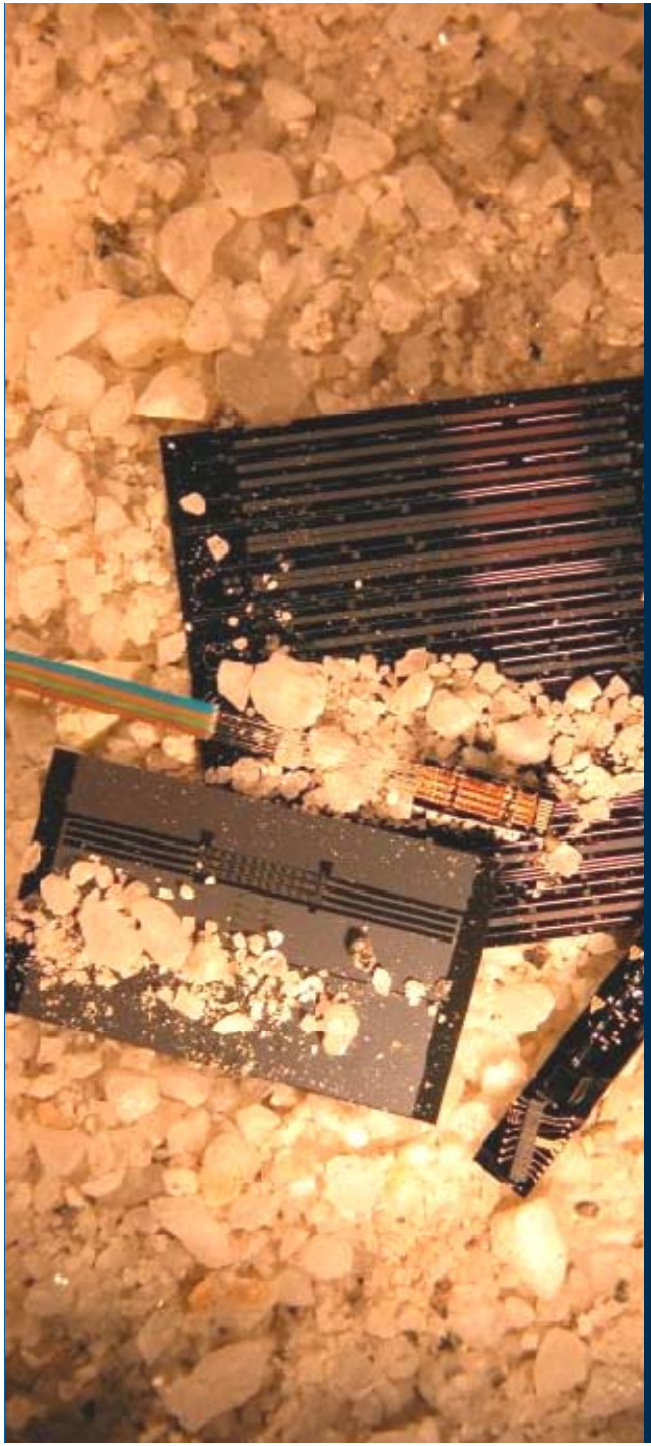


Optical Spectrum



Linewidth Measurement

- 8 mW output power at room temperature
- Single wavelength with 50 dB side mode suppression ratio
- 3.6 MHz line width (de-convolved from measurement)



- Motivation
- History & Progress
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  - –Modulator, detector, hybrid laser
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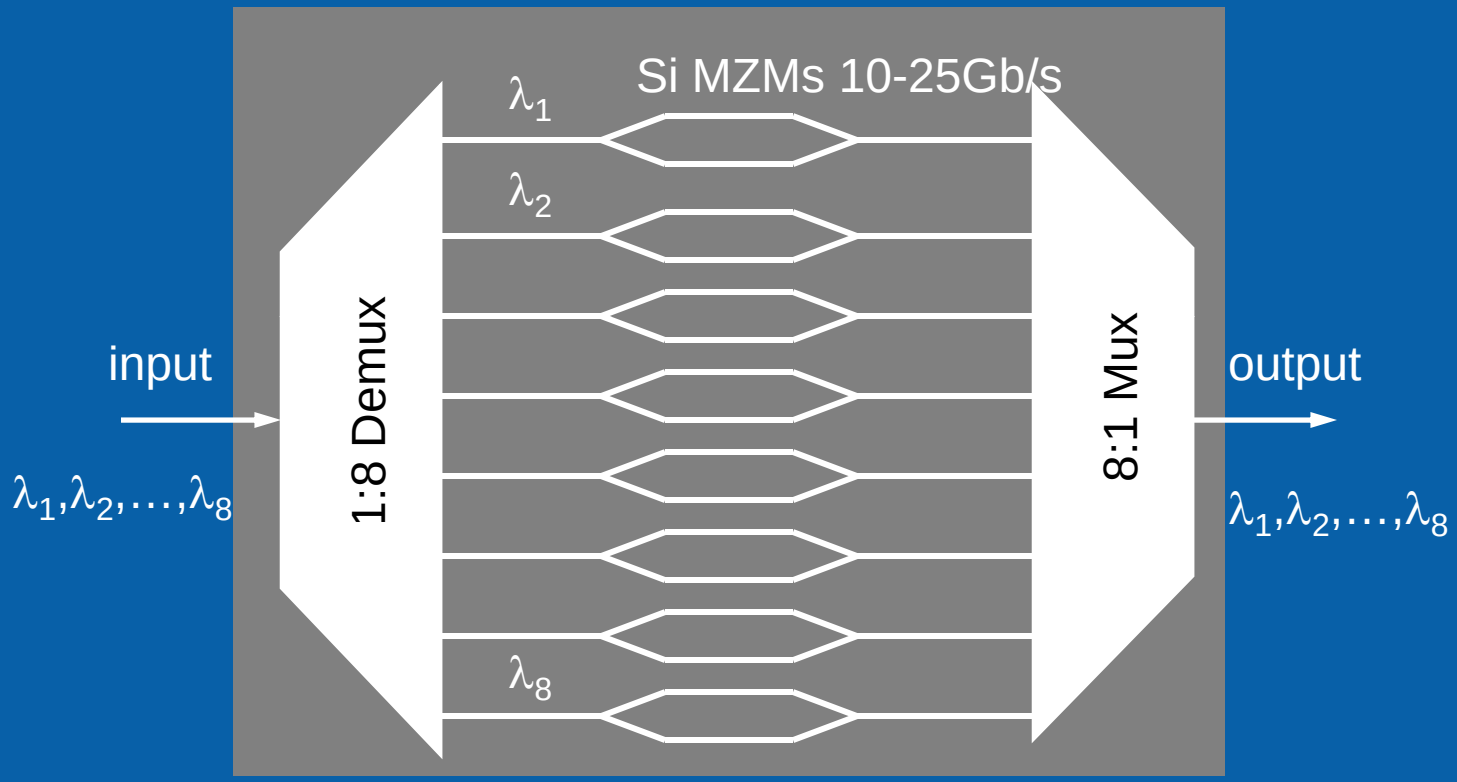
- Future work & Summary

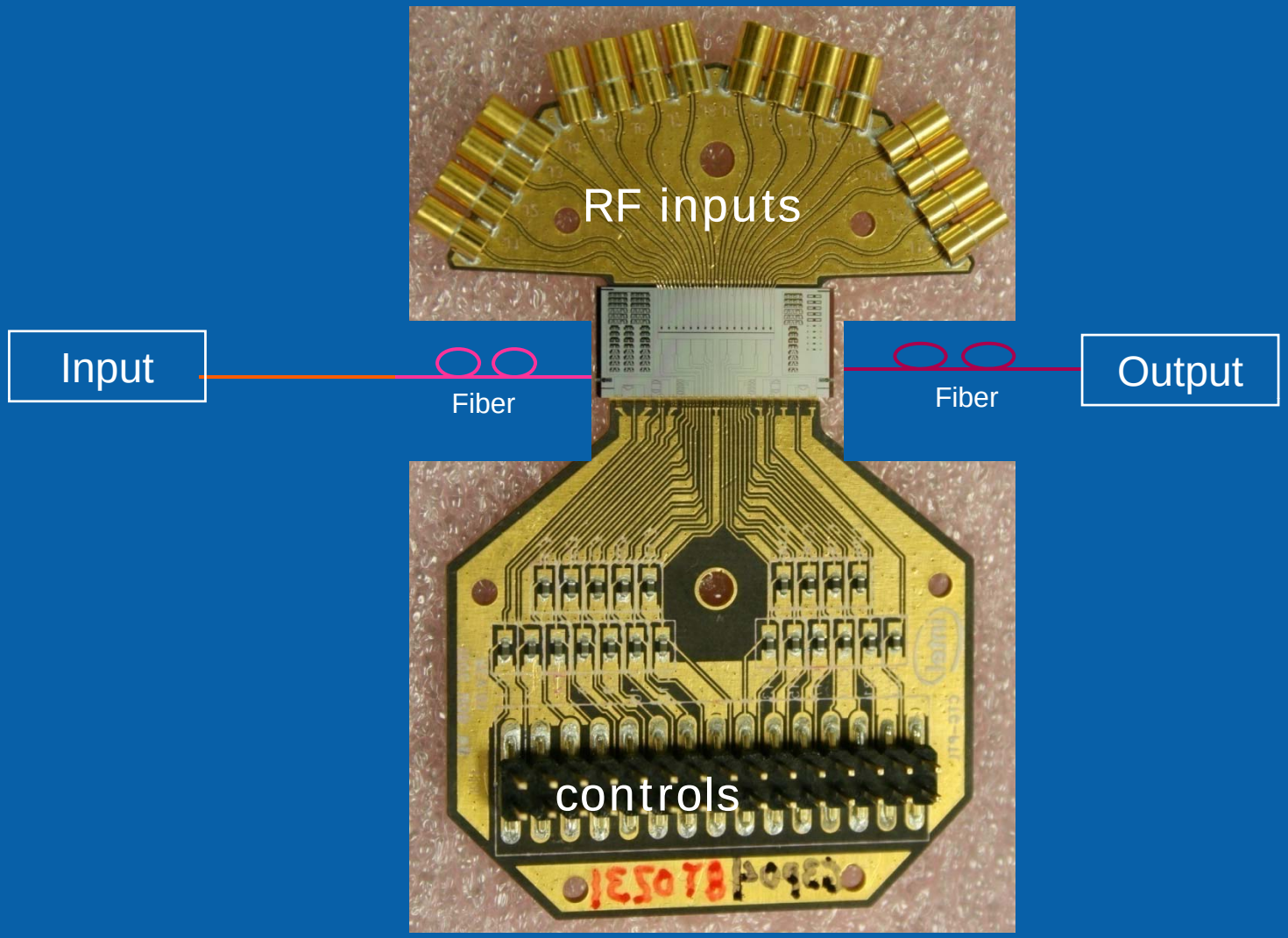
Integrated SiP Test chip

Learning Vehicle: target >100Gb/s



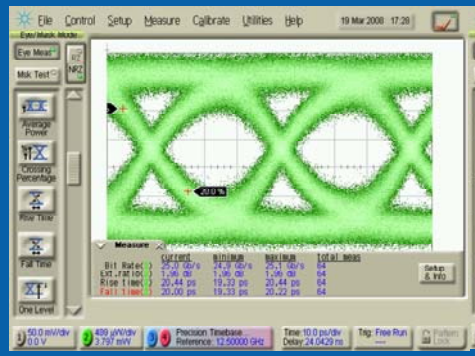
- **Learning vehicle for:**
  - **Process integration**
  - **Electrical and high speed packaging**
  - **Performance, die variation, uniformity**

Integrated Test chip



Integrated TX: Results

1534.6



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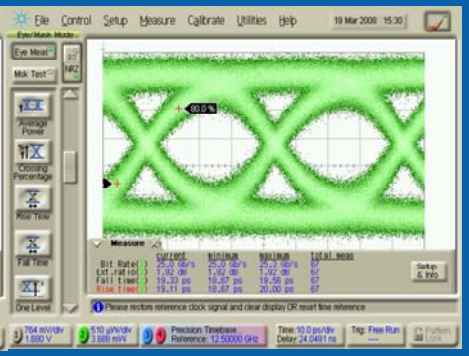

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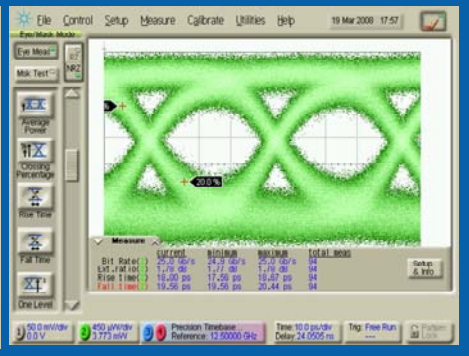

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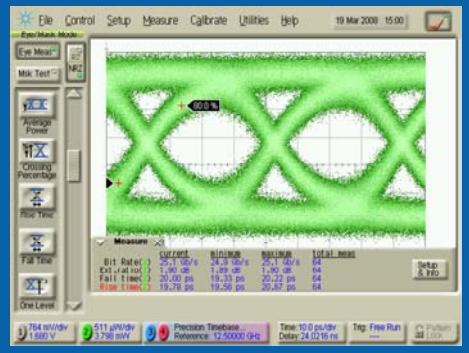

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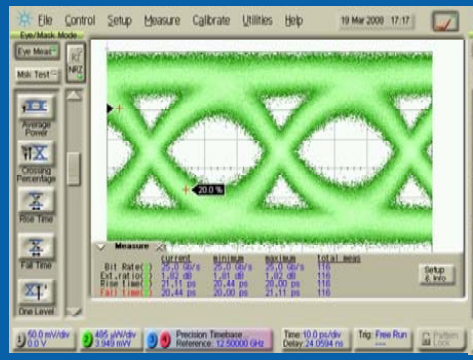

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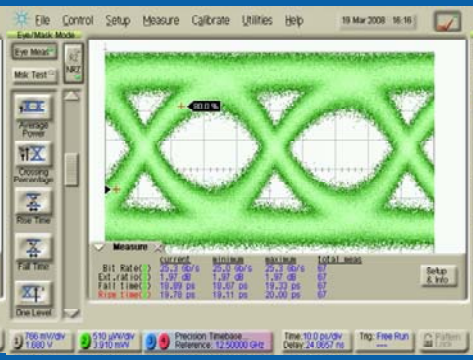

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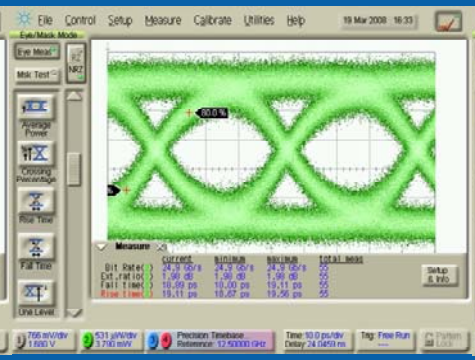

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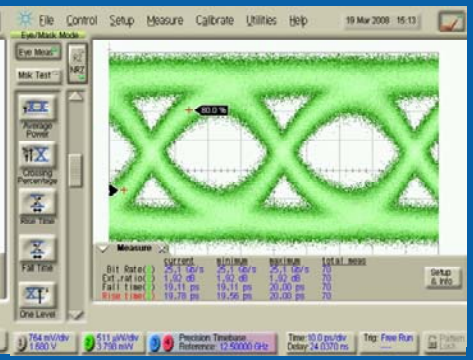

- All 8 channels yielded open 25 Gbps optical eyes close to expectation.
- Aggregate data rate of 200 Gbps
- Good step toward Tb/s …

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  - –Modulator, detector, hybrid laser
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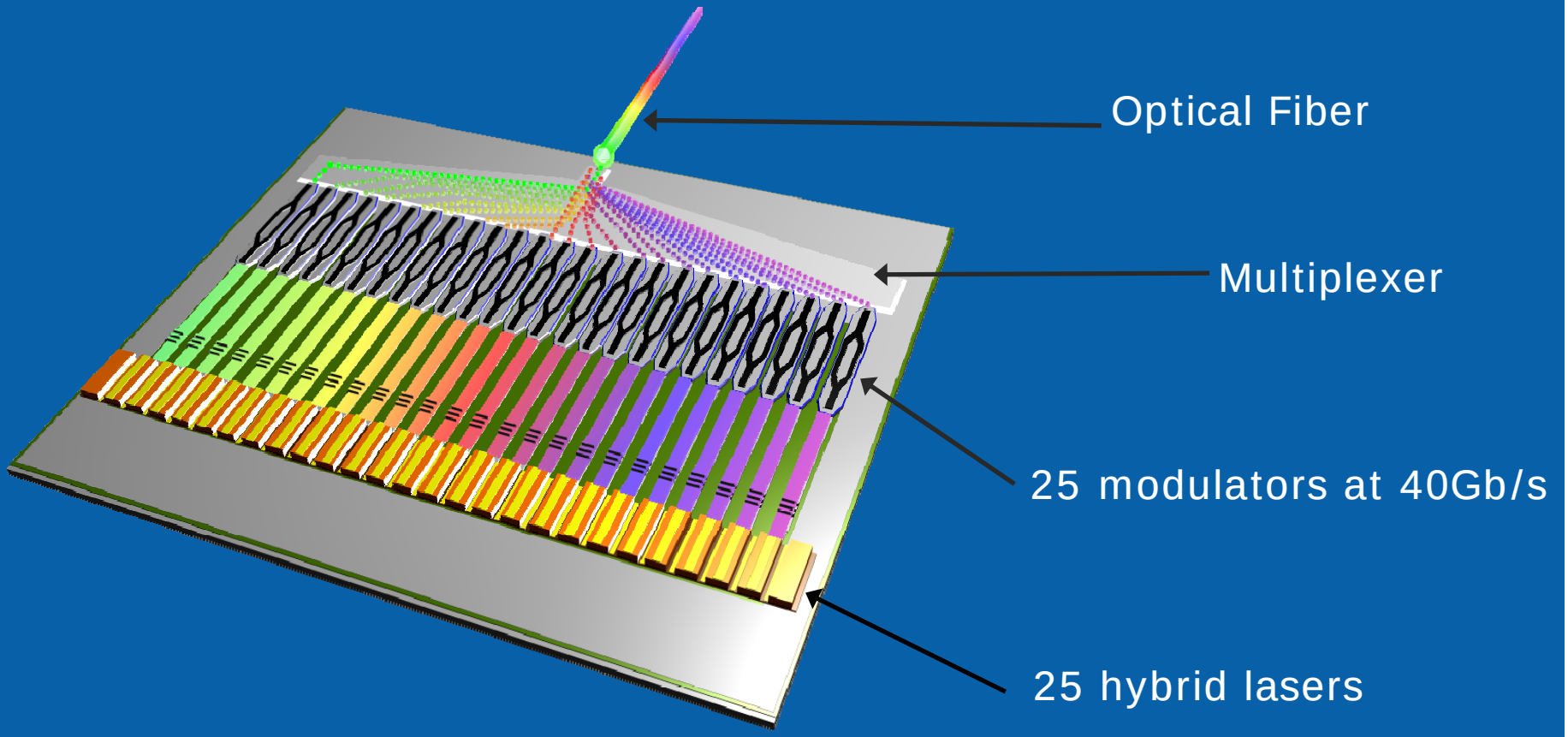
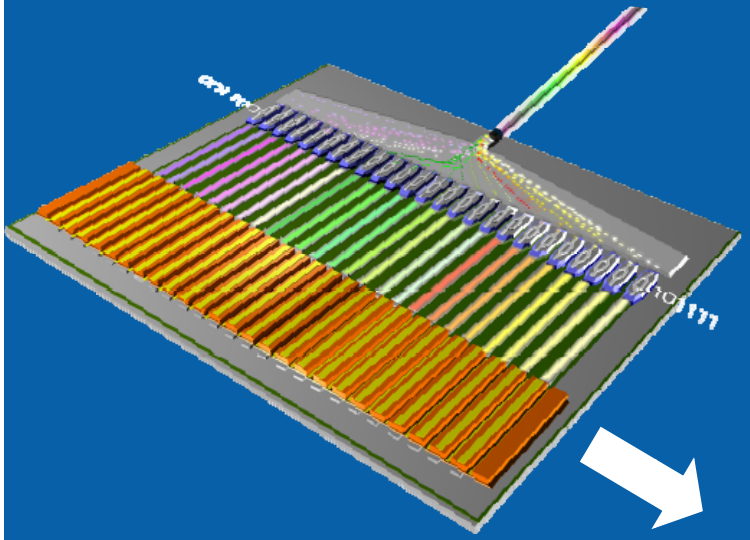
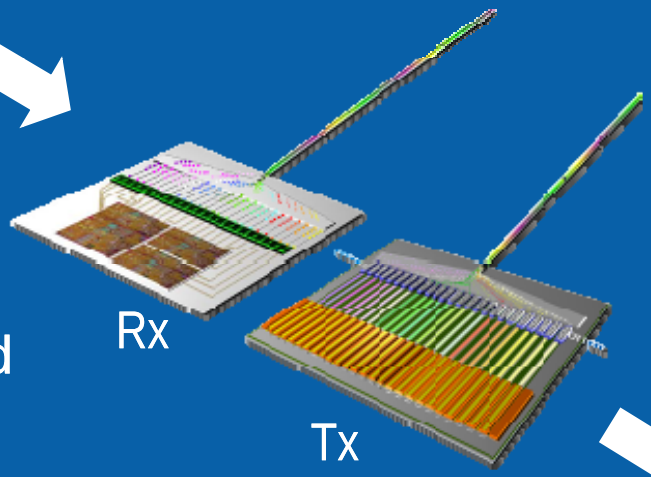
Future: A Terabit Optical Chip

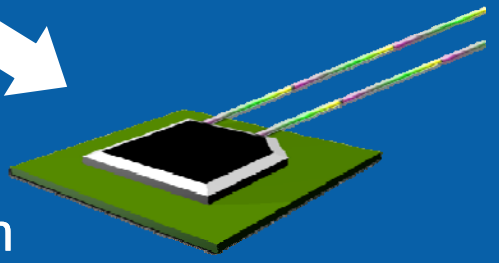


A future integrated terabit per second optical link on a single chip

Integrating into a Tera-scale System



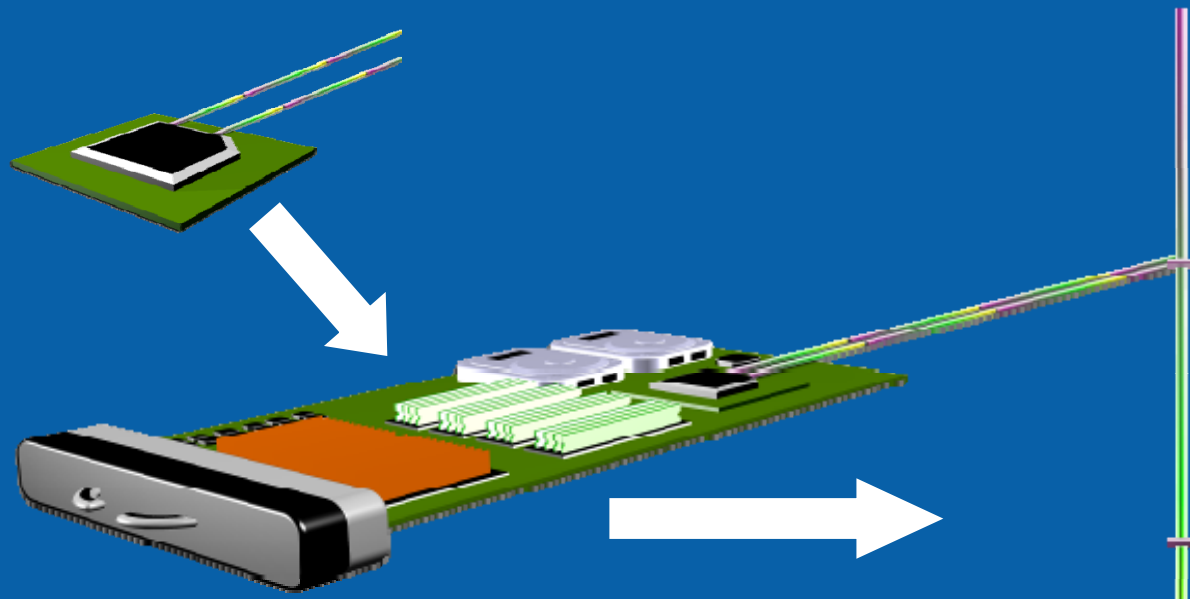




This transmitter would be combined with a receiver

Which could then be built into an integrated, silicon photonic chip!!

Integrating into a Tera-scale System



This integrated silicon photonic chip could then be integrated into computer boards

And this board could be integrated into a Tera-sca system

Summary

Future multi-core processors will continue to drive I/O bandwidth needs to ~Tb/s data rates in near future pushing need for optical interconnects

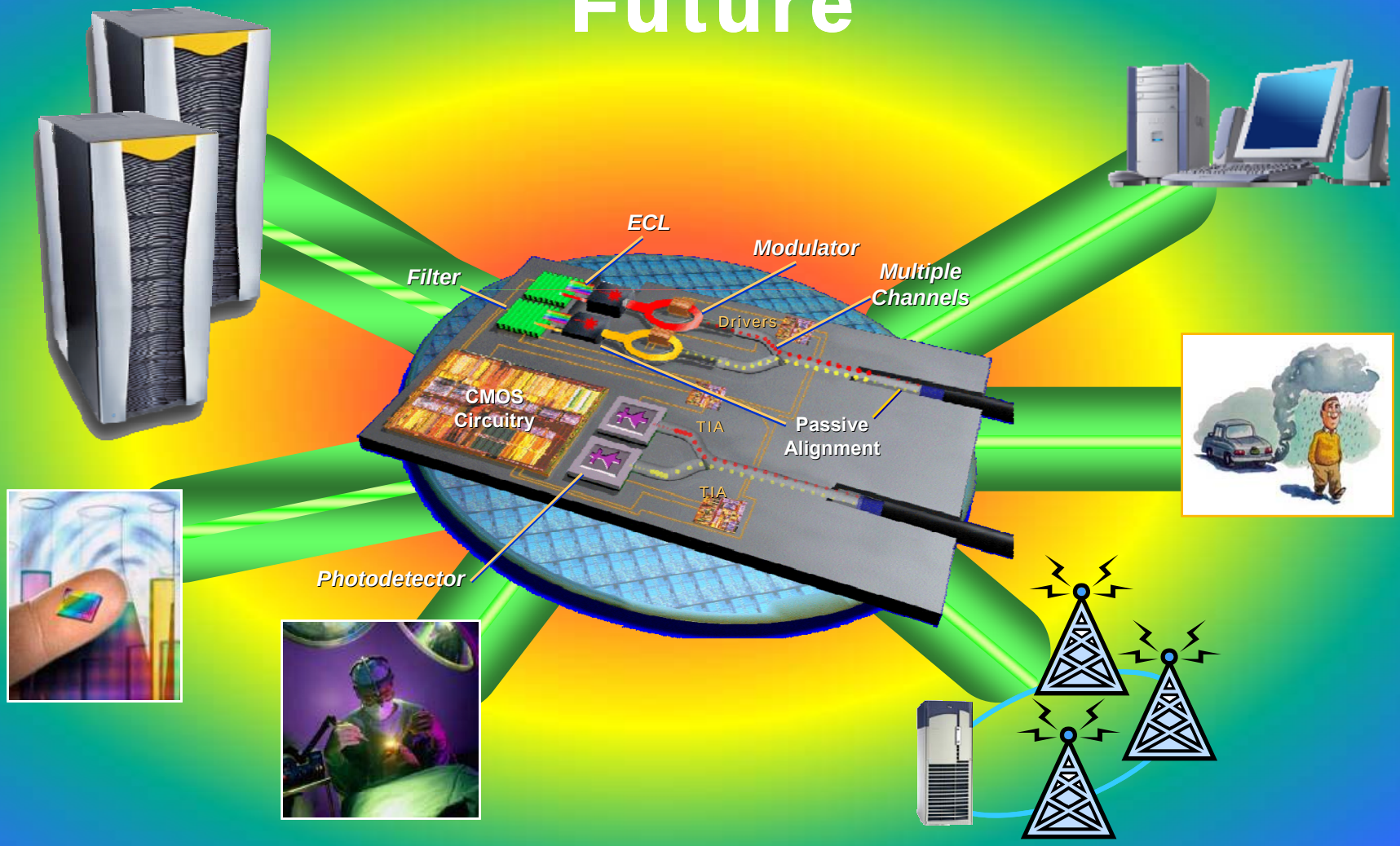
Cost will be primary driver for enabling optical links in and around the PC and Server

Silicon Photonics device performance advancing at a rapid rate. Need to continue pushing higher levels of integration (ie 200G, 400G etc)

Next phase of challenges will be with integration combined with low cost packaging

Overall solution must focus on power efficiency, integration and cost tradeoffs

Silicon Photonics' Future



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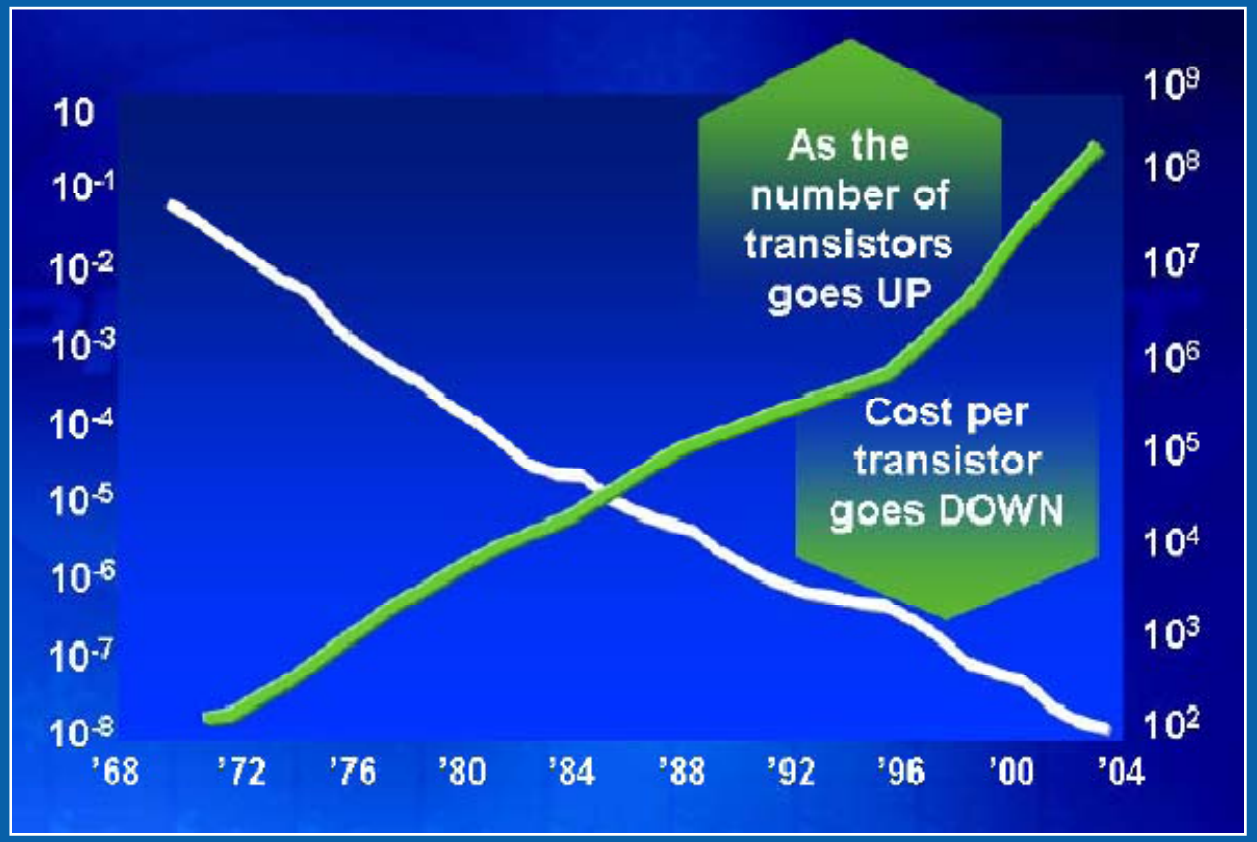
Leap ahead

Electronics:
Economics of Moore's Law

SCALING + WAFER SIZE + HIGH VOLUME = LOWER COST



Integration & increased functionality

The Opportunity of Silicon Photonics

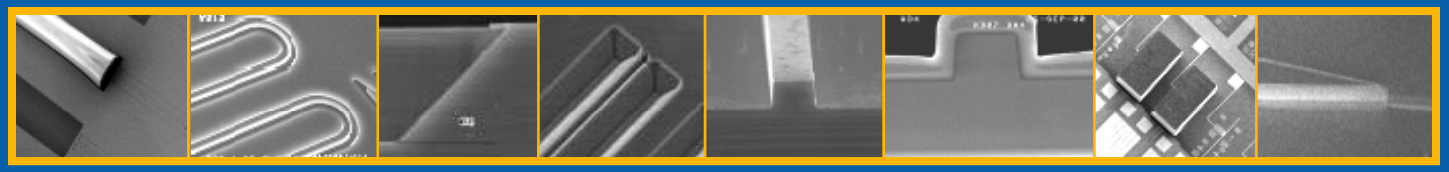
Enormous ($ billions) CMOS infrastructure, process learning, and capacity

- Draft continued investment in Moore's law

Potential to integrate multiple optical devices

Micromachining could provide smart packaging

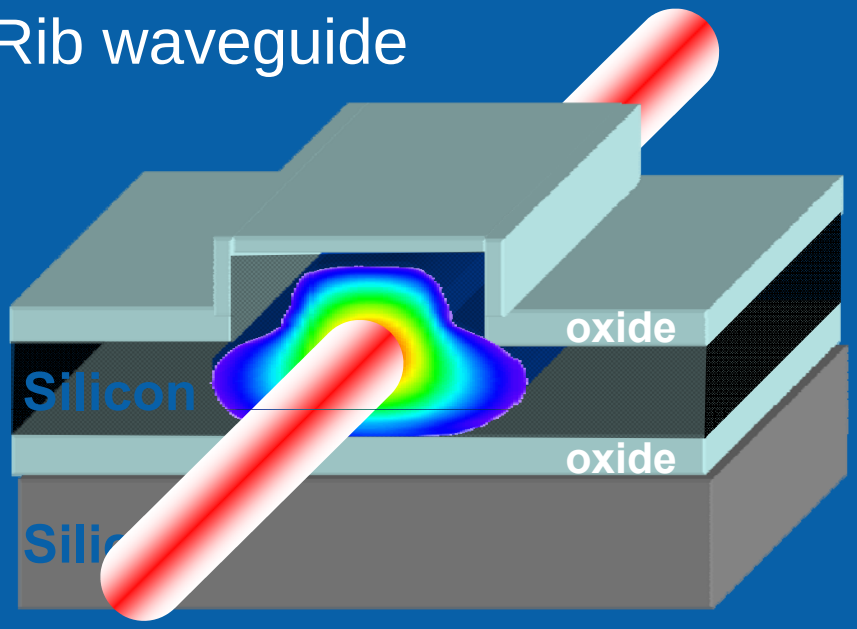
Potential to converge computing & communications

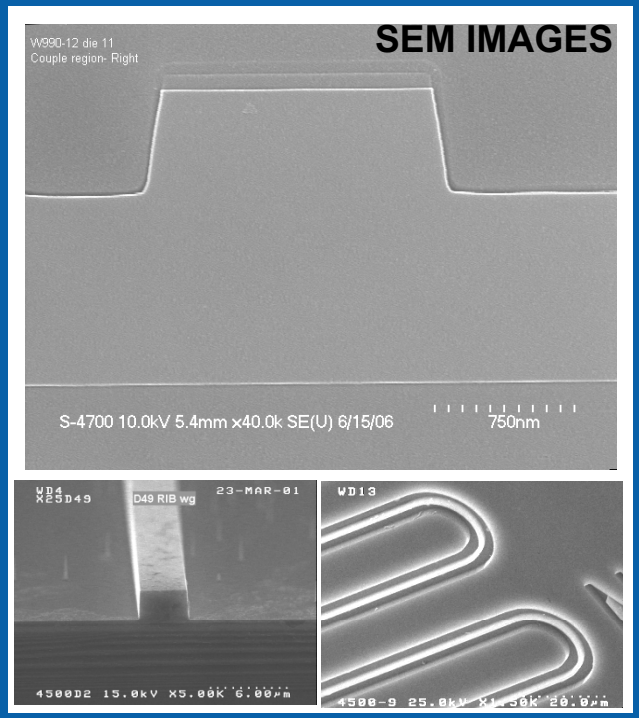


To benefit from this optical wafers must run alongside existing product.

Guiding Light with Si Waveguides

Ex: Rib waveguide





- Proven area for silicon
- High index = small structures
  - Strip and Photonic crystals for further scaling
- Splitters, couplers, gratings, AWGs, MMIs have all been demonstrated

Continue *to reduce size while maintaining performance*

intel Leap ahead™