Nanotechnology: State-of-the-Art and Applications

Nanotechnology in the Semiconductor Industry

May 19, 2010
Hans Stork, PhD.
Group VP and CTO, Silicon Systems Group
Applied Materials

think it. apply it.™

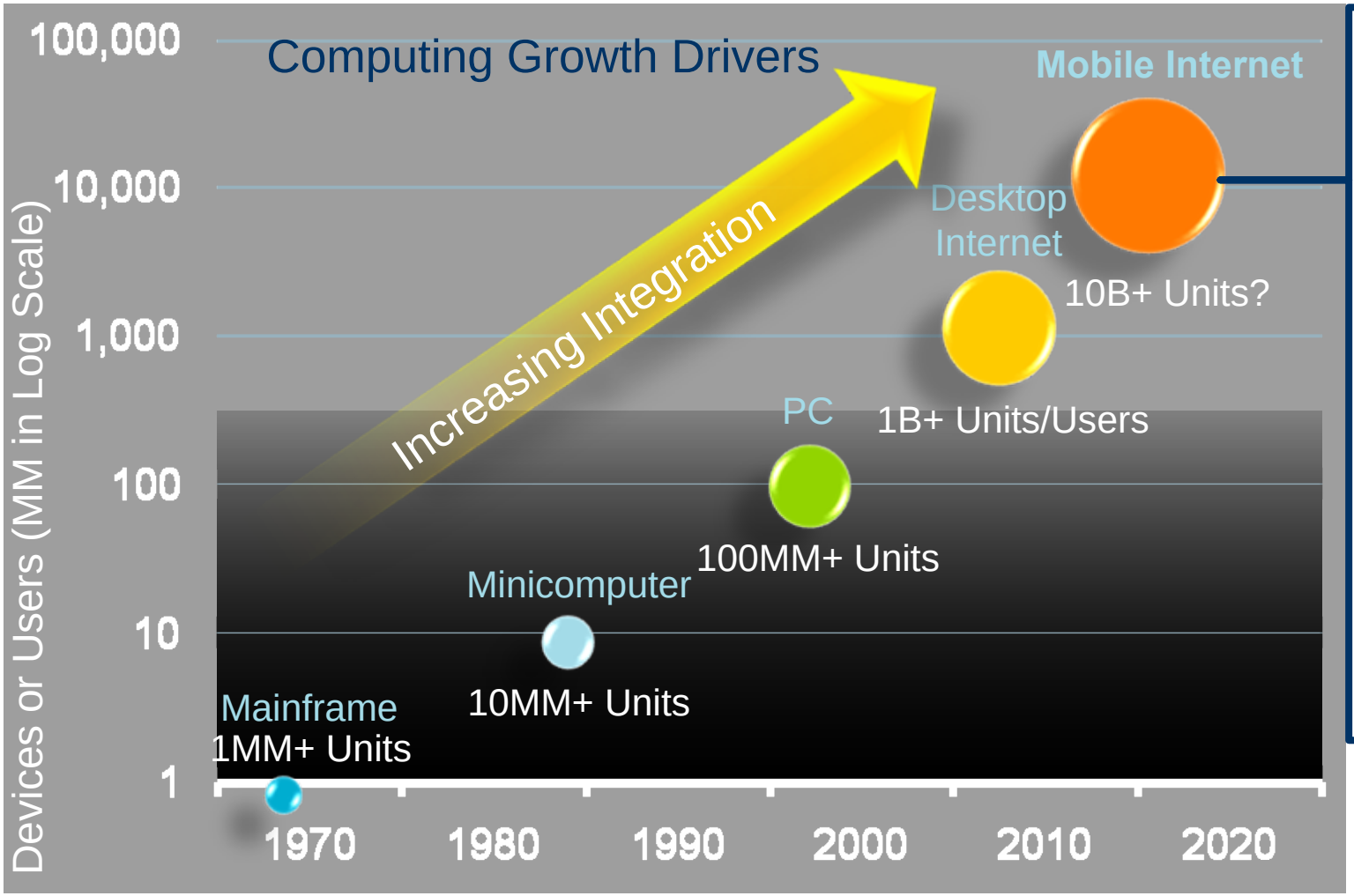
External Use

Outline

- Introduction
- Moore's Law and Device Scaling
- Process Challenges and Technology Solutions
  - Lithography and Patterning
  - Front-End-of-Line
  - Back-End-of-Line
  - Inspection and Defect Control
- Summary

External Use

Pervasiveness of Semiconductors



Scaling enabled exponential unit growth…

Source: Morgan Stanley

External Use

“Applied Inside” the iPad 3G 64GB

DISPLAY
(>20% of iPad BOM*)

Enabled by Applied’s CVD, PVD, Test, and WEB equipments

Touch panel
Capacitive multitouch

LCD Display
9.7” LED backlit panel

SEMICONDUCTOR
(>30% of iPad BOM*)

Enabled by Applied’s CMP, CVD, ECD, Epi, Etch, Inspection, Gate, PVD, and RTP equipments

Microprocessor

256MB DRAM

64GB MLC NAND Flash

I/O Controller

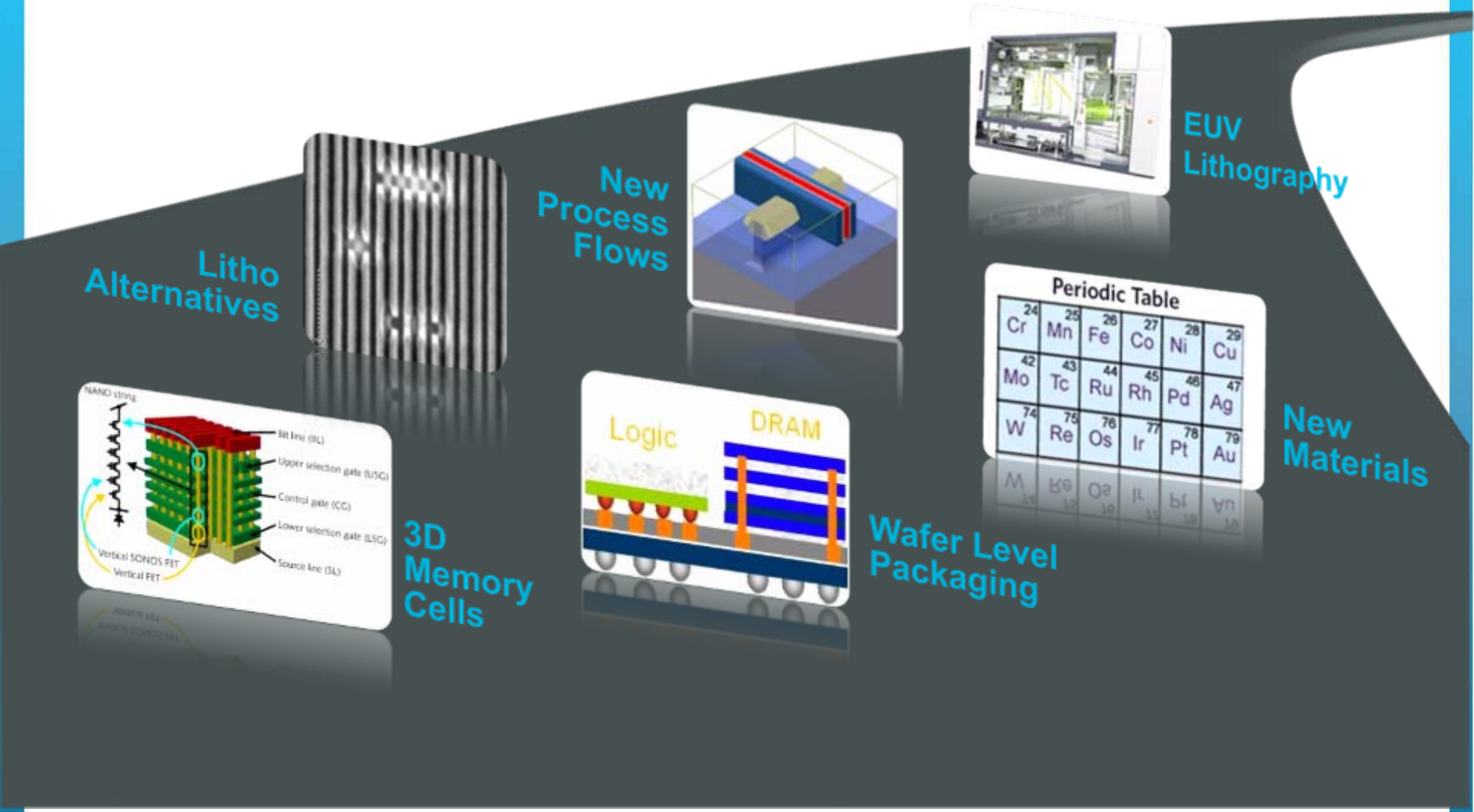
Multi-Touch Controller

Applied Materials equipment used to manufacture over 50% of iPad Bill of Materials*

*Value basis
Sources: iFixit.com, UBS, and Applied Materials estimates

External Use

Technology Evolution



Enabled by continuous improvement AND step function change

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Moore's Law and Scaling to Continue

90nm	65nm	45nm	32nm	22nm	15nm	11nm	08 ?
2003	2005	2007	2009	2011	2013	2015	2017

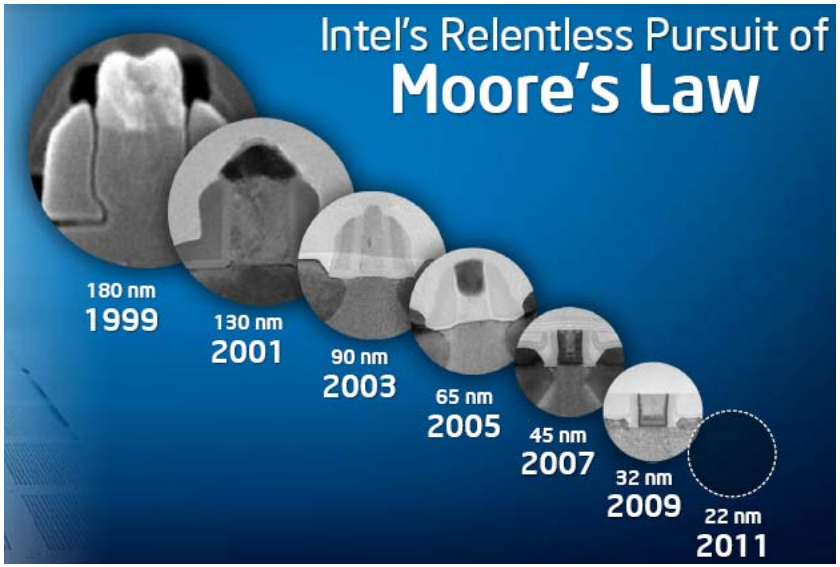
Strained channels (stress liner, Stress Memorization, eSiGe, eSiC)

High k Metal Gate (Gate-first, Replacement Metal Gate)

New channel materials (SiGe, Ge, III-V)

FinFET, ET SOI (fully depleted devices)

Nanowire devices



Source:

Paul Otellini, Intel CEO, "Building a Continuum of Computing", Opening Keynote, Intel Developer Forum 2009, San Francisco, Sep 22 – 24, 2009

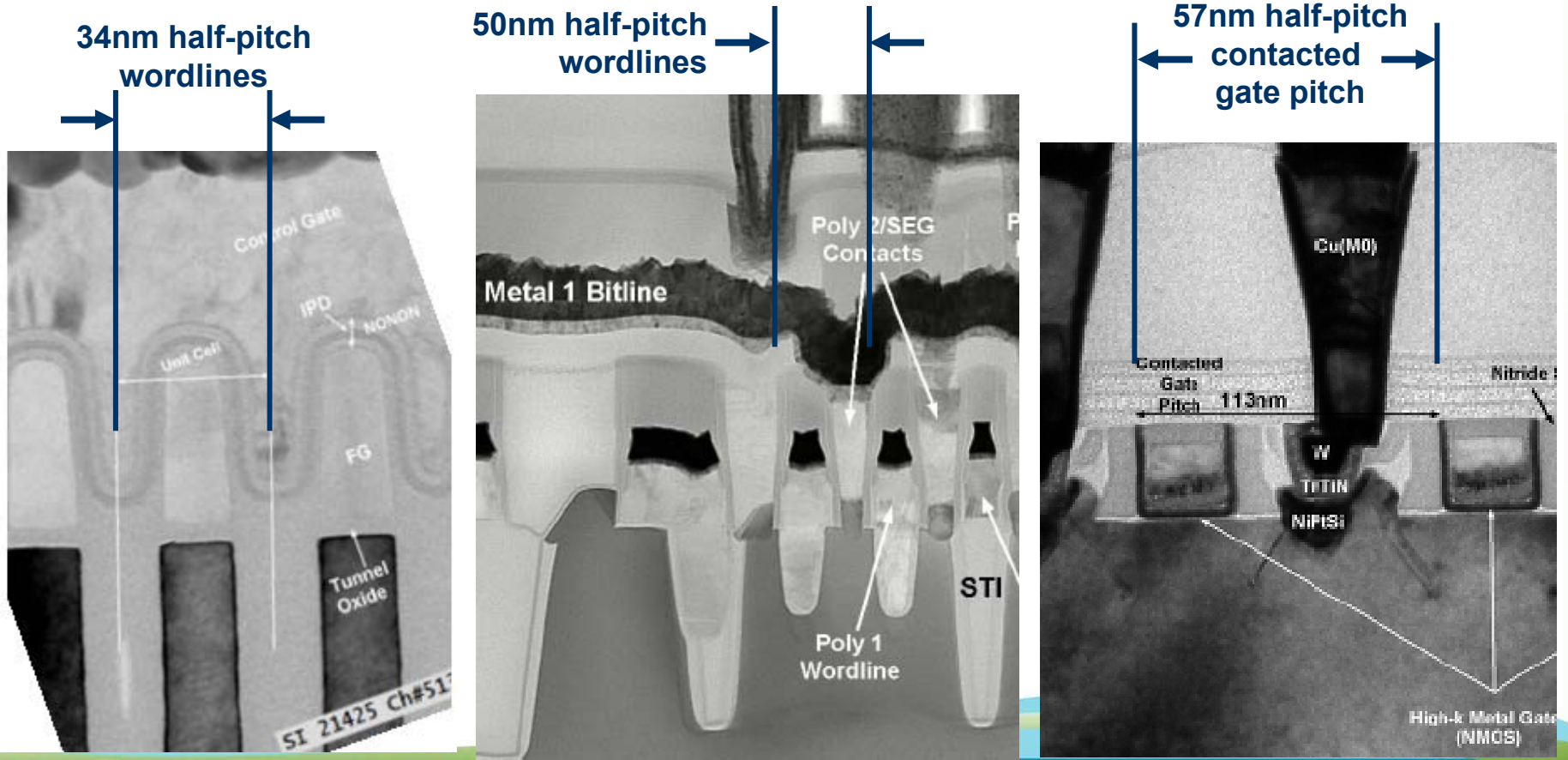
Definition of Node – Logic vs. Memory

- Memory (NAND and DRAM) "Node" **=** half-pitch of minimum feature size, e.g. wordlines,
- Logic "Node" **≠** half-pitch of any minimum feature size,

34nm Node 32Gbit NAND Flash from IM Flash Technologies, an Intel Micron Venture

50nm Node 1Gbit DDR2 DRAM from Micron Technology, Inc.

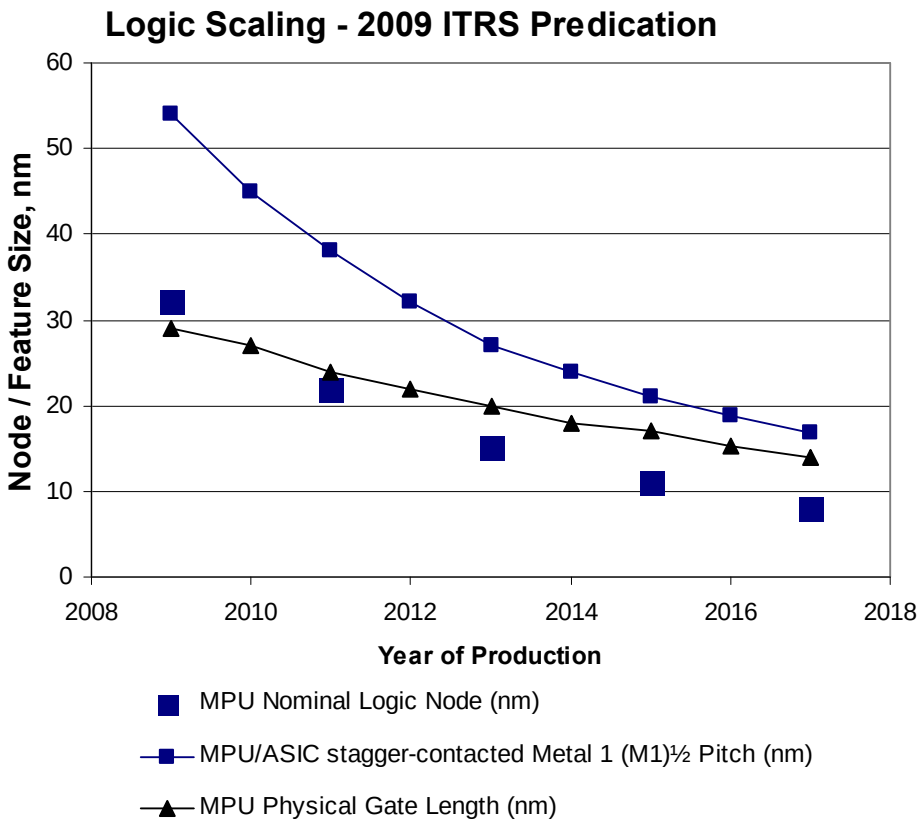
32nm Node Microprocessor with High k Metal Gate from Intel Corporation

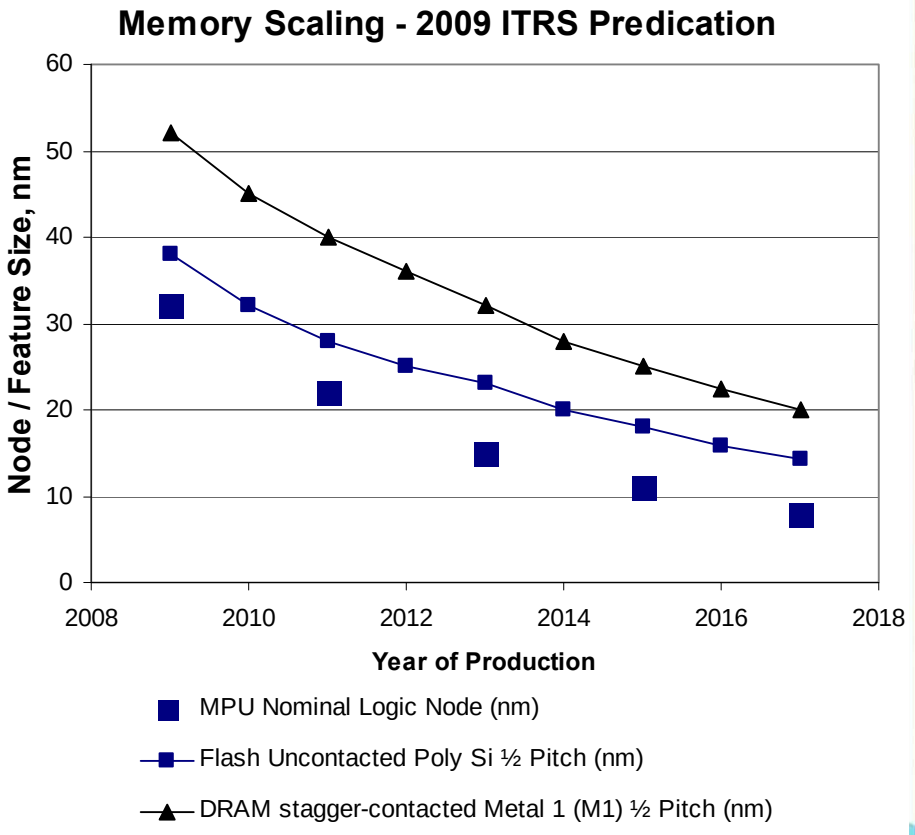


Source: Semiconductor Insights Reports

International Technology Roadmap for Semiconductors

- **Logic Scaling**, MPU physical gate length in nm is close to nominal logic node now, but will scale slower than node scaling in the future; MPU M1 half-pitch (the ITRS definition of Logic Node) is much larger than nominal node
- **Memory Scaling**, DRAM node = M1 half-pitch in nm, is larger than Flash NAND poly half-pitch; both are larger than nominal logic node (but smaller than MPU contacted gate half-pitch),





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Lithography Roadmap for Critical Layers

90nm	65nm	45nm	32nm	22nm	15nm	11nm	08 ?
2003	2005	2007	2009	2011	2013	2015	2017

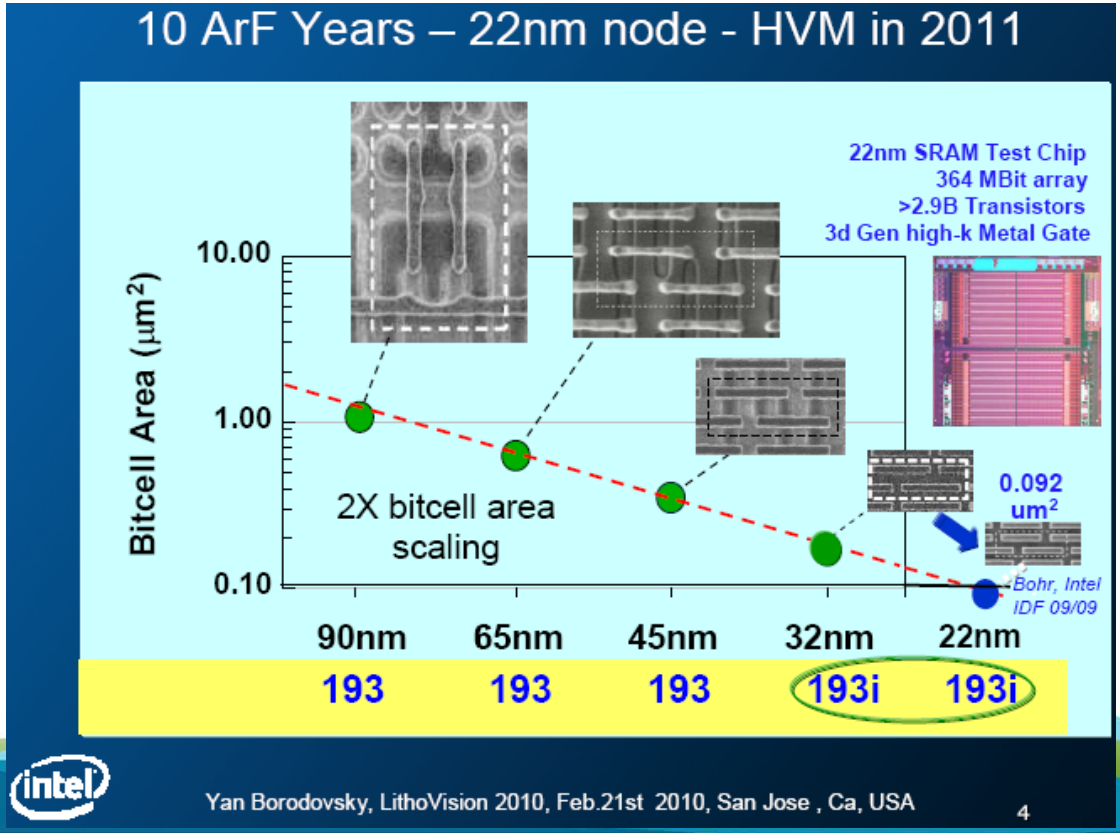
DUV 193nm Lithography

Immersion DUV 193i (adopted by some Logic and all DRAM makers)

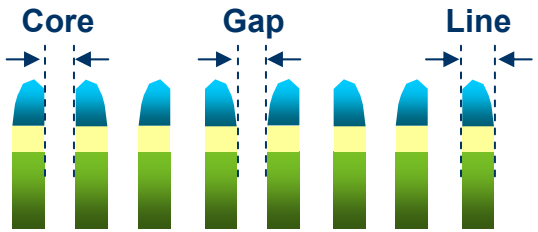
193i with Pitch Division

193i + EUVL / EBDW

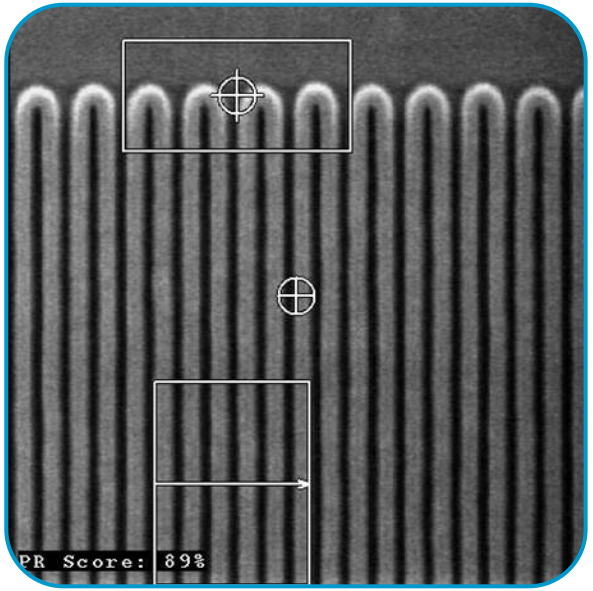
- First adoption of immersion DUV
  - Intel started using 193i at 32nm
  - TSMC and IBM started 193i at 45nm
  - DRAM makers started using 193i around 50nm (true 50nm half-pitch)
- 193i with Pitch Division
  - Self-Aligned-Double-Patterning
  - Litho-Etch-Litho-Etch,
- Next Generation Litho
  - Extreme UV Litho,
  - E-Beam-Direct Write
  - Massively Parallel EBDW



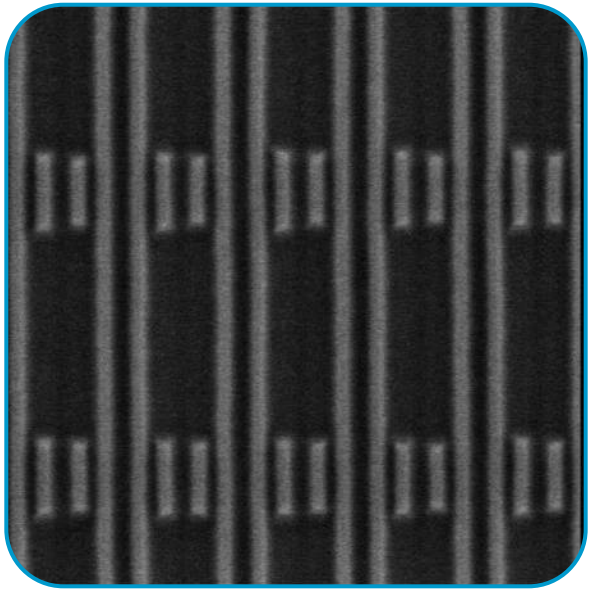
Self-Aligned Double Patterning (SADP)



22nm Half-Pitch Oxide



22nm Half-Pitch STI



Line CDU 3σ	1.0 nm	1.1 nm
Gap CDU 3σ	1.4 nm	2.5 nm
Core CDU 3σ	1.8 nm	2.0 nm
Line Width Roughness (LWR)	1.6 nm	1.6 nm

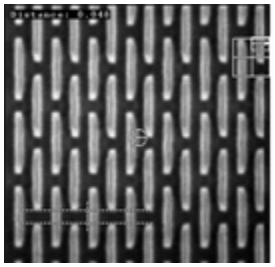
Demonstrated 22nm line and space patterning with <10% CDU and LWR

External Use

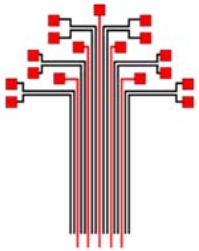
SADP: Evolving for all Market Segments

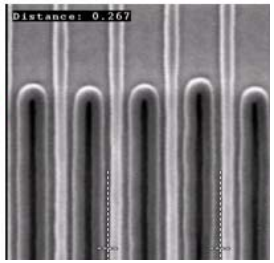
Memory Patterns

DRAM STI
64nm Pitch
SADP and Cut

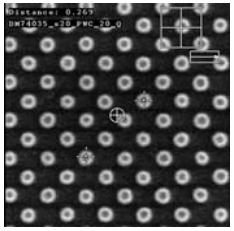


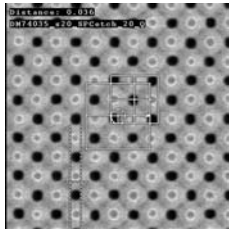
NAND Arrays
Frequency Tripling

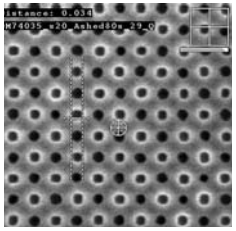




DRAM Container Pattern







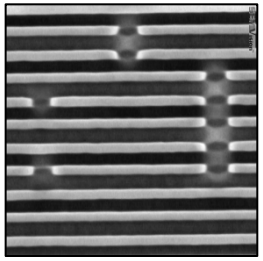
Immersion
Pillars

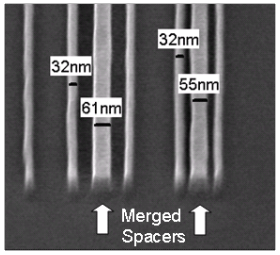
SADP

64nm Pitch
Contacts

Logic Patterns

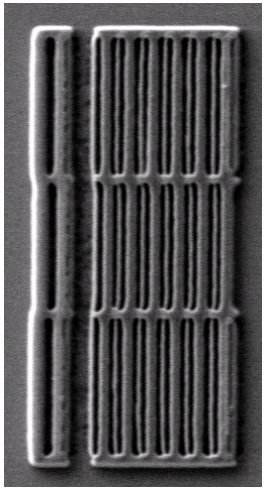
Gridded Poly
56nm Pitch
SADP and Cut





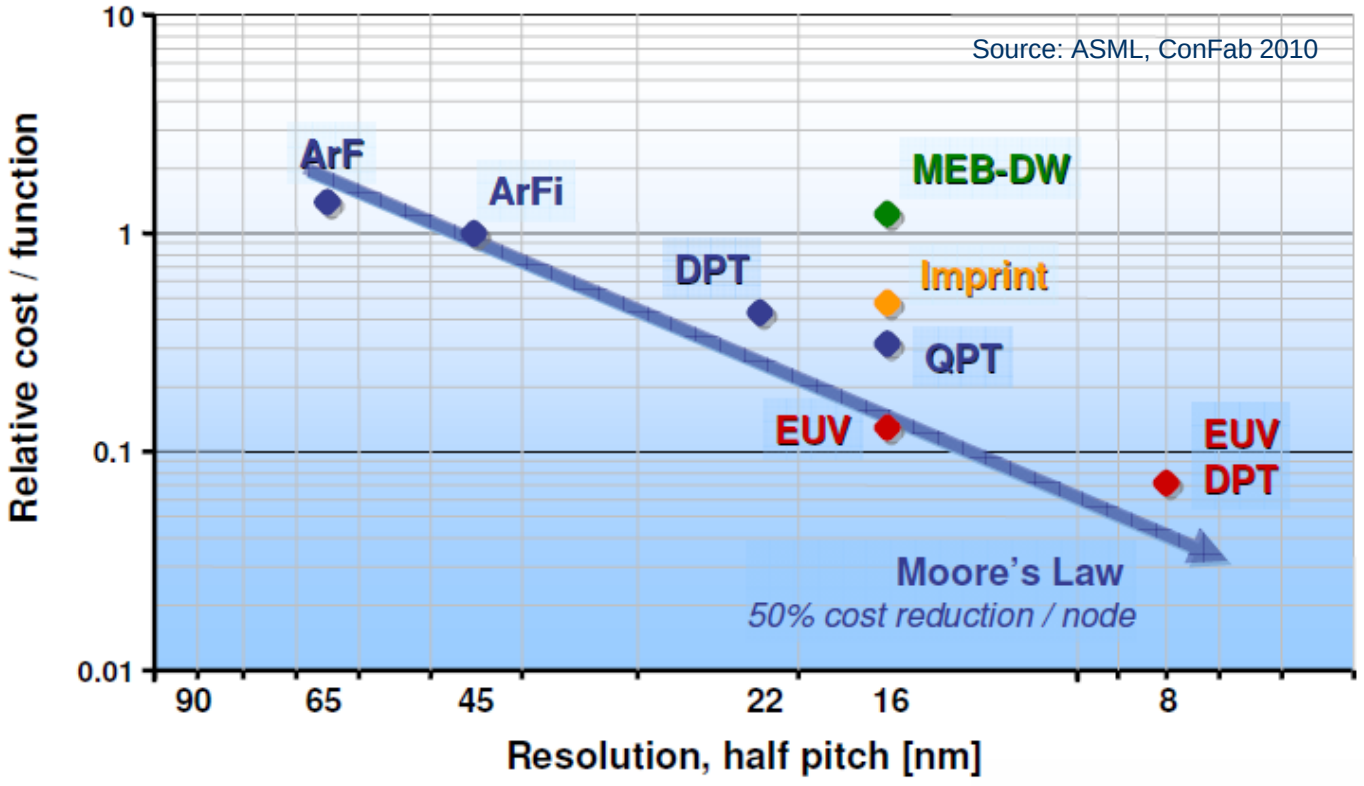
Non-Gridded Poly
Multiple CD / Pitch
SADP and Cut

BEOL
56nm Pitch
SADP and Block



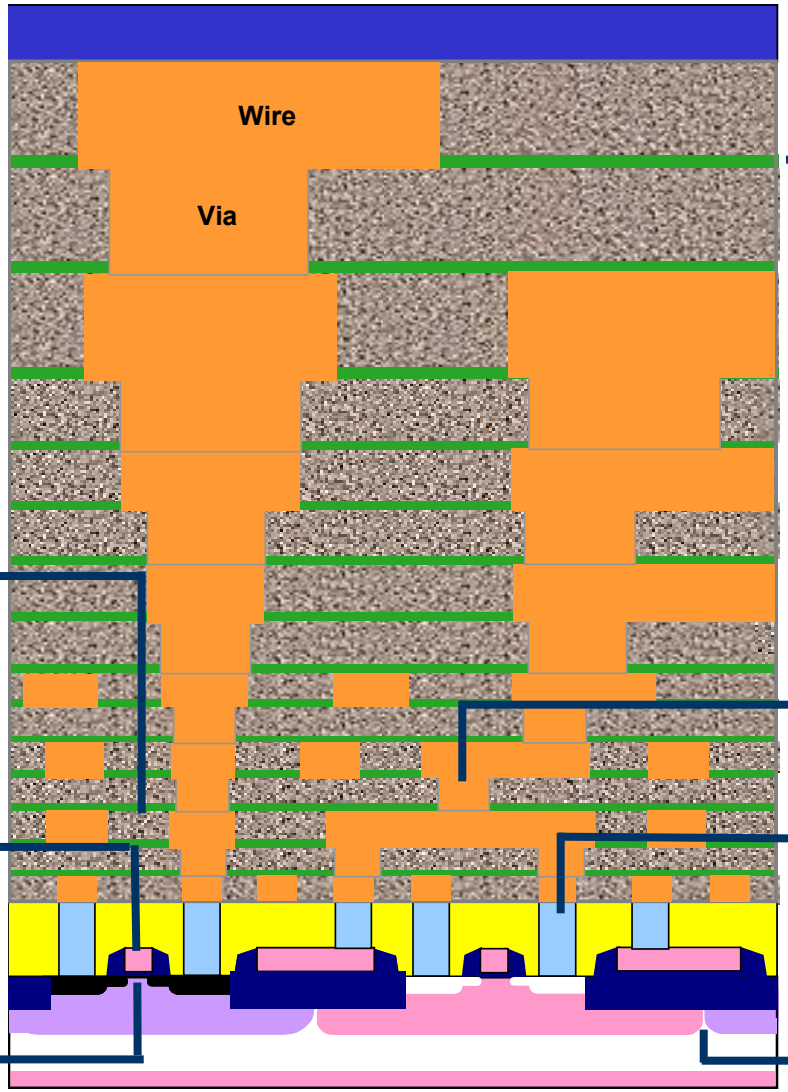
Mixed CD
Mixed Pitch
Off-Grid / Jogs
40nm Tip-Tip

EUV should keep us on Moore's Law



Progress encouraging, but infrastructure and learning cycles challenging

Process Technologies for MPU/Logic



BF, DF Inspection,
Defect Review SEM,
CD SEM,
E-Beam Inspection,
Mask Inspection

Low k Dielectric,
Low k Dielectric
Barrier, Patterning
Film/Hardmask,
Dielectric Etch

Cu B/S, Cu CMP

Gate Dielectric,
Gate Conductor,
Gate Stack Etch

PMD, Contact
Liner, Low R W

RTP, DSA, EPI RP
S/D, Stress Nitride

STI Etch, STI
Liner, STI Fill,
STI CMP

* Typical MPU cross section, from ITRS Interconnect Working Group

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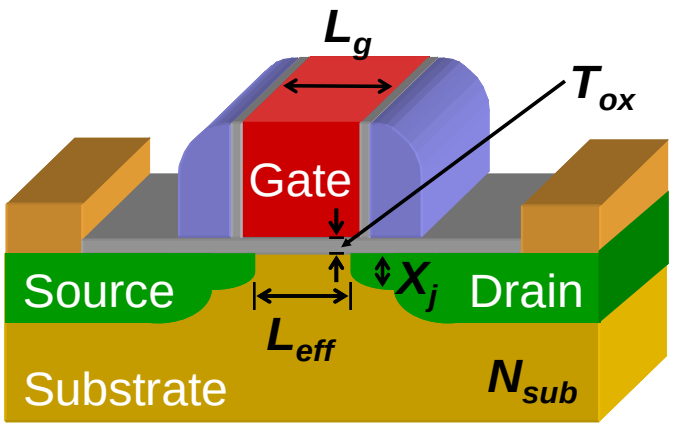
CMOS Device Inflections

- **Material Innovation**
  - Poly/SiO(N) to HKMG transition started at 45/32nm Node
- **Device / Structure Innovation**
  - Planar CMOS to FinFET (Tri-gate) transition is likely to start at 15nm Node,

Leading HP Logic	65nm	45nm	32nm	22nm	15nm
Gate Stack	poly/SiON	⇨ HKMG	HKMG	HKMG	HKMG
MOSFET	planar	planar	planar	FinFET	⇨ FinFET

Bulk-Si Planar MOSFET

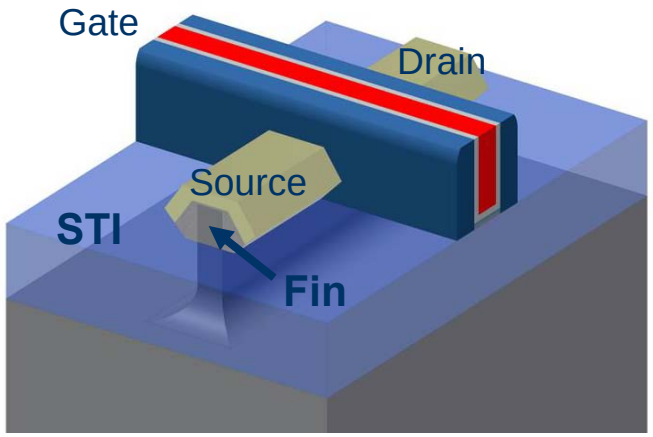


(~1970 to present)

scaling to
L_g < 20 nm

(beyond 2010)

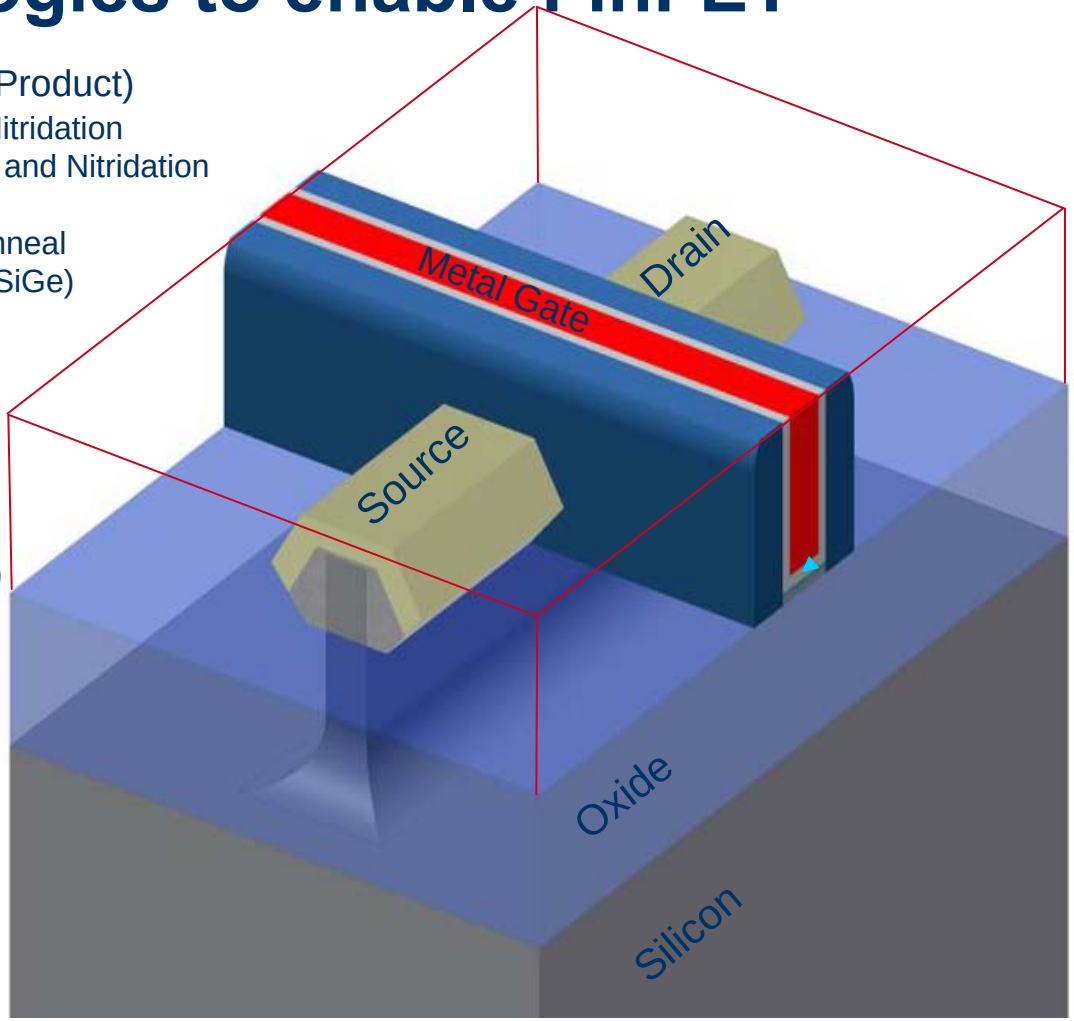
Bulk FinFET MOSFET



(~ 15nm node)

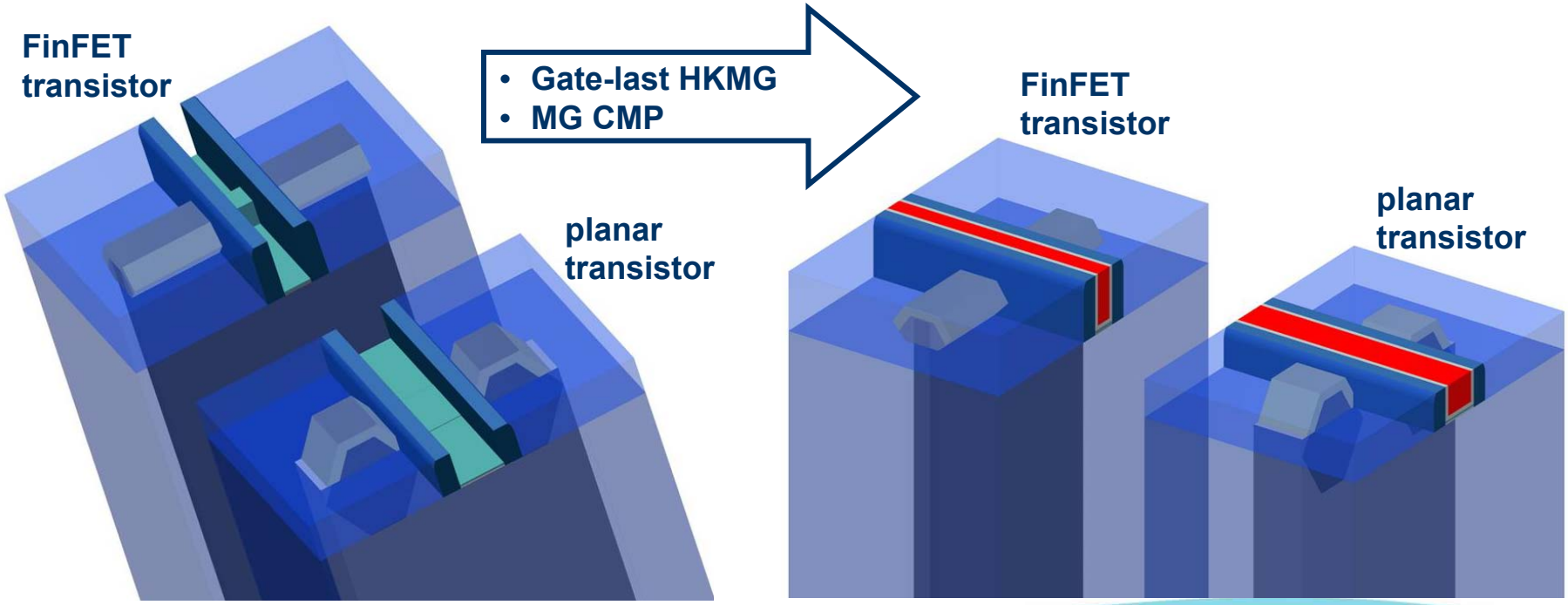
Applied Technologies to enable FinFET

- FEP (Front End Product)
  - Base Oxide and Nitridation
  - High-k Deposition and Nitridation
  - Doping
  - RTP and Laser Anneal
  - EPI (Si, SiC, and SiGe)
- Etch
  - Fin Etch (i.e. STI Etch)
  - STI Oxide Recess Etch
  - Gate Etch
  - Side-Wall-Spacer Etch
- MDP (Metal Deposition Product)
  - Dielectric Capping Film
  - Work Function Films
  - Barrier Film
  - Bulk Metal Fill
- CMP
  - STI CMP
  - Polysilicon Planarization
  - Poly Gate Opening Polish
  - Metal Gate Polish
- DSM (Dielectric Product)
  - Dielectric Film as Doping Source
  - Low-k Side-Wall-Spacer Film
  - Low Temp Oxide Liner/Spacer
  - PMD Film
  - Patterning Film
- PDC (Process Diagnostic and Control)
  - Fin sidewall angle control
  - Detection and review of defects on fin sidewall
  - Gate cd control across fin height



Hypothetical FinFET Implementation

- FinFET or Tri-gate transistors could be fabricated on 1) SOI, or 2) bulk substrate; cost vs. process complexity trade-off,
- FinFET and planar CMOS transistors are likely fabricated simultaneously on same chip, at least initially,
- For HKMG, Replacement Metal Gate (or, Gate-Last HKMG) likely to be adopted,
- Gate Trench for MG fill very challenging with very high Aspect Ratio (need for ALD)



External Use

III-V Channel on Silicon – Another Inflection?

- Technical challenges to be overcome
  - Defect-free, III-V EPI channel materials on silicon substrate with buffer under-layers,
  - High-k gate dielectric on III-V,
  - Low resistance source/drain contacts,
- To be manufacturable
  - Intel demonstration of III-V devices (2009 IEDM) done on EPI by Molecular Beam Epitaxial technology
  - MOCVD EPI technology on 300mm wafers required,

EE Times:

Intel's Gargini pushes III-V-on-silicon as 2015 transistor option

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Peter Clarke
EE Times
(02/12/2010 7:56 AM EST)

LONDON — A presentation prepared by Paolo Gargini, Intel's director of technology strategy, to give to the Industry Strategy Symposium Europe, held in Dublin, Ireland, earlier this week, stressed Intel's progress in adding compound semiconductor layers to silicon as a means of continuing scaling and reducing power consumption.

Gargini, also chairman of the International Technology Roadmap for Semiconductors (ITRS), said in the presentation that the inclusion of III-V materials is a 2015 transistor option that could deliver either three times the performance of silicon at the same power consumption, or deliver the same performance as silicon at one-tenth the power consumption. However, integration of a thin compound semiconductor transistor channel with conventional silicon manufacturing would be the key to adoption.

Demonstration of III-V Devices on Si

- 2009 IEDM, Intel paper, “Advanced High-K Gate Dielectric for High-Performance Short-Channel $In_{0.7}Ga_{0.3}As$ Quantum Well Field Effect Transistors on Silicon Substrate for Low Power Logic Applications”, M. Radosavljevic, et al,
- High transconductance and high drive current demonstrated at **0.5 V**,
- Manufacturable EPI technology required for commercial adoption, e.g. MOCVD EPI technology on 300mm wafers

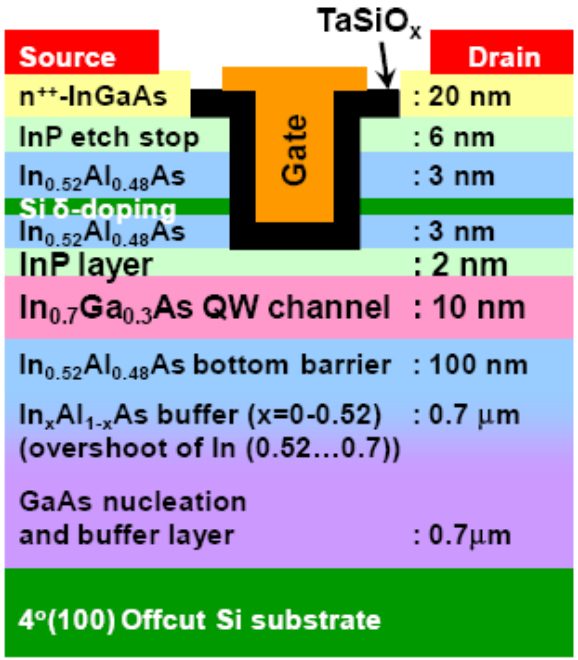


Fig. 4: Schematic of $In_{0.7}Ga_{0.3}As$ QWFET on silicon with 2nm InP upper barrier layer and a 4nm $TaSiO_x$ high-K gate dielectric, which form a composite $TaSiO_x$-InP gate stack.

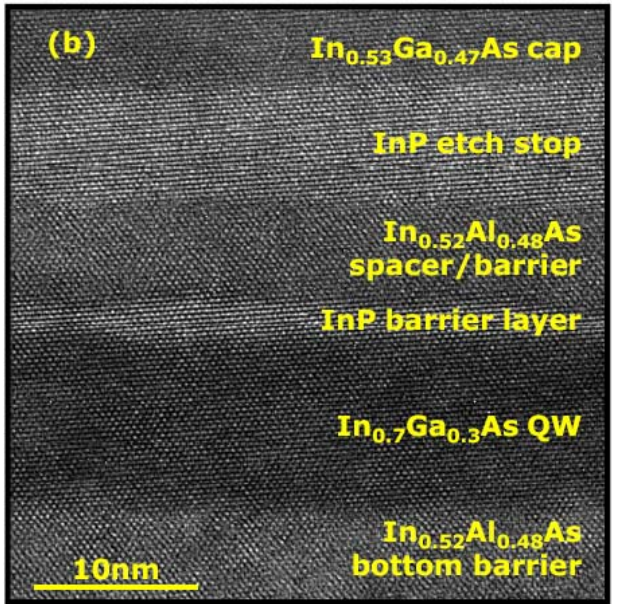
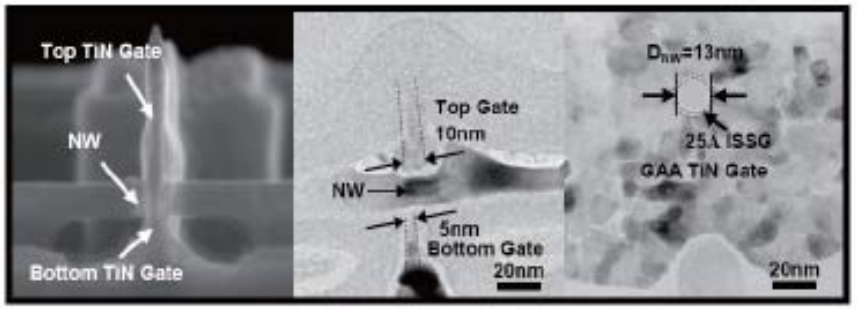


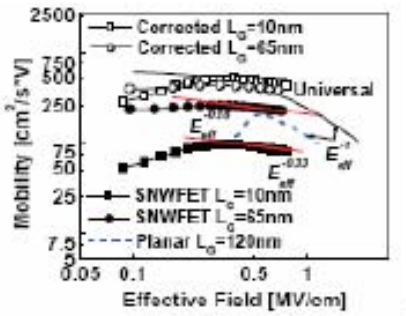
Fig. 6(b): High-resolution TEM micrograph of $In_{0.7}Ga_{0.3}As$ QW stack with 2nm InP top barrier layer. All III-V layers were grown using MBE.

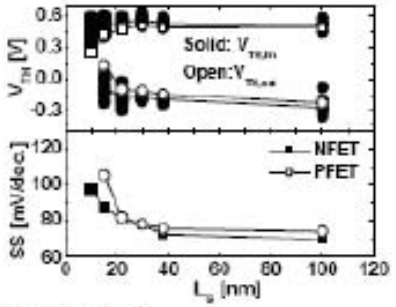
External Use

Silicon Nano-Wires : Ultimate in SC Control

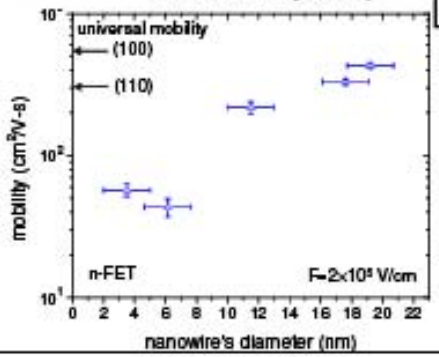
- **Benefit:**
  - Ultimate SC control
    - Gate control from many directions
  - "Correct" minimum W for beyond 11 nm, i.e. enable <10 nm widths
- **Challenge:**
  - Transport
  - Contact resistance, ...

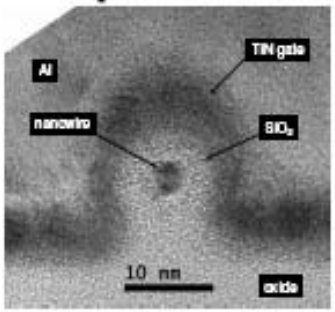






[Cohen 08]





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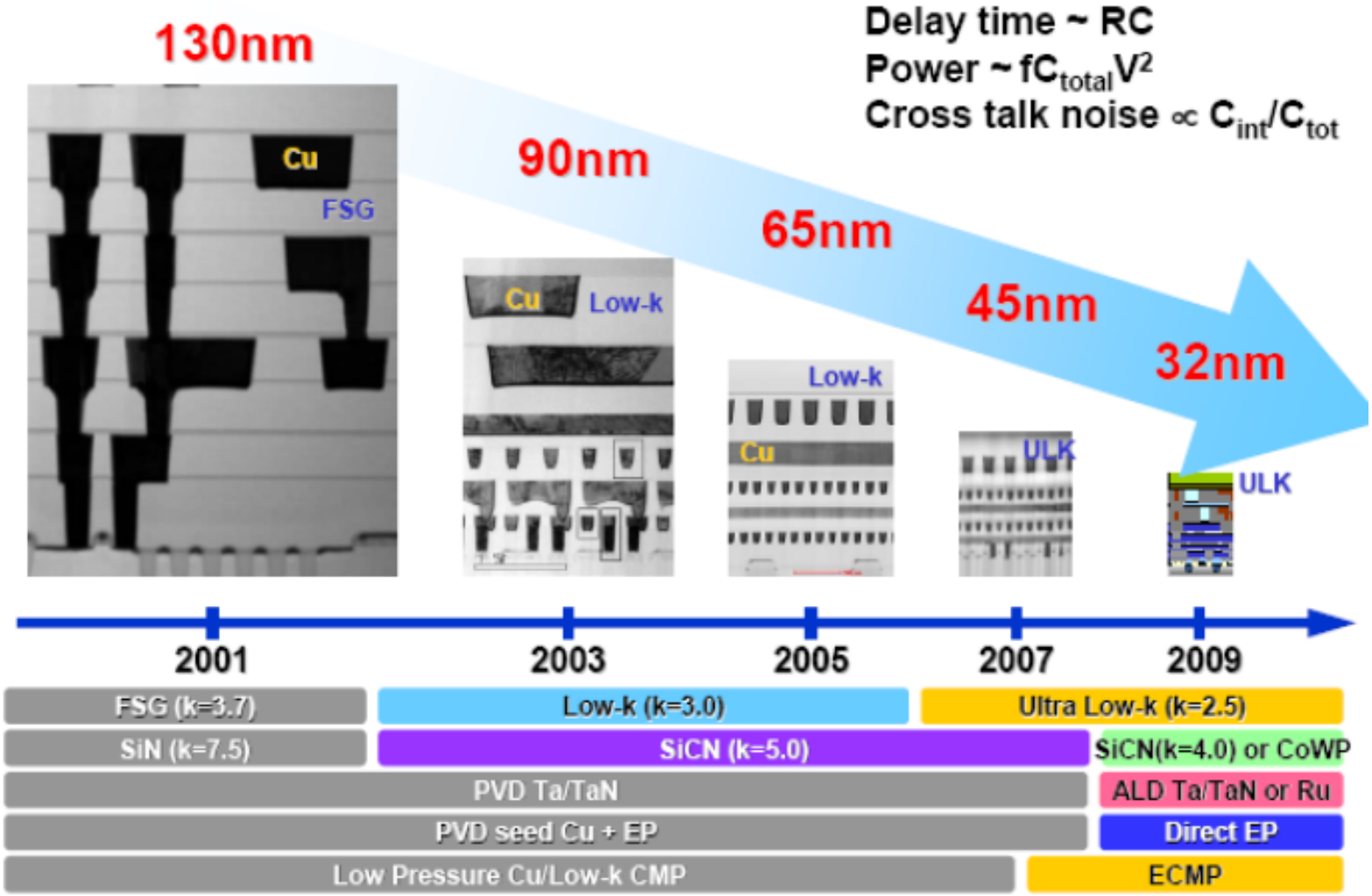
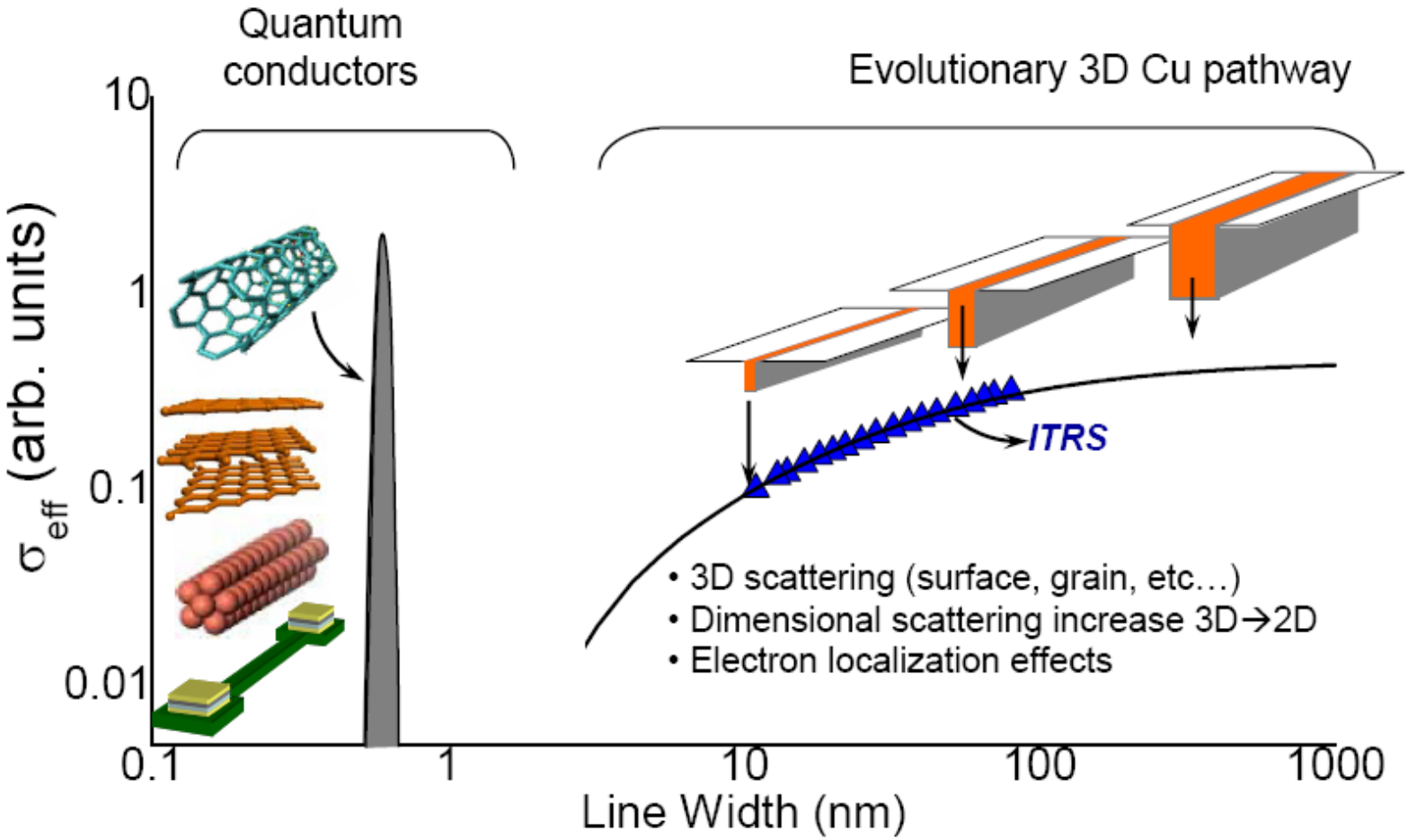
BEOL Technology Evolution – 130 to 32nm Node



Source: Interconnect Roadmap, H.-K Kang, tutorial on Advanced Logic Technology, 2007, from 2008 IEDM short course, "BEOL Technology for 22nm Technology Node", Jeff Gambino, IBM,

Alternate Approach for Interconnect

- **To exploit alternate functionality/transport in quantum systems**



"Evolution of On-chip Interconnects for Equivalent Scaling: To 22nm and Beyond", Robert Geer and Wei Wang, College of Nanoscale Science and Engineering, University at Albany, SUNY, Semicon West TechXPOT, July 14, 2009

BEOL Scaling Roadmap

90nm	65nm	45nm	32nm	22nm	15nm	11nm	08 ?
2003	2005	2007	2009	2011	2013	2015	2017

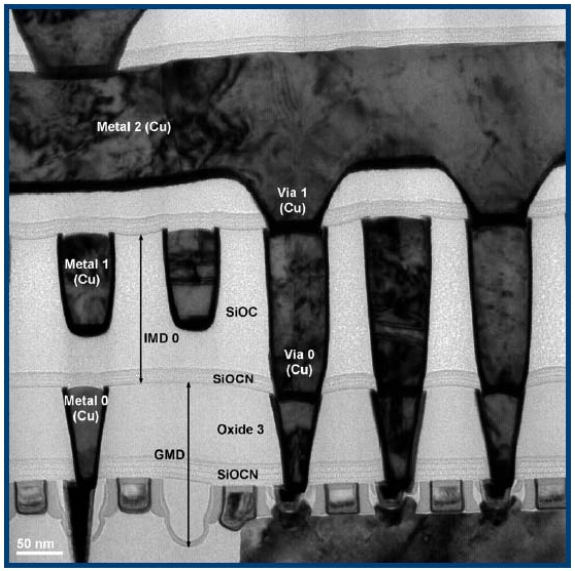
Low-k dielectric & dielectric barrier, PVD Ta/TaN, CMP → Ultra Low-k dielectric →

ALD Ta/TaN, or Ta/Ru →

Air-gap →

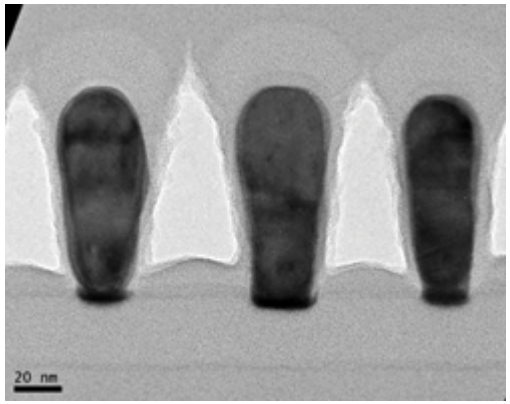
Optical interconnect ⋯⋯▸

Cu-Low k interconnect in Intel 32nm Microprocessor



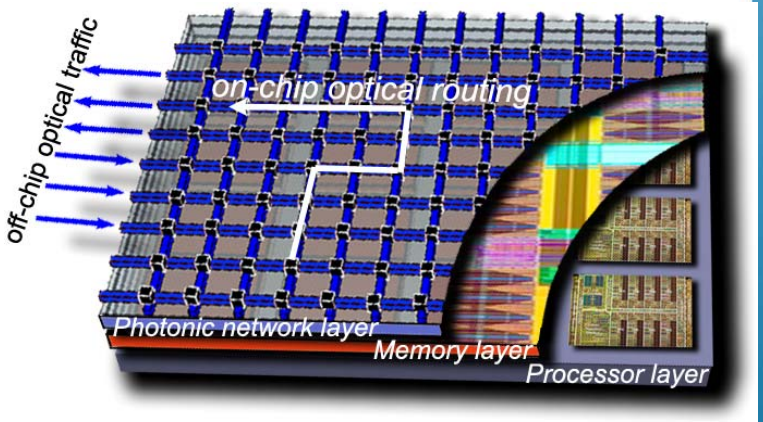
Source: Semiconductor Insights report

Air-Gaps w/ 50% lower capacitance than SiO2



Source: Semiconductor International, "IMEC Reveals Interconnect Roadmap to 10nm" by Laura Peters, 7/4/2009

On-chip Optical interconnect



Source: IBM website, updated Mar 4, 2010; Nanophotonic network for on-chip optical interconnect, for implementation post-2018

Outline

- Introduction
- Moore's Law and Device Scaling
- Process Challenges and Technology Solutions
  - Lithography and Patterning
  - Front-End-of-Line
  - Back-End-of-Line
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External Use

Defect Inspection Roadmap

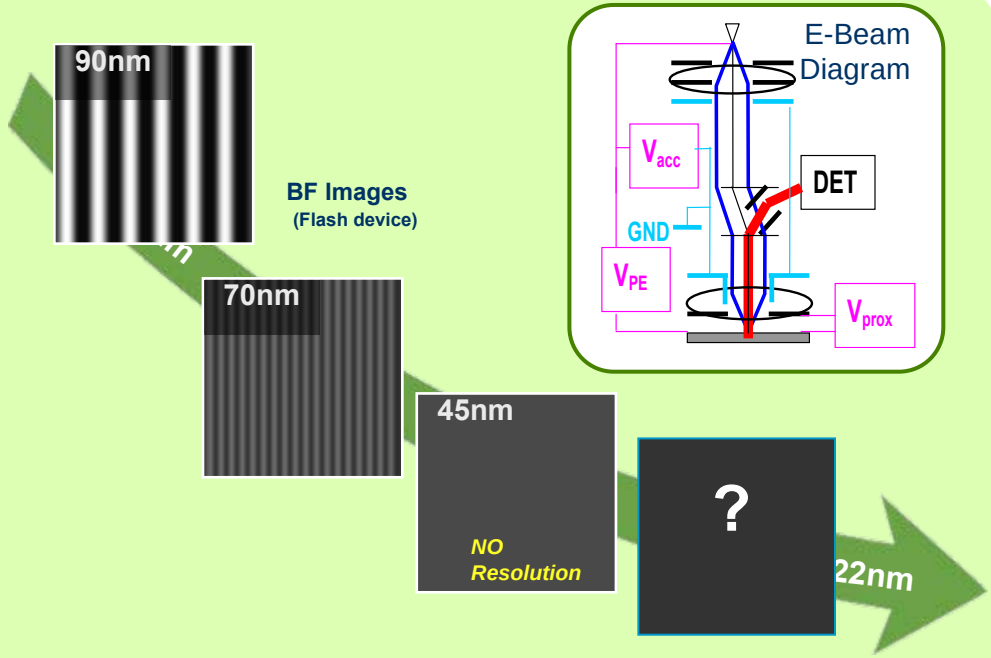
90nm	65nm	45nm	32nm	22nm	15nm	11nm	08 ?
2003	2005	2007	2009	2011	2013	2015	2017

UV Lamp

DUV Laser

E-Beam Based inspection

- Smallest defects are of similar dimensions as design rule
- Traditional brightfield imaging resolution of optical tools is reaching its limits
- E-beam based inspection has the necessary resolution to detect <30nm defects



What is a Defect?

For example…

Bridging

Protrusion

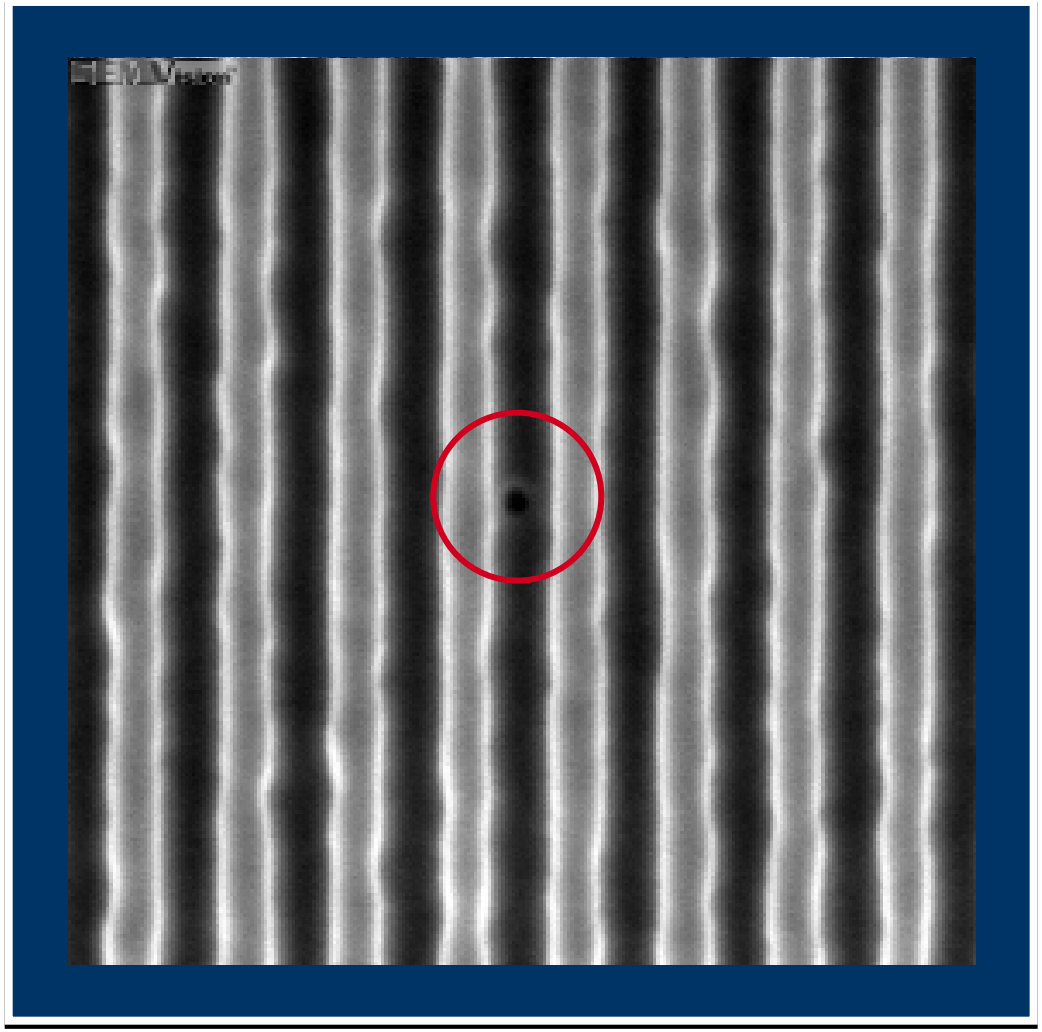
Particle

Line thinning

Scratch

Residue

Void

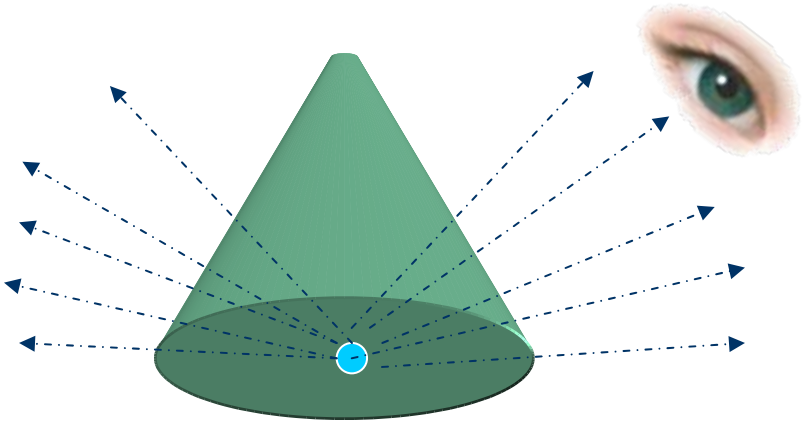


An undesirable local change that may kill the chip or affect its reliability

External Use

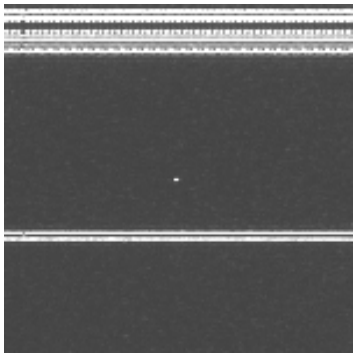
Optical Wafer Inspection Technologies

Dark-field



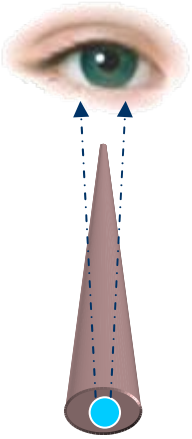
Spot size >> defect size
Collecting scattered light

Signal-to-Noise ratio determines detection



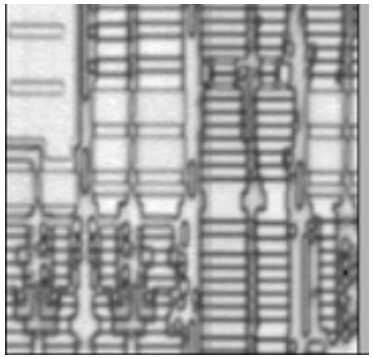
Dark-field image

Bright-field



Spot size ~ defect size
Collecting reflected light

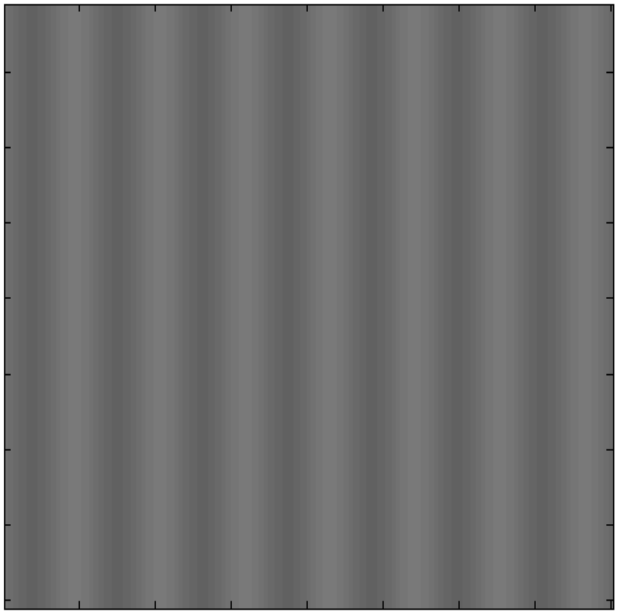
Resolution determines detection



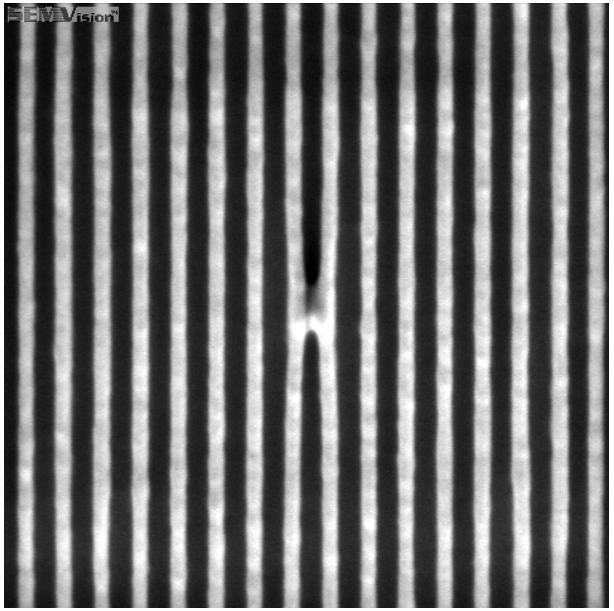
Bright-field image

E-Beam Inspection for Physical Defects

193nm; 60nm l/s simulation



SEM image; 4x nm



- No inherent sensitivity limitation for Electron-Beam technology
- Available solutions have limited throughput

Smallest defect: limited only by good engineering

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Summary Comments

- Moore's Law is expected to continue; for leading MPU/HP Logic makers, 0.7X scaling is expected to occur every two years, with < 10nm node to be in production at approximately Year 2017
- Multiple Lithography options are being developed to support scaling to <10nm node,
- New device structures, new materials, and manufacturable unit processes need to be developed to support the scaling to <10nm node

External Use

think it. apply it.™

APPLIED MATERIALS.