IBM Research

Nanotechnology Trends in Nonvolatile Memory Devices

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The Elusive Universal Memory

CMP EETIMES ONLINE

EE Times: Semi News

'Universal' memory market to hit $75 billion in 2019, says iSuppli

Peter Clarke
(07/27/2005 7:45 AM EDT)
URL: http://www.eetimes.com/showArticle.jhtml?articleID=166402857

LONDON — The market for a memory integrated circuit that combines the speed of SRAM, the density of DRAM and the non-volatility of flash, could be $76.3 billion by 2019, according to market research company iSuppli Corp. (El Segundo, Calif.).

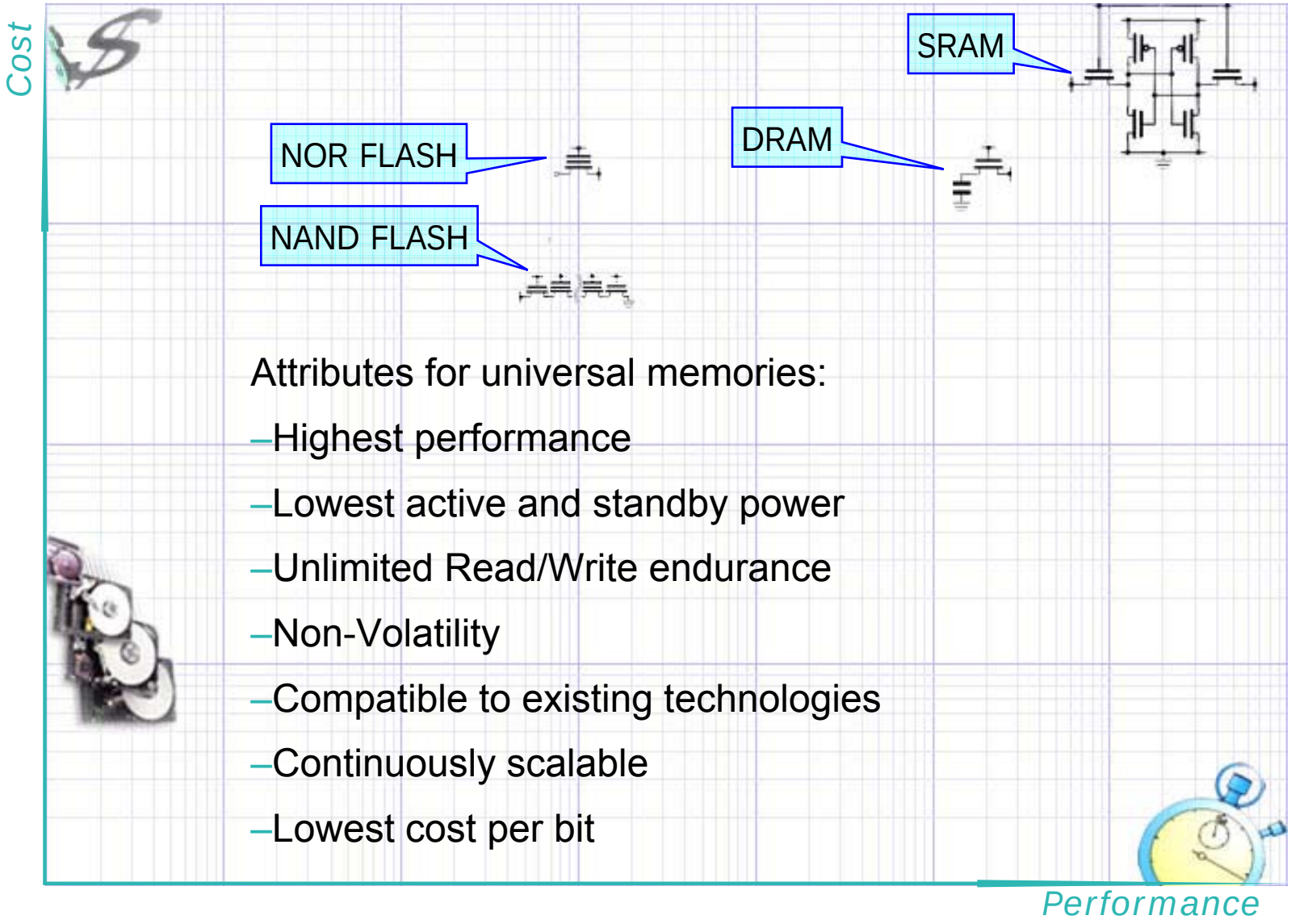
The so-called "universal" memory would, by then, have grabbed about 80 percent of the market, the market researcher has estimated in a long-range forecast it described as "speculative."

There is no single semiconductor memory technology today that has all the desired attributes, which on top of speed, density and non-volatility include: low-cost of manufacture, low switching energy and scalability to nanometer-scale dimension.

Products in various stages of commercialization that include at least some of the attributes include: Ovonic Unified Memory (OUM), Magneto-Resistive RAM (MRAM), Ferroelectric RAM (FRAM) and Nanotube RAM (NRAM), iSuppli said. But the rewards for a winning technology are likely to be immense with the memory market set to double from $46.8 billion posted in 2004 to $95.4 billion by 2019, iSuppli said.

The market researcher said that it does not usually forecast markets beyond a five-year horizon. However, due to the emerging status of the universal memory market, a longer-range forecast is required.

Incumbent Semiconductor Memories



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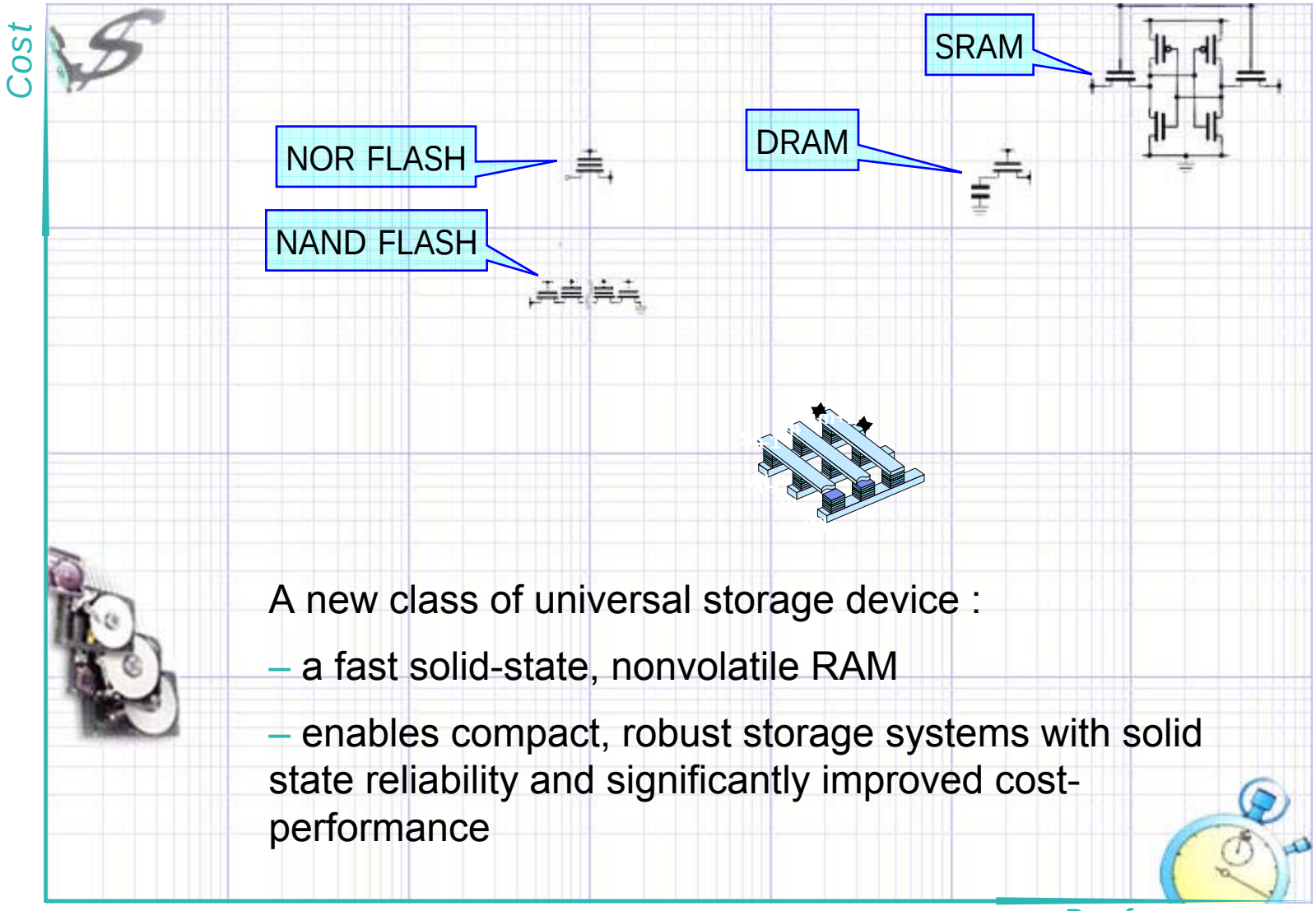
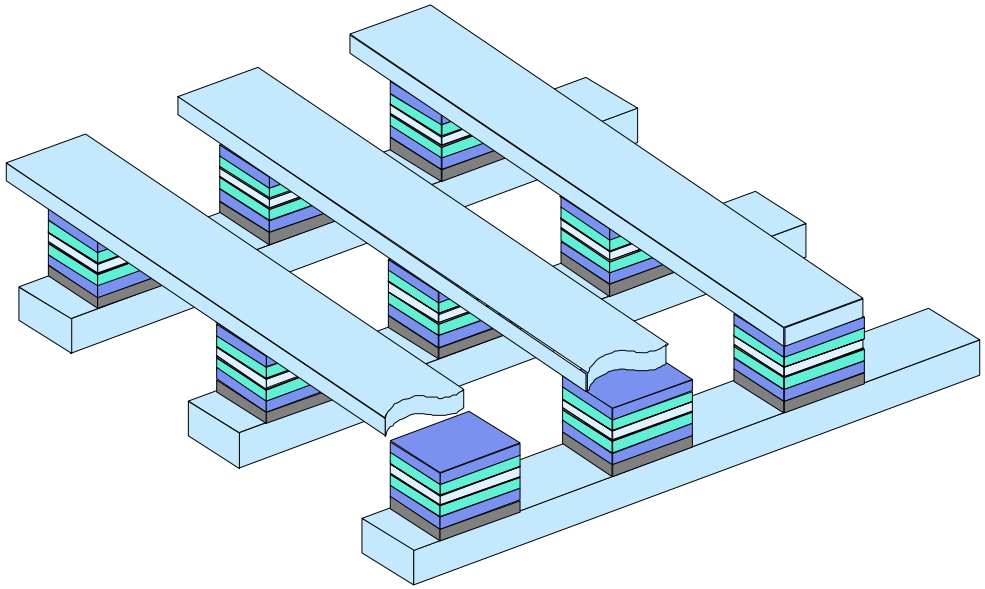


A new class of universal storage device :

– a fast solid-state, nonvolatile RAM

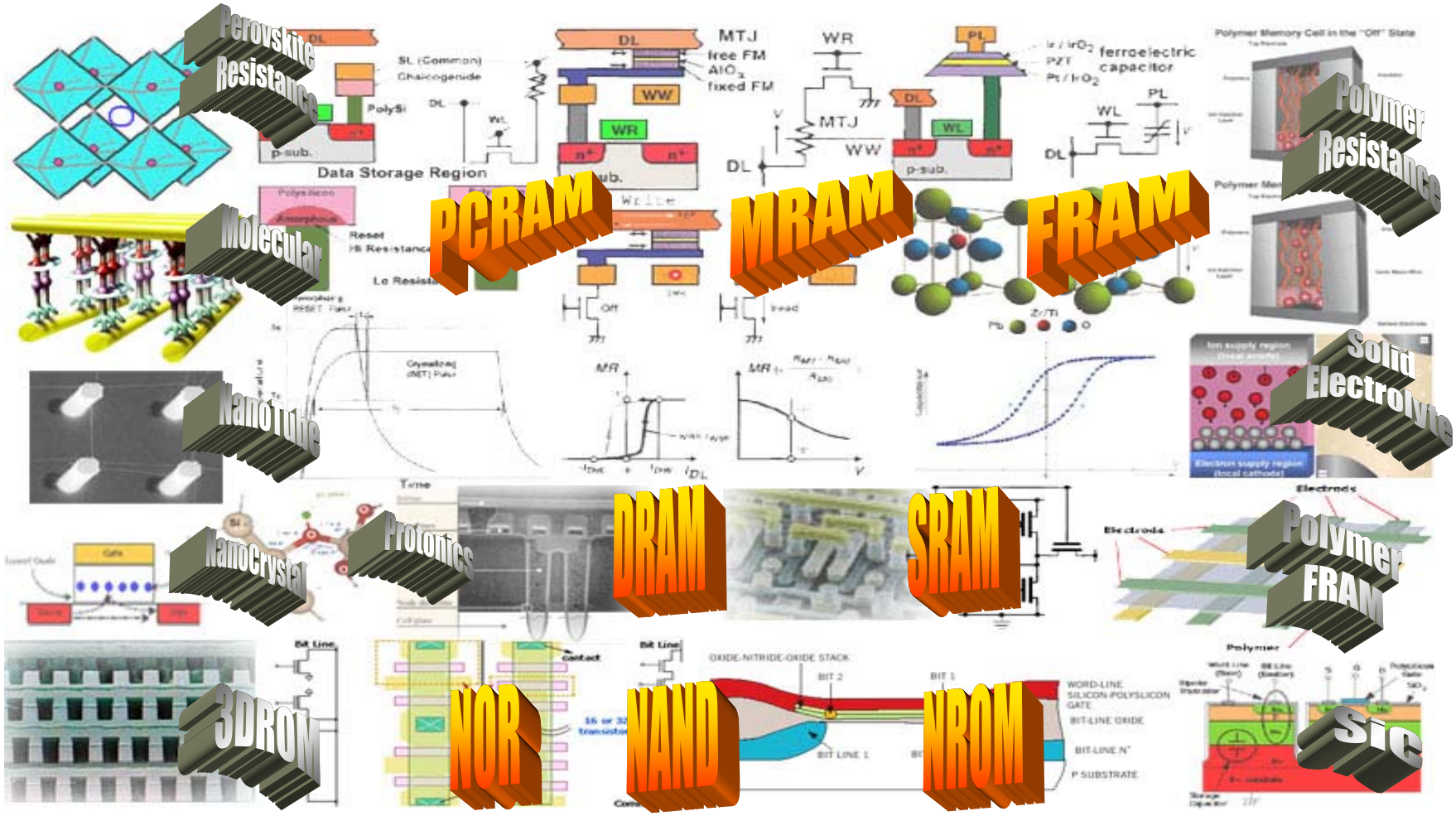
– enables compact, robust storage systems with solid state reliability and significantly improved cost-performance

Non-volatile, universal semiconductor memory

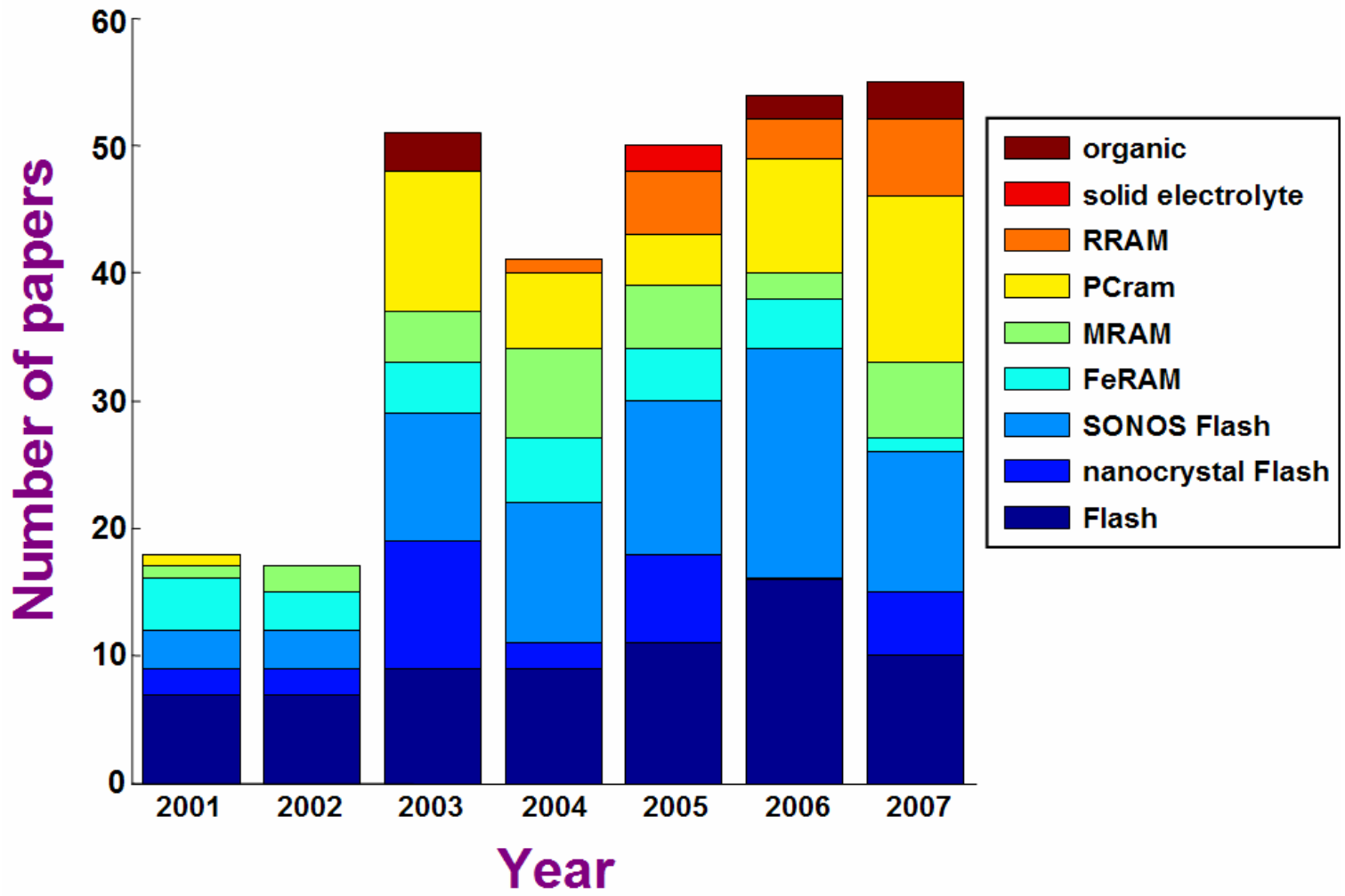


- Everyone is looking for a dense (cheap) crosspoint memory.
- It is relatively easy to identify materials that show bistable hysteretic behavior (easily distinguishable, stable on/off states).

The Memory Landscape



Histogram of Memory Papers



Papers presented at Symposium on VLSI Technology and IEDM;
Ref.: G. Burr et al., IBM Journal of R&D, Vol.52, No.4/5, July 2008

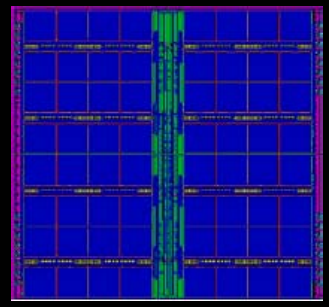
Emerging Memory Technologies

Memory technology remains an active focus area for the industry

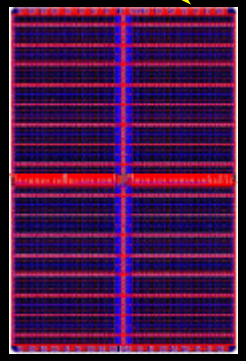
FLASH Extension	FRAM	MRAM	PCRAM	RRAM	PCM - SS Electrolyte	Polymer/ Organic	Mechanical	3D	Thyrister
Trap Storage	Ramtron	IBM	Ovonyx	IBM	Axon	Spansion	Nantero	Matrix	T-RAM
Saifun *NROM*	Fujitsu	Infineon	BAE	Sharp	Adesto	Samsung	STMicro	(Sandisk)	Sony
Tower	STMicro	Freescale	Intel	Unity	Infineon	TFE	Hitachi	3D-ROM	
Spansion	TI	Philips	STMicro	Spansion	Quimonda	MEC		Samsung	
Infineon	Toshiba	STMicro	Samsung	Samsung		Zettacore		Macronix	
Macronix	Infineon	HP	Elpida			Roltronics		Infineon	
Samsung	Samsung	NVE	IBM			Nanolayer			
Toshiba	NEC	Honeywell	Macronix						
Spansion	Hitachi	Toshiba	Infineon						
Macronix	Rohm	NEC	Hitachi						
NEC	HP	Sony	Philips						
Nano-x'tal	Cypress	Fujitsu							
Freescale	Matsushita	Renesas							
Matsushita	Oki	Samsung							
	Hynix	Hynix							
	Celis	TSMC							
	Fujitsu								
	Seiko Epson								

IBM working towards a 16GB part by 2010

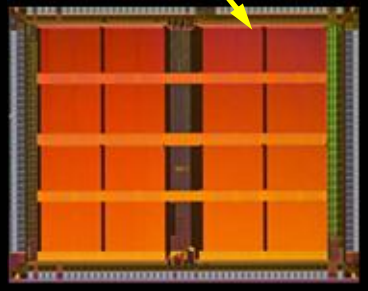
STMicroelectronics is claiming significant progress in the development of a new type of electronic memory that could eventually replace Flash memory technology



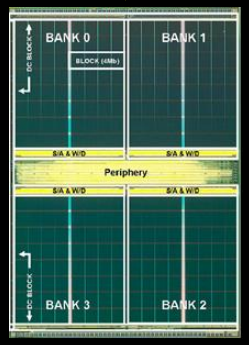
4Mb C-RAM (Product)
0.25um 3.3V



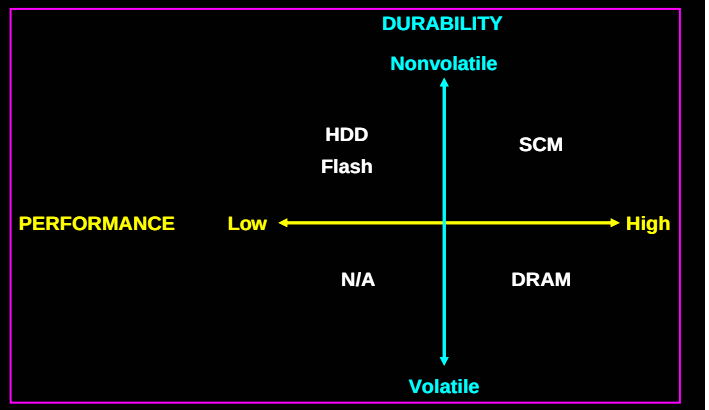
2Mb FRAM (Product)
0.35um 3.3V



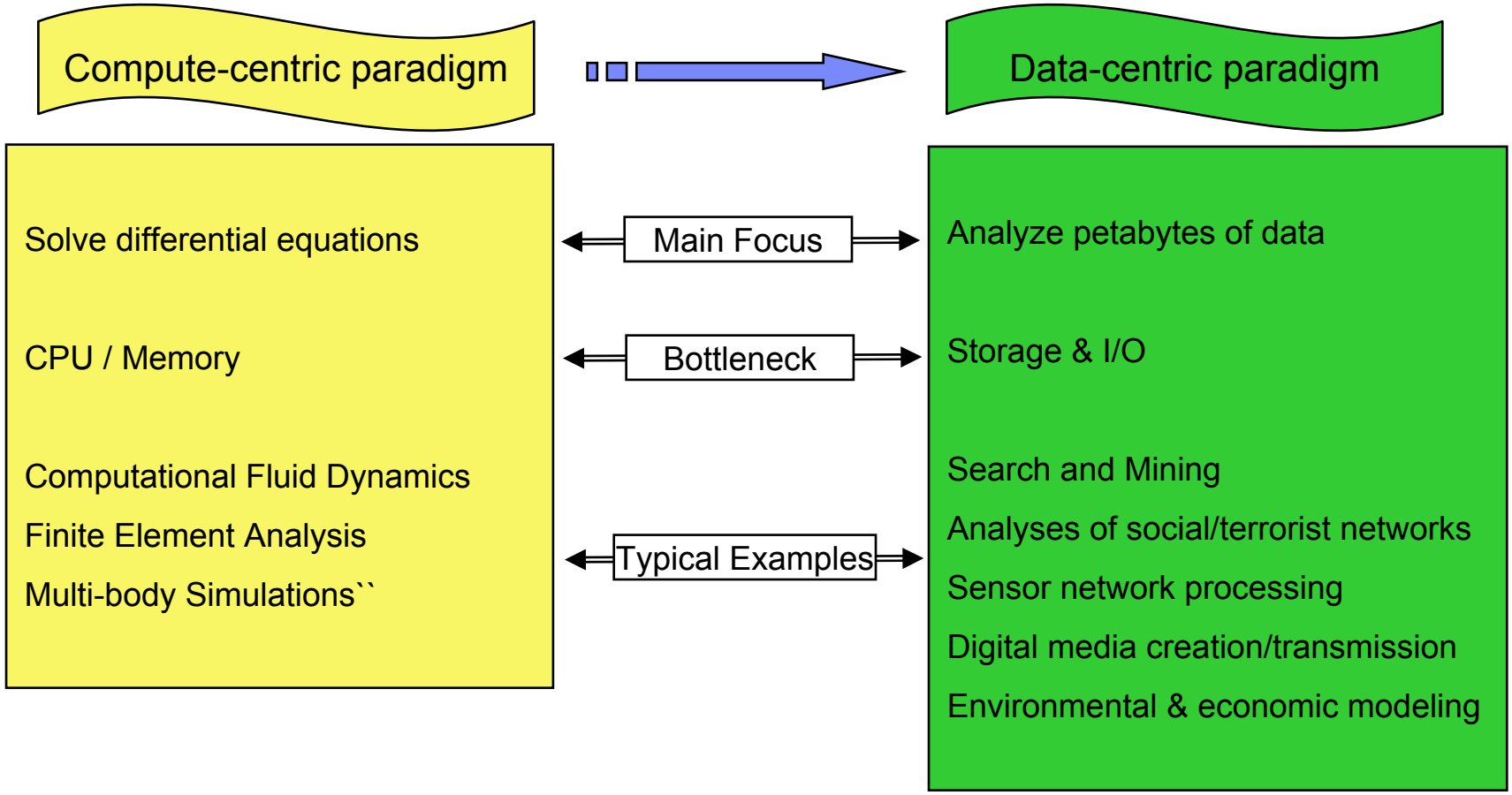
4Mb MRAM (Product)
0.18um 3.3V



512Mb PRAM (Prototype)
0.1um 1.8V



Critical applications are undergoing a paradigm shift



Thesis: *Disks or Flash can't keep up w/data centric applications*
Proposal: *Develop device technology and build a high density array and demonstrate performance and endurance for the data-centric paradigm*

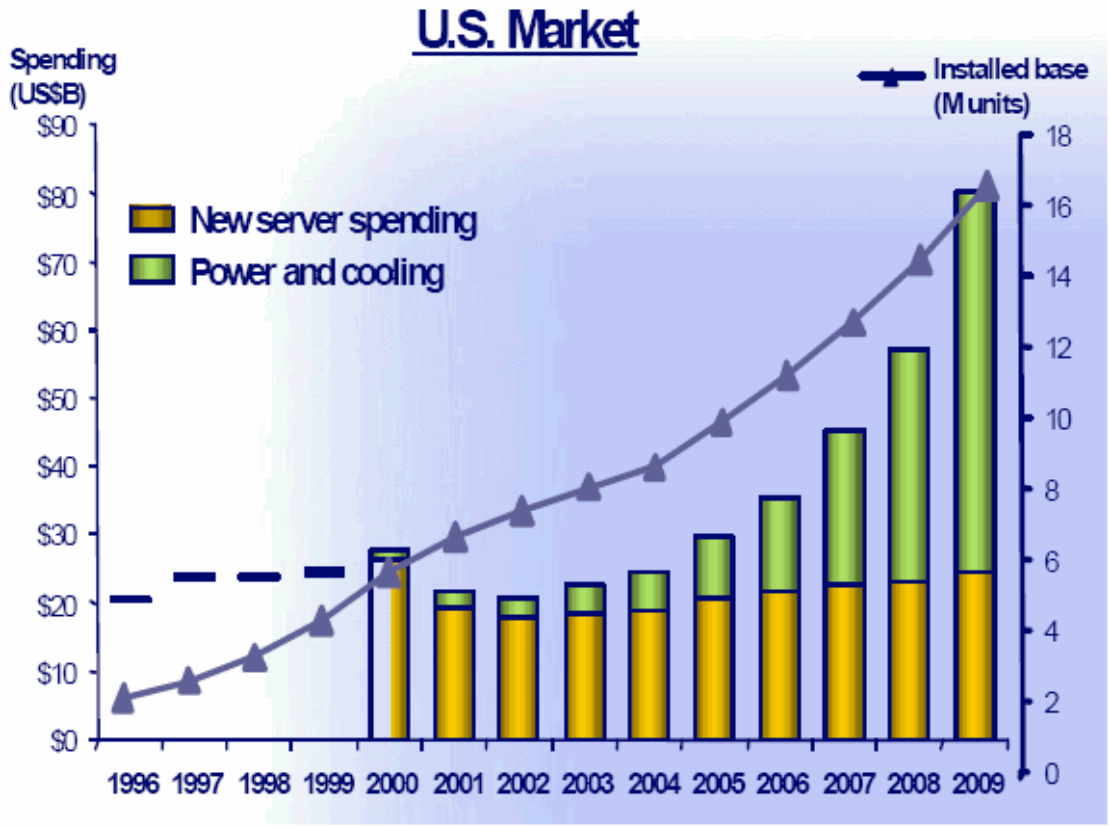
What are the limitations with disks?

- **Bandwidth – Access Time – Reliability - Power**
- **Disk Performance improves very slowly**
  - Gap between processor and disk performance widens rapidly
  - Bandwidth 100MB/s – slow improvement
    - gap can be solved with many parallel disks
    - but need 10,000 disks today, >1,000,000 disks by 2020
      - *but that's just for a traditional high-end HPC system*
      - *data intensive problems are much worse*
  - Access time gap has no good solution
    - disk access times (msec); decrease only 5% per year
    - complex caching or task switching schemes help - sometimes
- **Disk power dissipation is a major factor in data-centric systems (~4W/disk)**
- **Newest disk generations are *less* reliable than older ones**
  - Data losses occur in even the best enterprise-class storage systems

Power & space in the server room

The cache/memory/storage hierarchy is rapidly becoming the **bottleneck for large systems**.

We know how to create MIPS & MFLOPS cheaply and in abundance,
but **feeding them with data** has become
the performance-limiting *and* most-expensive part of a system (in **both $ and Watts**).



Source IDC: 2006, Document # 201722, "The Impact Of Power and Cooling On Data Center Infrastructure", John Humphreys, Jed Scaramella

Extrapolation to 2020

(at 90% CGR → need **1.7 PB/sec**)

- **5.6 million HDD**
  - **19,000** sq. ft. !!
  - **25 Megawatts**

R. Freitas and W. Wilcke, *Storage Class Memory: the next storage system technology* –to appear in "Storage Technologies & Systems" special issue of the IBM Journal of R&D.

What are the limitations with Flash?

- Read/Write Access Times – Write endurance – Block architecture

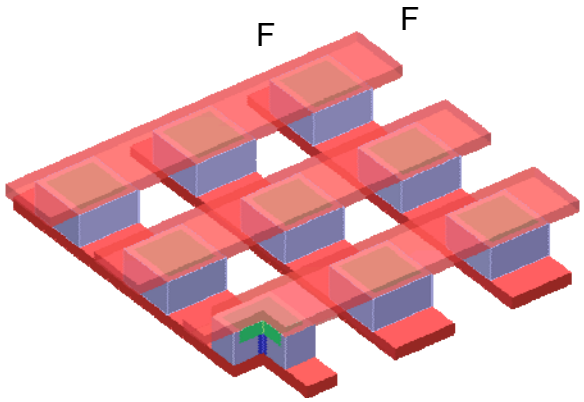
- Flash Performance showing no improvement
  - Gap between processor and Flash performance continues to widen

  - Write endurance $<10^6$ and showing no improvement trends
    - Need $>10^9$ to cater to frequent writes as data continually flows into the system
      - *Tomorrow's hand-held devices will be continuously updated*
      - *Intel applications characterized by continuous data streams*

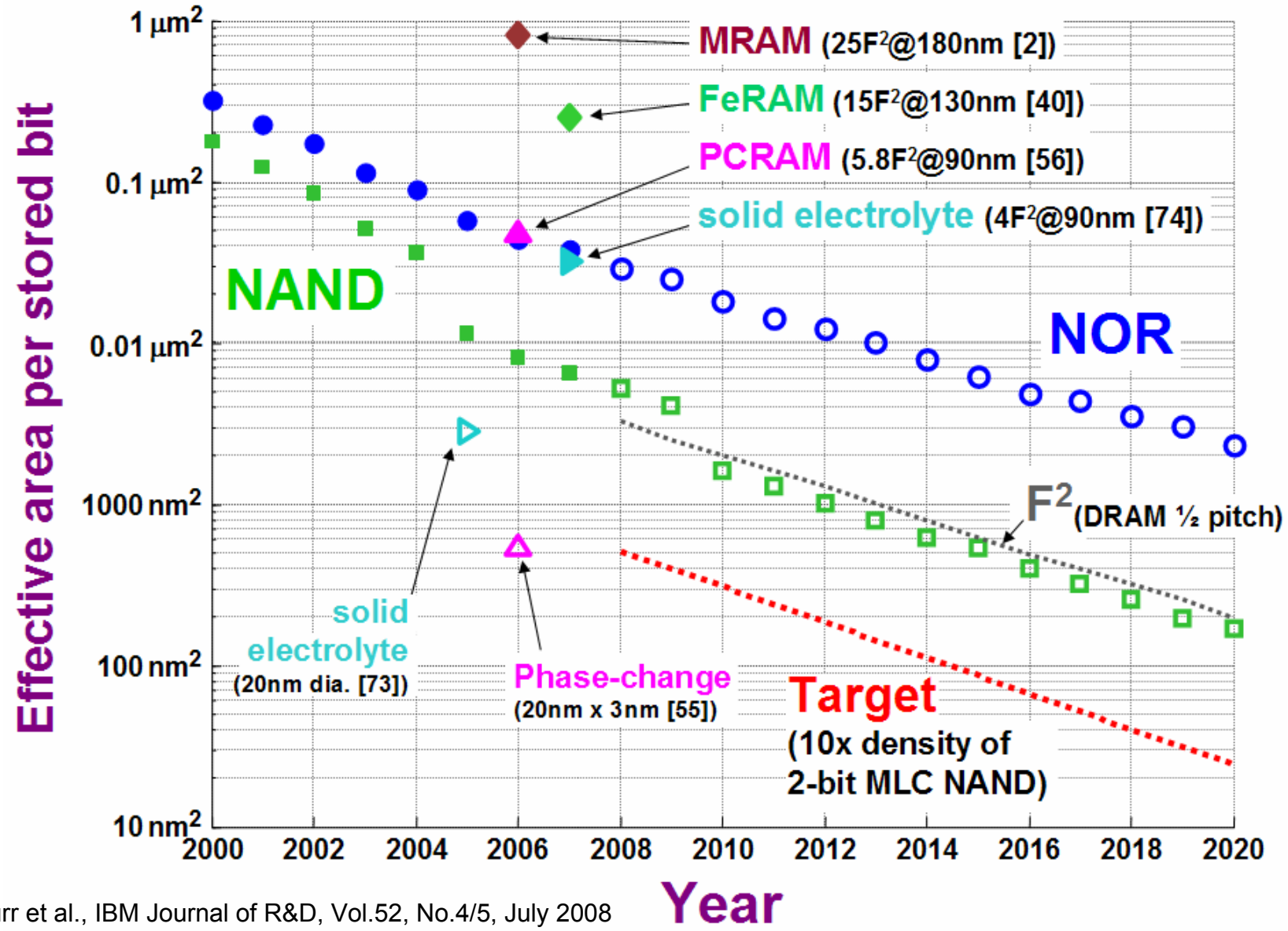
  - Access time gap has no good solution

Processing Cost and F²

- **The bit cell size drives the cost of any memory**
- **Cell area is expressed in units of F² where F is the minimum lithographic feature of the densest process layer**
  - Half pitch dimension of metallization connecting drain and source for ICs
  - MR sensor width in magnetic recording
- **Cell areas**
  - DRAM 8F² ➔ 6F²
  - NAND 4F² ➔ 2F²
  - SRAM 100F²
  - MRAM 15F² -- 40F²
  - Hard Disk 0.5F² ➔ 1F²
  - ….



Density



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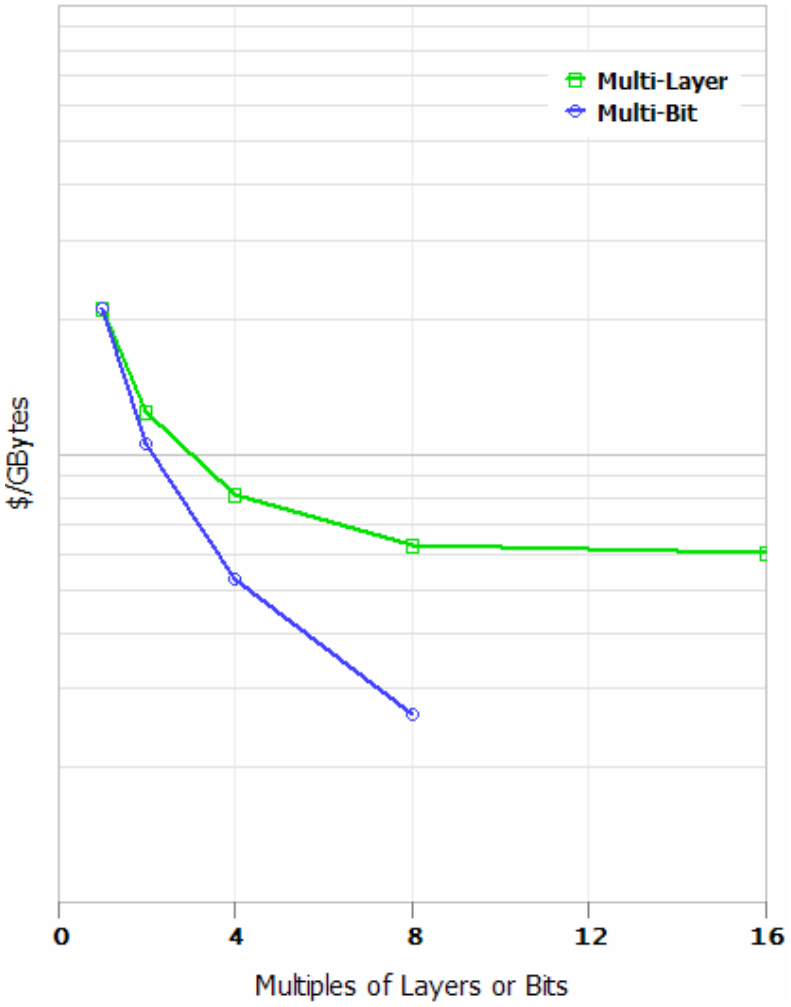
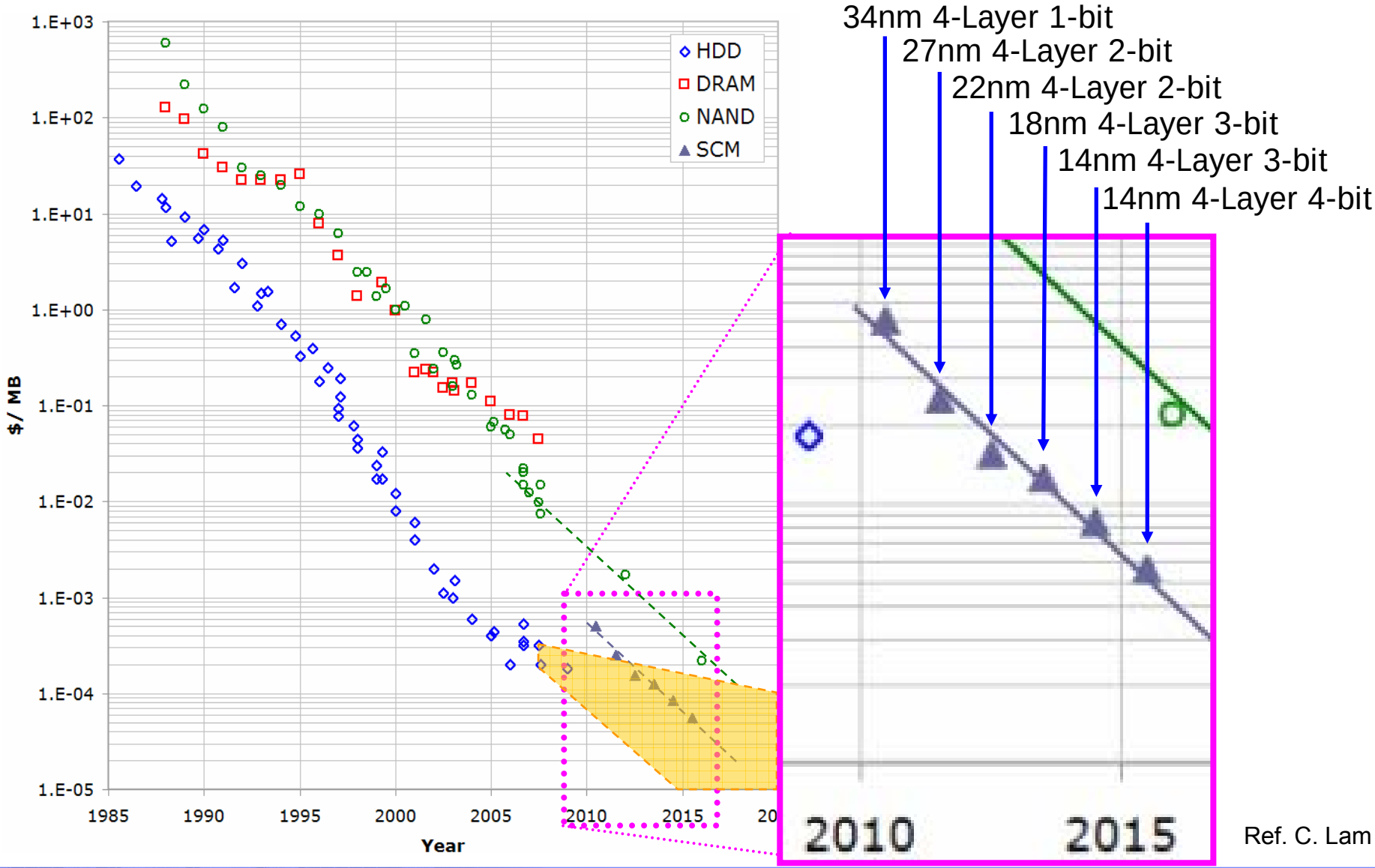
What's next after CD reaching Physical Limit?



- **Beyond the lithographic CD limit, there are 2 ways to continue Moore's Law of Cost Reduction in Semiconductor Memories:**
  - Multi-bit per cell (MLC),
  - Multi-layer stacking (3D).
- **Multi-bits per cell is the more effective way, the combination is most powerful:**
  - 8-layer stack is probably the cost-effective limit for fully integrated stacking,
  - 2 bits per cell is probable with Phase Change Memories,
  - >2 bits would require more innovation.

Storage Historic Price Trend and Forecast



Ref. C. Lam

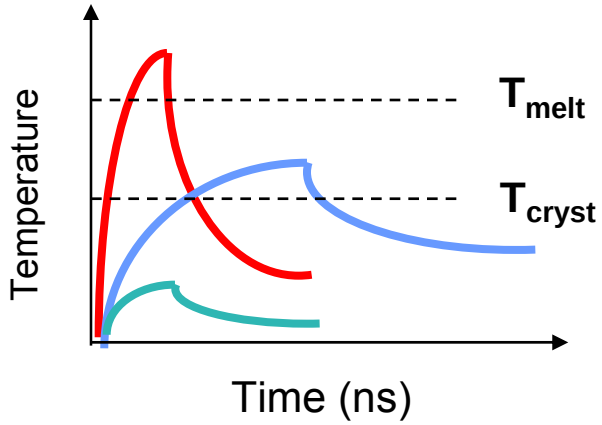
Universal Memory or Storage Class Memory Target Specifications

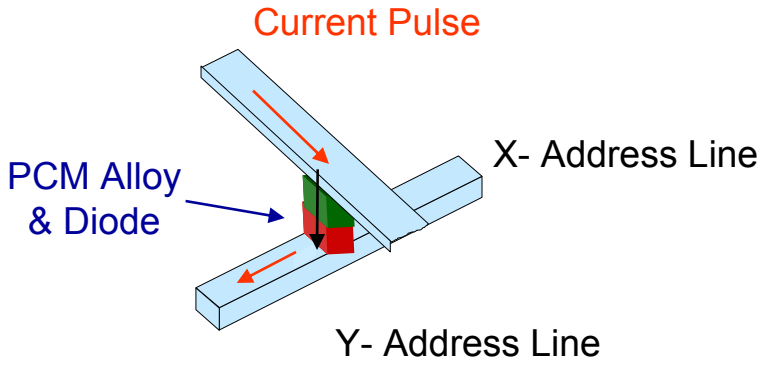
Access Time	**~100-200 ns**
Data Rate (MB/s)	**100**
Endurance	**10^9 - 10^{12}**
HER (/TB)	**10^{-4}**
MTBF (MH)	**2**
On Power (mW)	**100**
Standby (mW)	**1**
Cost ($/GB)	**<5.5**
CGR	**35%**

Very challenging to achieve in combination

SCM Basic Concepts: Phase Change Example

- **Using a phase transition of a *Ge-Sb-Te alloy to store a bit***
- ***Ge-Sb-Te* exists in a stable amorphous and a stable crystalline phase**
  - Phases have very different electrical resistances
- **Transition between phases by controlled heating/cooling**
  - Write '1' : short (10ns) intense current pulse melts alloy crystal => amorphous
  - Write '0' : longer (50ns) weaker current pulse re-crystalizes alloy => crystalline
  - Read : short weak pulse senses resistance, but doesn't change phase
- **Issue: rectifying diode materials for high-ON current density (> 10^7 A/cm^2 – needed for PCM) and ultra-low OFF current density (< 1 A/cm^2).**





A Brief History of Phase Change Memory

1962 A.D. Pearson et al reported switching pheonomena in AsTeI (Advanc. Galss Tech. p357)

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STMicro licensed OUM from Ovonyx and announce Joint Development Project 12/21/2000
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2007 Ovonyx and Qimonda Sign Technology Licensing Agreement for Phase Change Memory 1/16/2007

REVERSIBLE ELECTRICAL SWITCHING PHENOMENA IN DISORDERED STRUCTURES

Stanford R. Ovshinsky
Energy Conversion Devices, Inc., Troy, Michigan
(Received 23 August 1968)

A rapid and reversible transition between a highly resistive and conductive state effected by an electric field, which we have observed in various types of disordered semiconducting material, is described in detail. The switching parameters and chemical composition of a typical material are presented, and microscopic mechanisms for the conduction phenomena are suggested.

We describe here a rapid and reversible transition between a highly resistive and a conductive state effected by an electric field which we have observed in various types of disordered materials, particularly amorphous semiconductors[1,2] covering a wide range of compositions. These include oxide- and boron-based glasses and materials which contain the elements tellurium and/or arsenic combined with other elements such as those of groups III, IV, and VI.

Such amorphous materials can be described as intrinsic semiconductors[3,4] with an optical energy gap E_g typically between 0.6 and 1.4 eV and an activation energy[5] for electrical conduction ΔE between 0.7 and 1.6 eV depending on composition.

ing (in atomic percent) 48 at.% tellurium, 30 at.% arsenic, 12 at.% silicon, and 10 at.% germanium. The specimen was an evaporated film, 5×10^{-5} cm thick, between two carbon electrodes with a contact area of about 10^{-4} cm^2. This material has a resistivity at 300°K of $\rho=2\times10^{7}$ Ω cm, $\Delta E=1.0$ eV, and a positive thermopower.

Figure 1 shows oscilloscope pictures of (a) the I-V characteristic, (b) the voltage V across the unit, and (c) the current I passing through the above unit as a function of time. In this case, a 60-Hz ac voltage was applied across the unit and a 10^4-Ω load resistor was used. The I-V curve is independent of frequency to at least 10^6 Hz.

The major features of the switching phenomena shown are the following: (1) The I-V character-

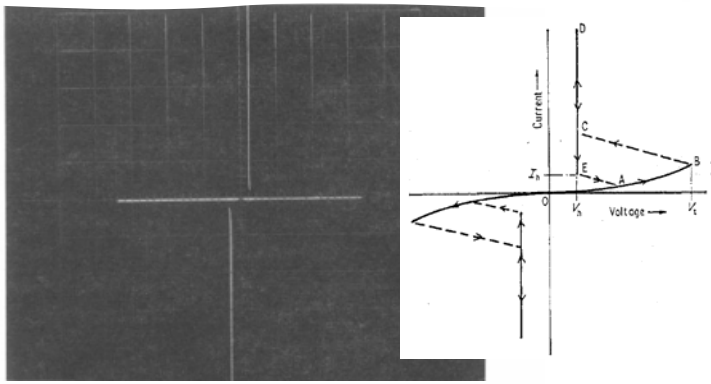

FIG. 1. Response of switching unit to 60-Hz voltage. (a) I-V characteristic: vertical, 2 mA/div; horizontal, 5 V/div. (b) Voltage: vertical, 5 V/div; horizontal, 5 msec/div. (c) Current: vertical, 20 mA/div; horizontal, 5 msec/div.

A Long "Pause"

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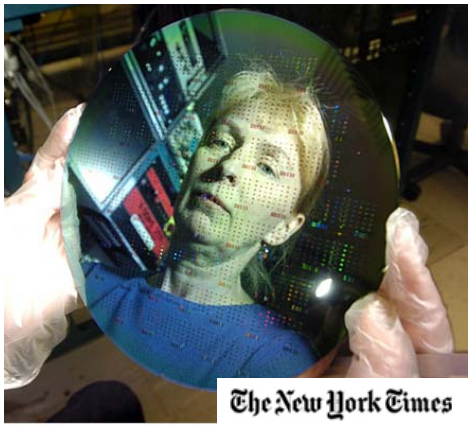
256 bits 25V 7.5mA 15ms, 25V 150mA 6us

Intel, ECD 1970

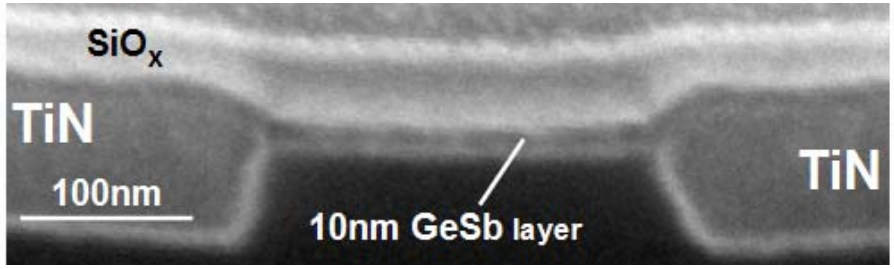
The energy required to melt the Phase Change Memory Element scales with CD ...

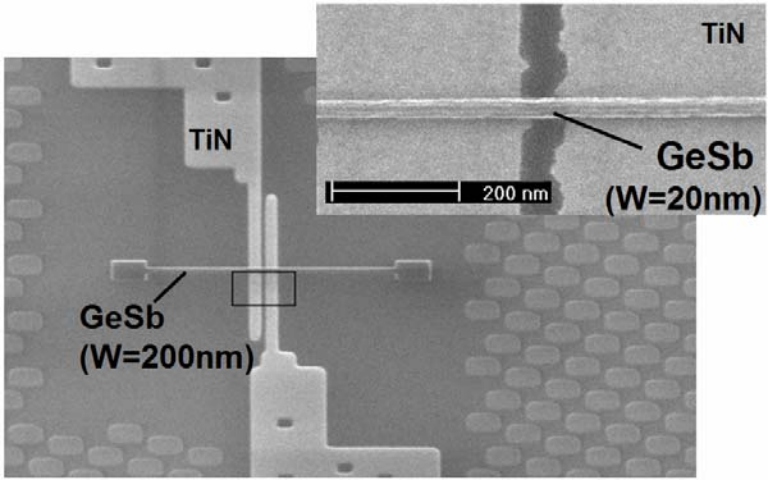
Phase-Change Nano-Bridge

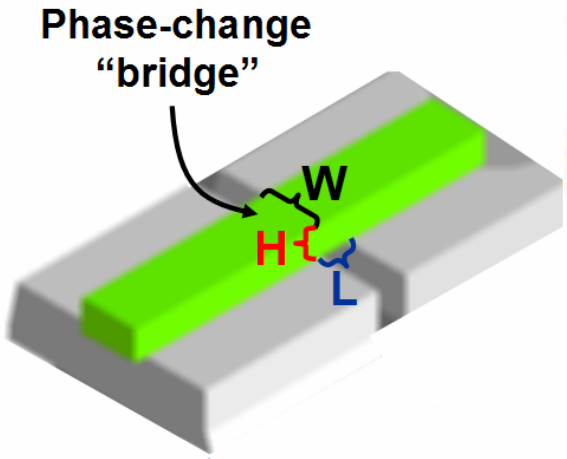
- Prototype memory device with ultra-thin (**3nm**) films demonstrated Dec '06



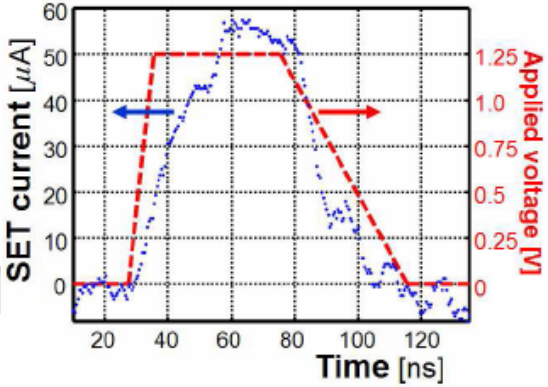
- 3nm * 20nm → 60nm^2
  ≈ Flash roadmap for **2013**
  → **phase-change *scales***
- Fast (<100ns SET)
- Low current (< 100μA RESET)

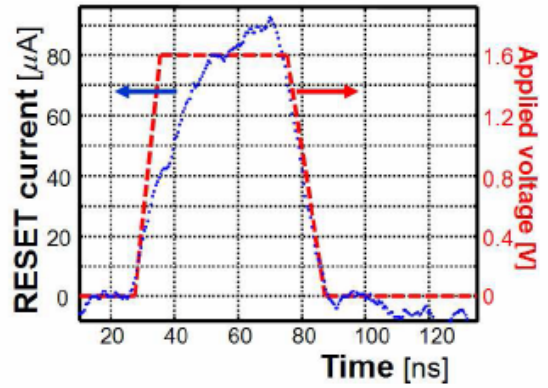




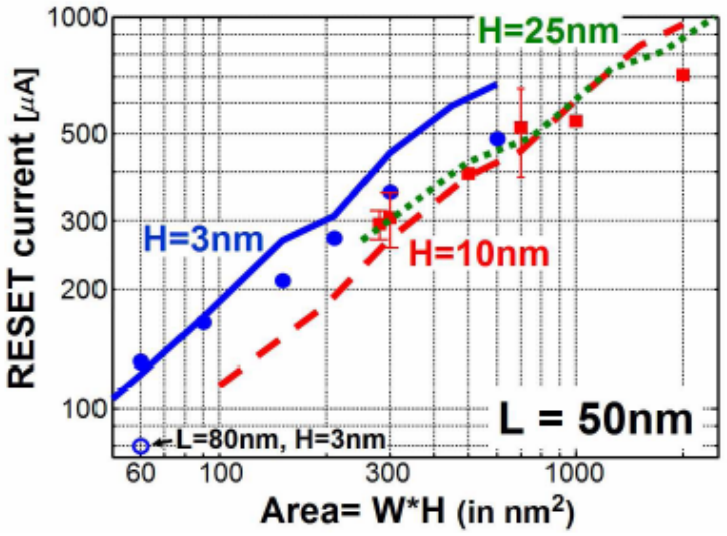


W defined by **lithography**
H by **thin-film deposition**

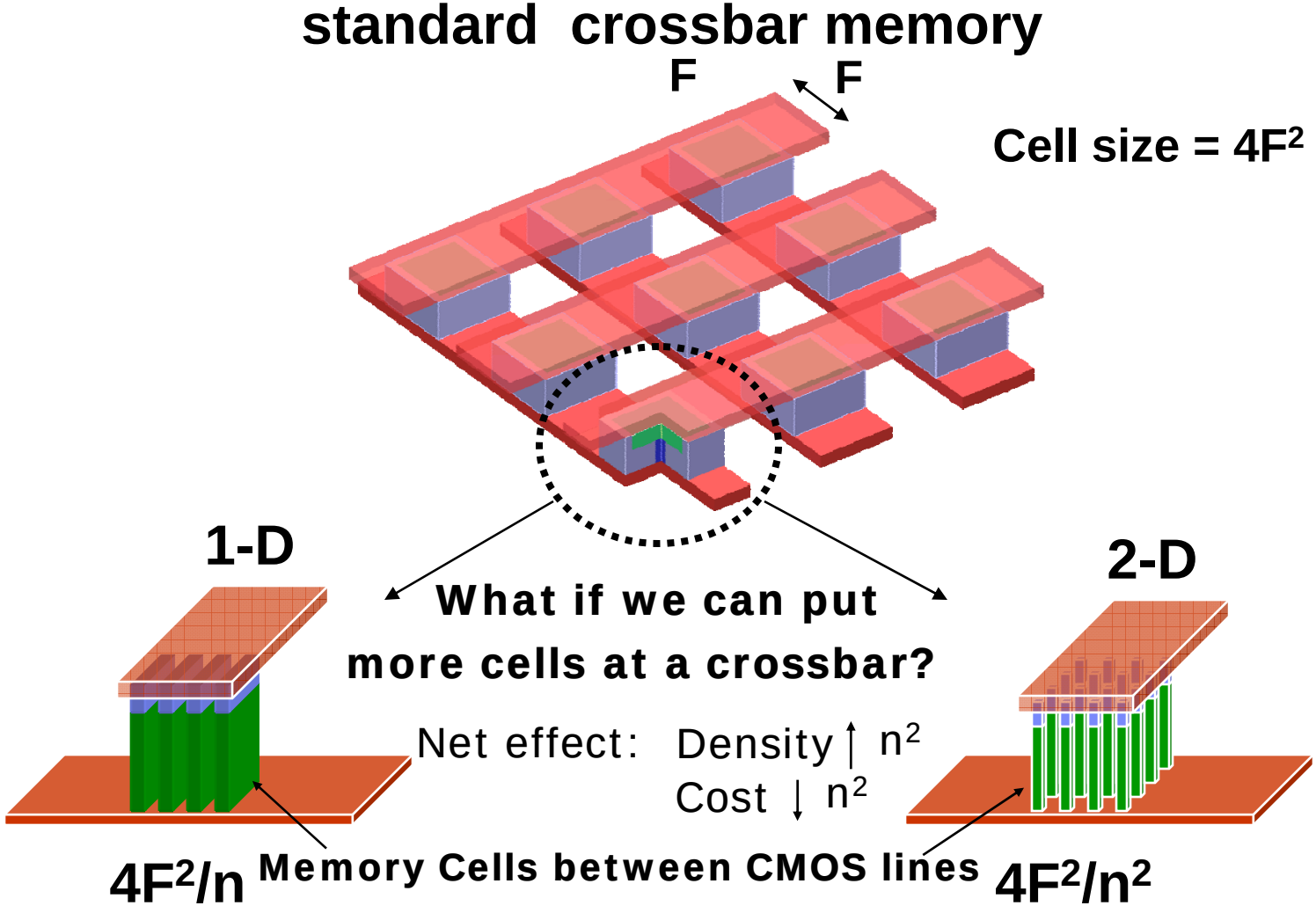




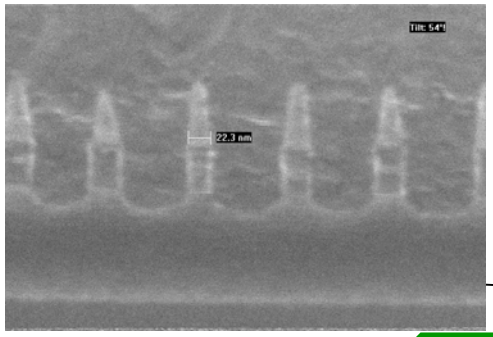
Current scales with area

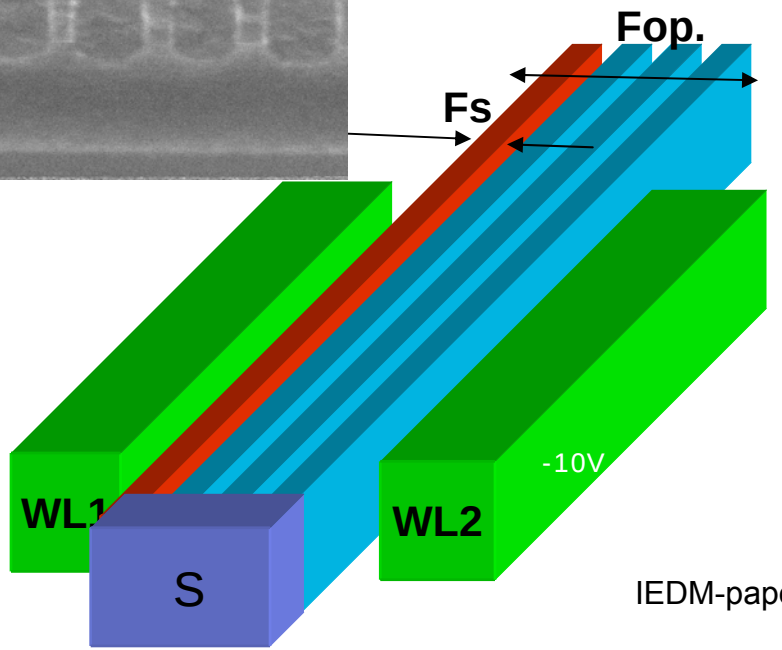


Crossbar Memory Fundamentals

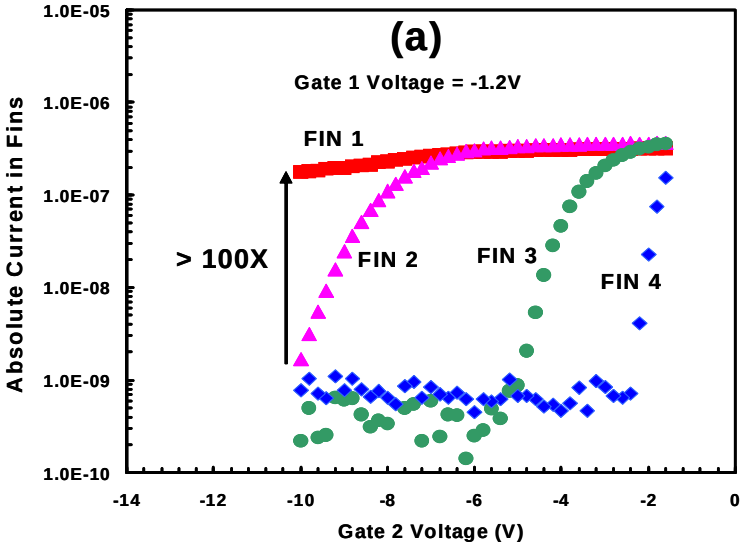


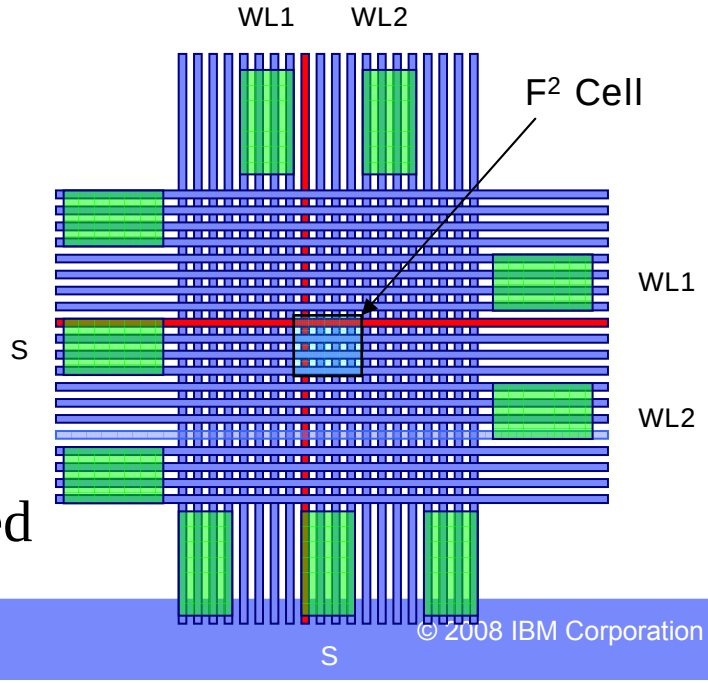
Micro-Nanoscale Decoder





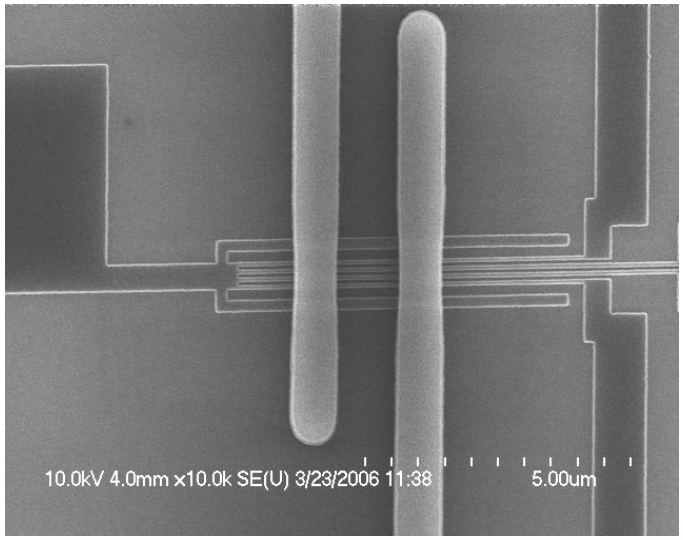
IEDM-paper 2005





- Sub lithographic feature is selected by moving depletion across the fine structure
- Modulating signal is brought in by lithographically defined lines
- Fins down to sub 20 nm have been addressed

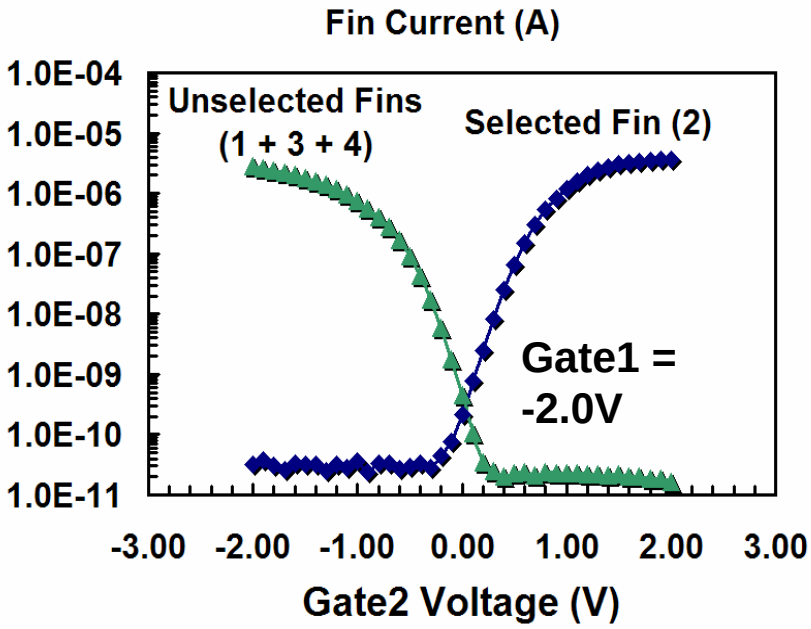
MNAB Concept Demonstrated

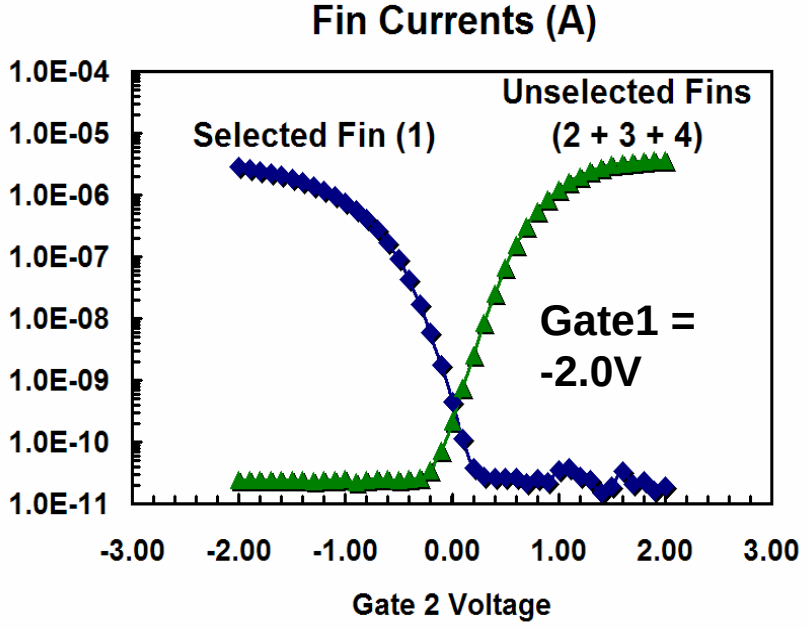


100nm Pitch MNAB Devices Fabricated by E-Beam Lithography

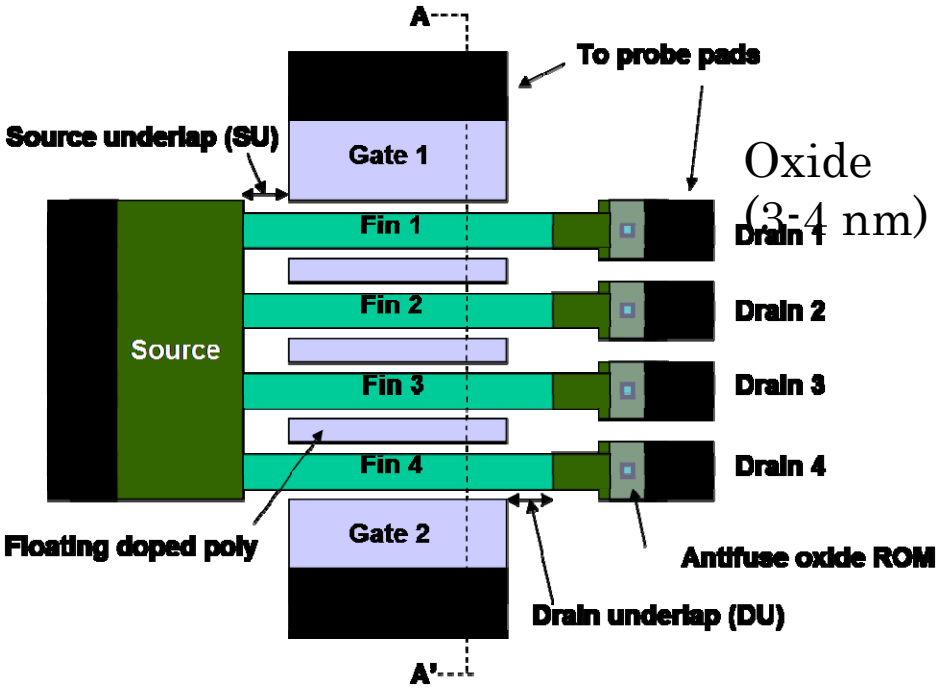
Obtained Fully Functional Devices

Selectivity > 10^5

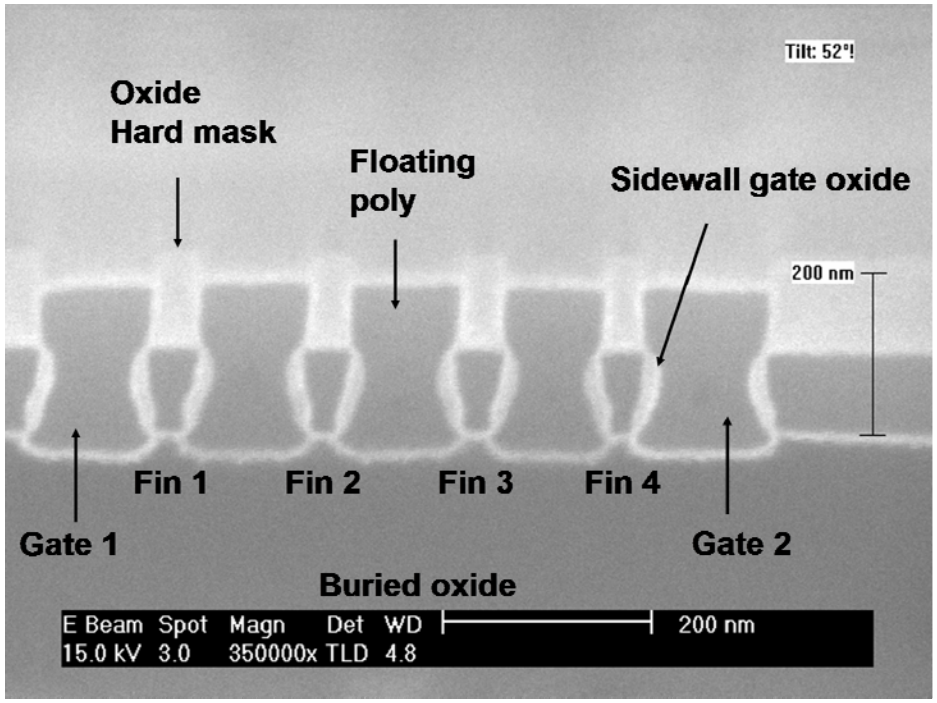




Combining Micro-Nano Decoder and ROM



4-fin UMB+ROM test structure



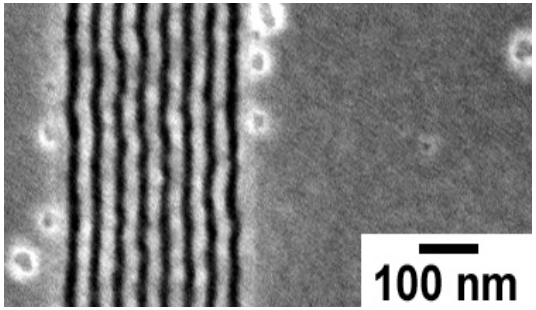
FIB x-SEM through gated fins (A-A')

✓ Successful integration of UMB with memory element
(2 terminal oxide antifuse ROM)

✓ Verified operation over all bit sequences for 4-fin UMB+ROM

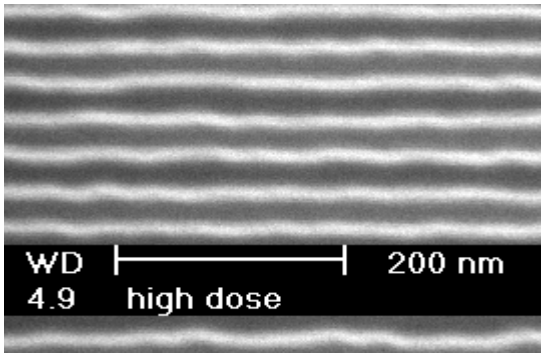
Nanoscale Patterning Techniques

Self Assembly



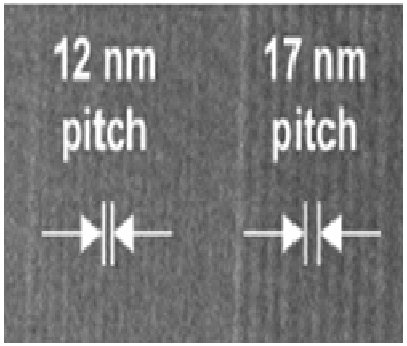
IBM Research

Spacers



Frequency doubling – 40 nm to 20 nm pitch (IBM)

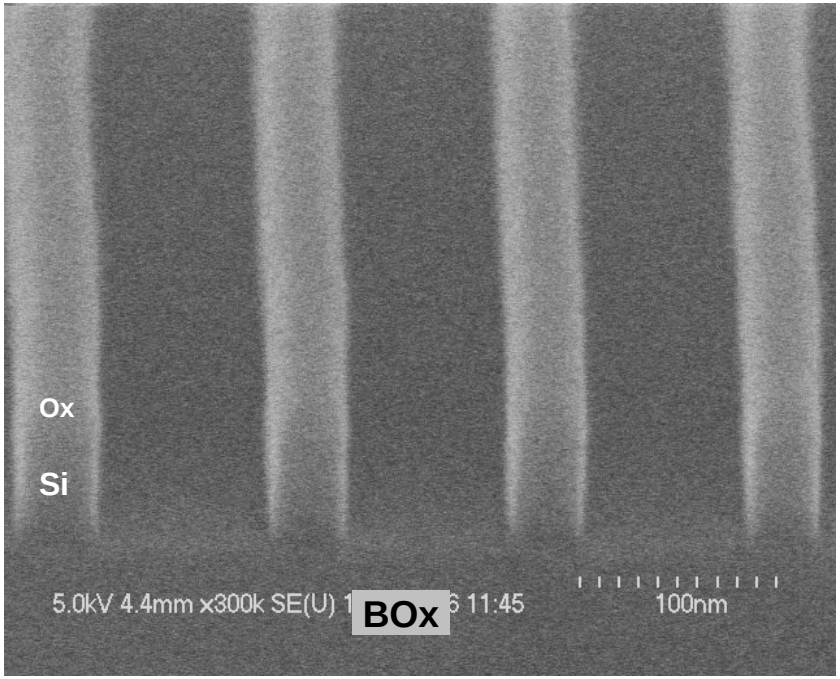
Nanoimprint Lithography



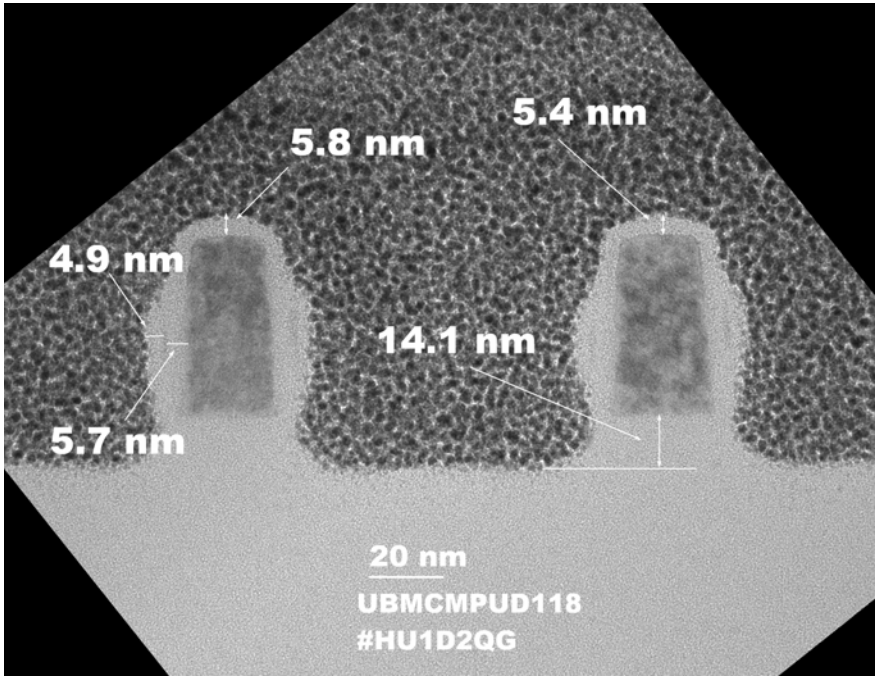
Princeton / Nanonex

- **Litho Tool: 193nm immersion at 1.35 NA, next?**
- **Various nanoscale patterning techniques exist.**
- **Simple regular line / space patterns possible.**

Step-and-Flash Imprint Lithography (SFIL)



Silicon Fins Resulting from Oxide and Imprint Etch Masks



Silicon Fins Ready for Ion-Implant Lithography and Processing

- ✓ **Critical Dimension Control**
- ✓ **Side-Wall Profile**
- ✓ **Line-Edge Roughness**

Mark Hart, et al.

Mix-and-Match Overlay of SFIL to Optical Lithography

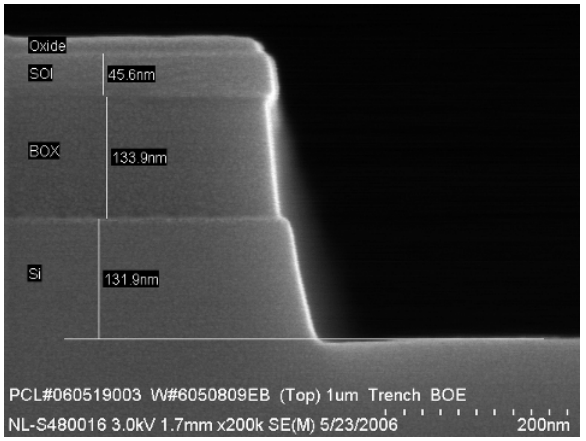
Molecular Imprints

KLA-Tencor

atdf

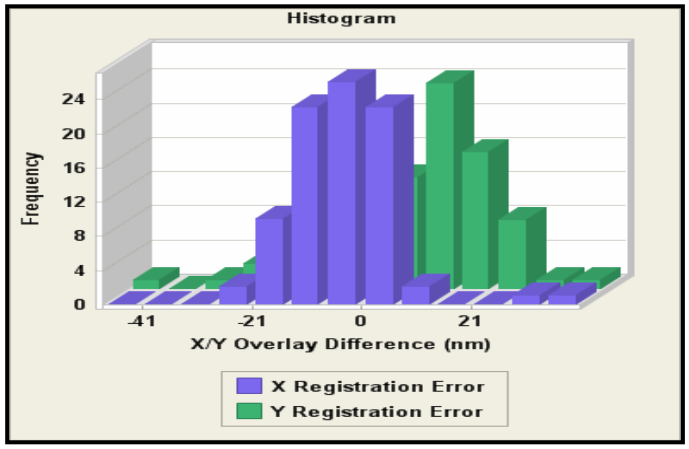
-- To Align Optical Levels with Imprint Level --

Generate "Zero-Level" Marks in Wafer via 193nm Lithography and Etch to Ensure they Survive the Full MNAB Process Build



Align both Imprint Level and Subsequent Optical Levels to These Zero-Level Marks

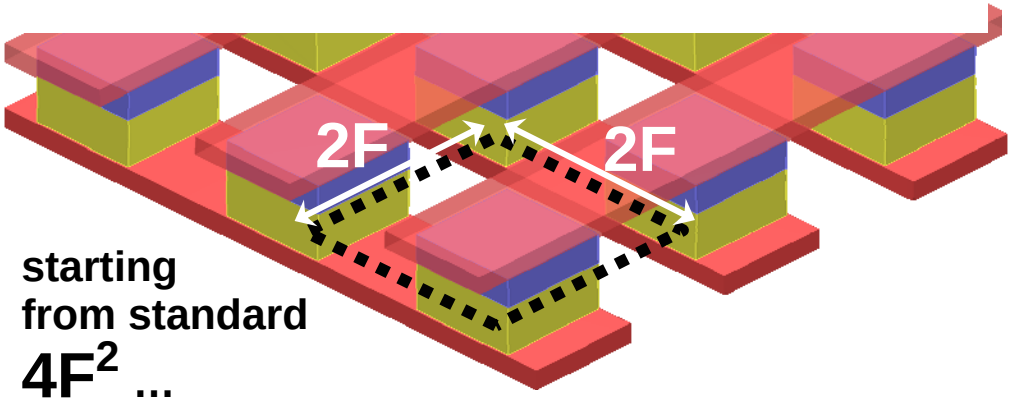
-- Using This Approach --



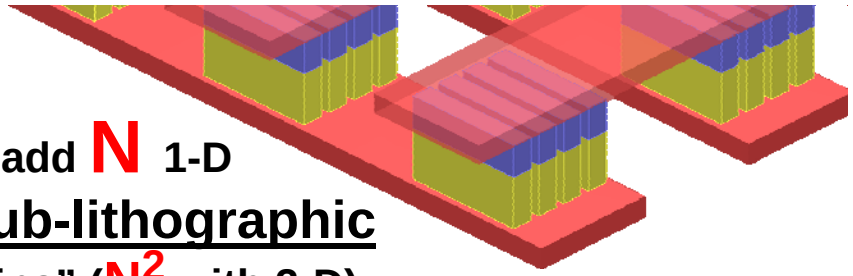
Demonstrated Sub-20nm (Mean+3σ) Overlay Between 193nm Litho Zero-Level and Imprint Over Full 200mm Wafers

Routinely Achieving Sub-50nm Overlay in Approximately 75% of Fields

Paths to ultra-high density me



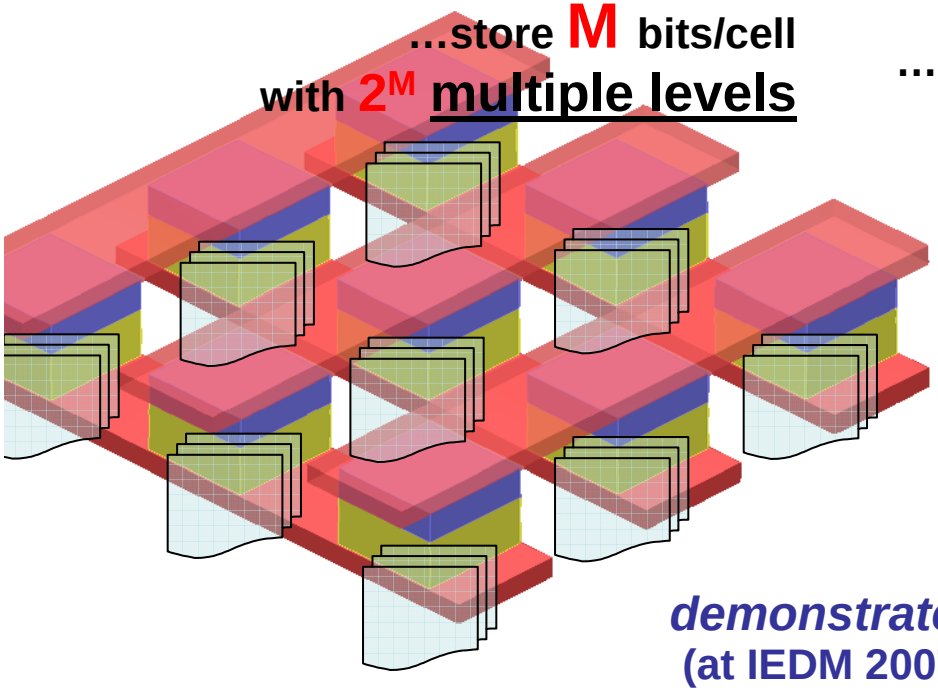
starting
from standard
$4F^2$ ...



...add **N** 1-D
sub-lithographic
"fins" (N^2 with 2-D)

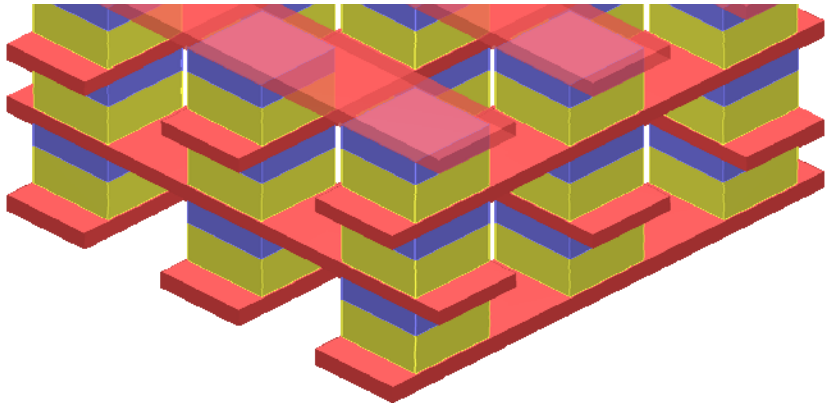
demonstrated
(at IEDM 2005)

...store **M** bits/cell
with 2^M **multiple levels**

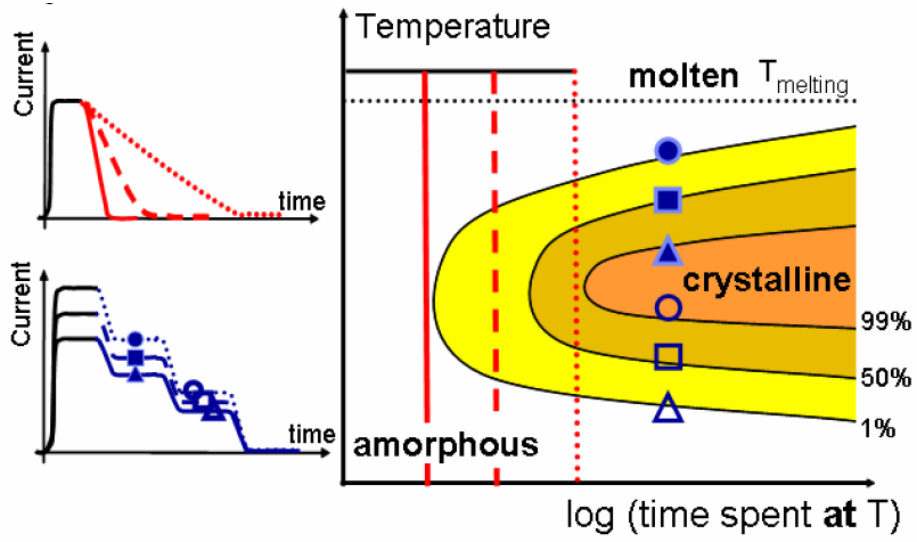


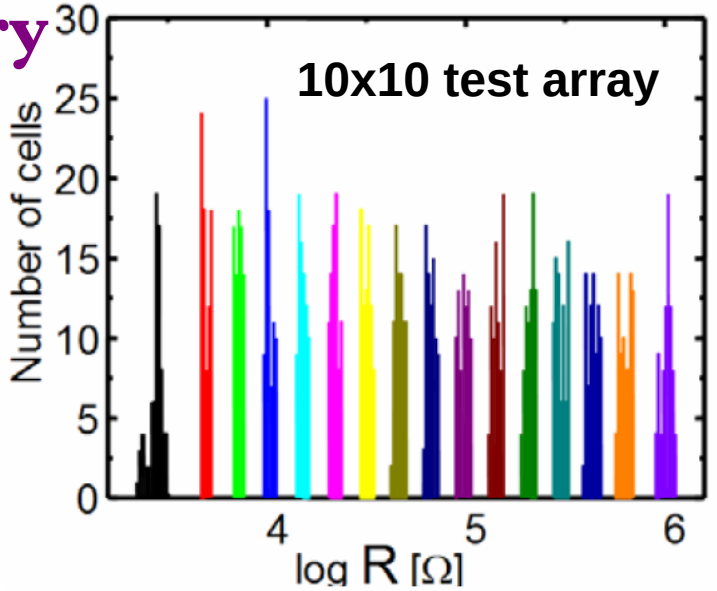
demonstrated
(at IEDM 2007)

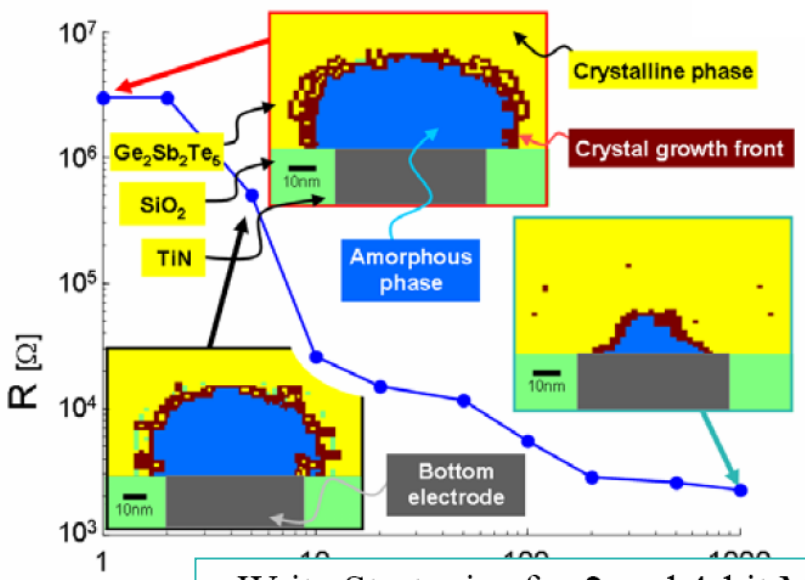
...go to 3-D with
L layers

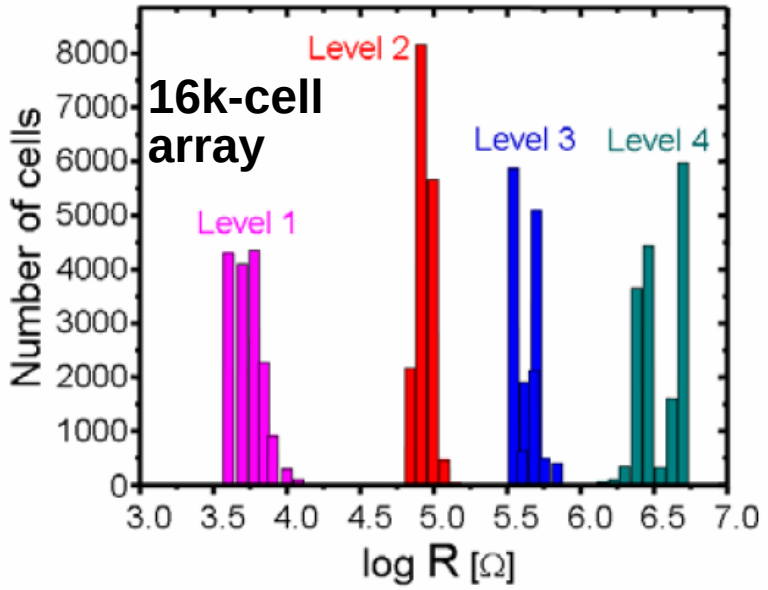


Multi-level phase-change memory









RETURN

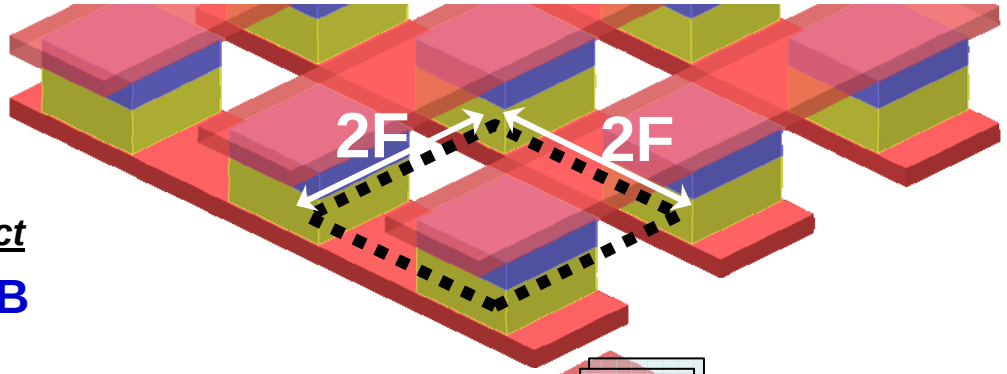
Write Strategies for 2 and 4-bit Multi-Level Phase-Change Memory

T. Nirschl[△], J. B. Philipp[§], T. D. Happ[§], G. W. Burr[‡], B. Rajendran[†], M.-H. Lee[◊], A. Schrott[†], M. Yang[†], M. Breitwisch[†], C.-F. Chen[◊], E. Joseph[†], M. Lamorey[*], R. Cheek[†], S.-H. Chen[◊], S. Zaidi[§], S. Raoux[‡], Y.C. Chen[◊], Y. Zhu[†], R. Bergmann[§], H.-L. Lung[◊], C. Lam[†]
IBM/Qimonda/Macronix PCRAM Joint Project
IBM T.J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, NY, 10598, USA,
[△]Infineon Technologies, [§]Qimonda, [†]IBM Yorktown, [*]IBM Essex Junction, [‡]IBM Almaden, [◊]Macronix International Co. Ltd.

→ **IEDM 2007**

Paths to ultra-high density memory

At the 32nm node in 2013,
MLC NAND Flash
(already M=2 → $2F^2$!)
is projected* to be at…



	density	*product*
2x	**43** Gb/cm² →	**32GB**

if we could shrink $4F^2$ by…

4x	**86** Gb/cm² →	**64GB**

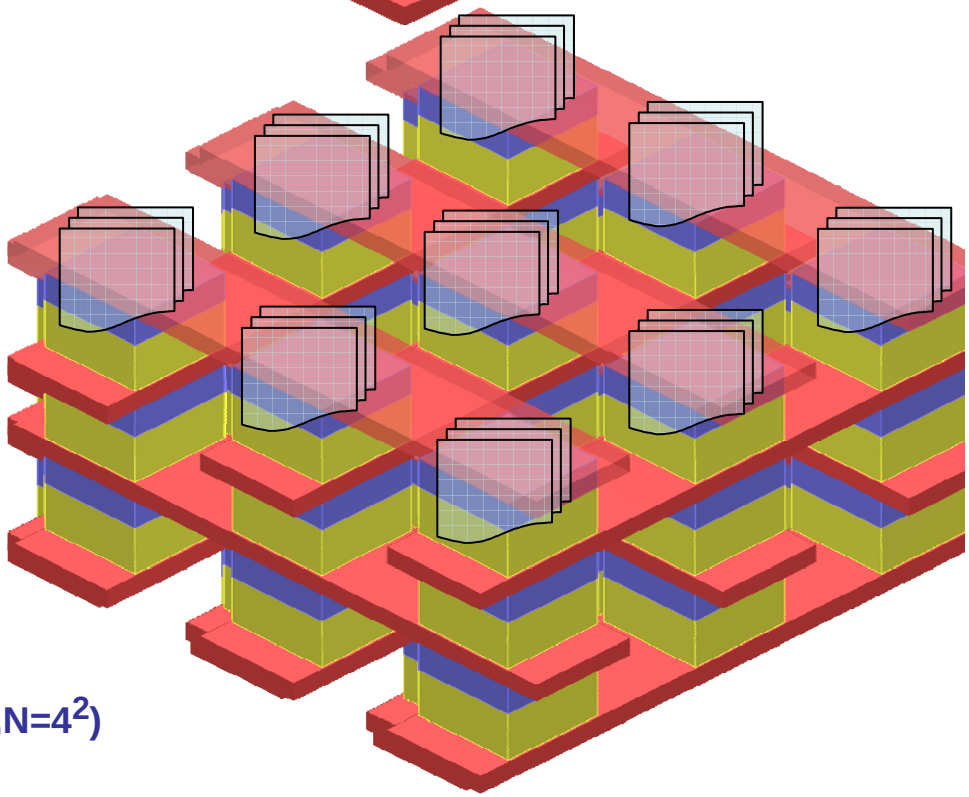
e.g., **4 layers of 3-D** (L=4)

16x	**344** Gb/cm² →	**256GB**

e.g., **8 layers of 3-D,**
2 bits/cell (L=8,M=2)

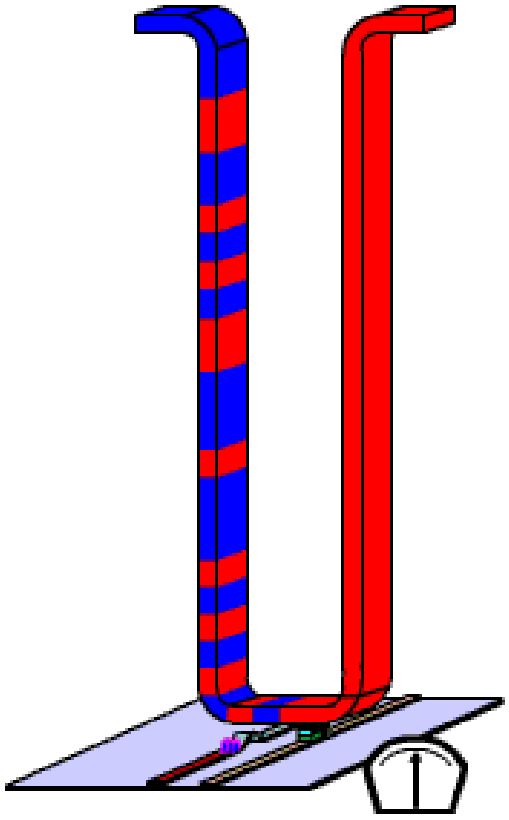
64x	**1376** Gb/cm² →	**~1 TB**

e.g., **4 layers of 3-D,**
4x4 sublithographic (L=4,N=4^2)



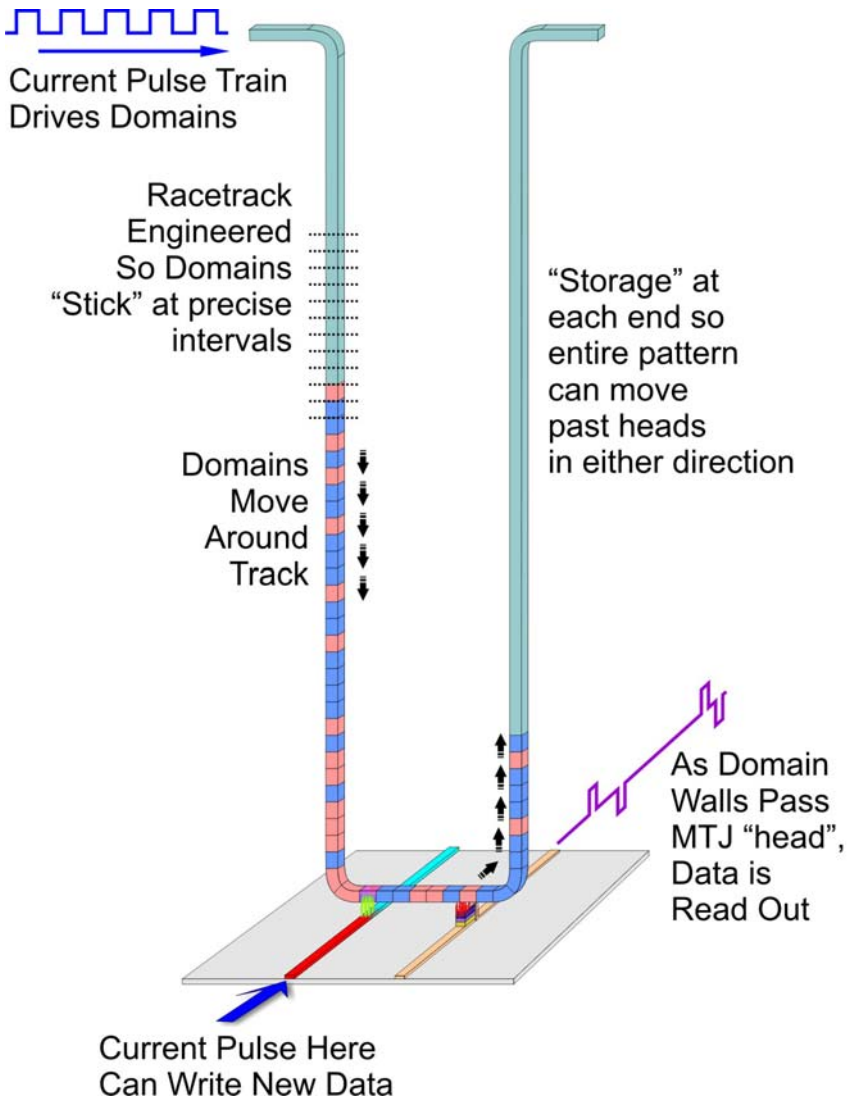
* 2006 ITRS Roadmap

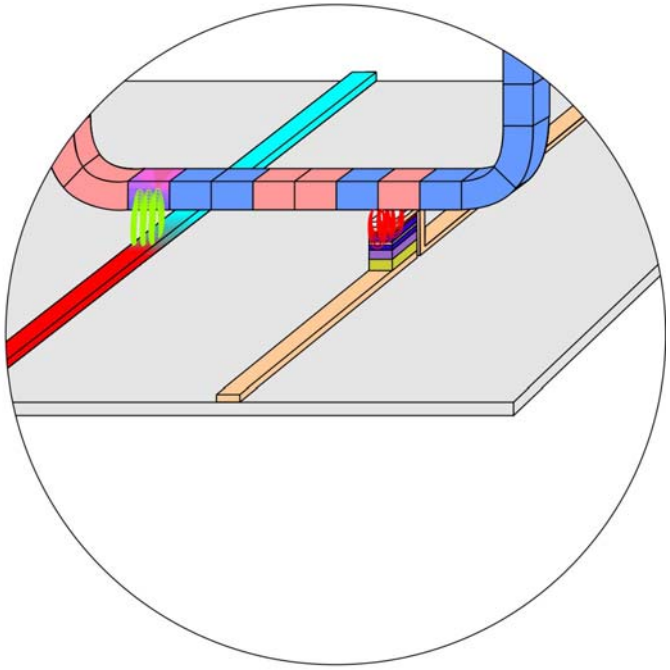
Magnetic Racetrack Memory: a 3-D shift reg. Memory



- Data stored as pattern of domains in long nanowire or "racetrack" of magnetic material.
- Data stored magnetically and is non-volatile.
- Current pulses move domains along racetrack – *no moving parts, just the patterns move.*
- Each memory location stores *an entire bit pattern* (10, 100, 1000 bits?) rather than just a single bit.

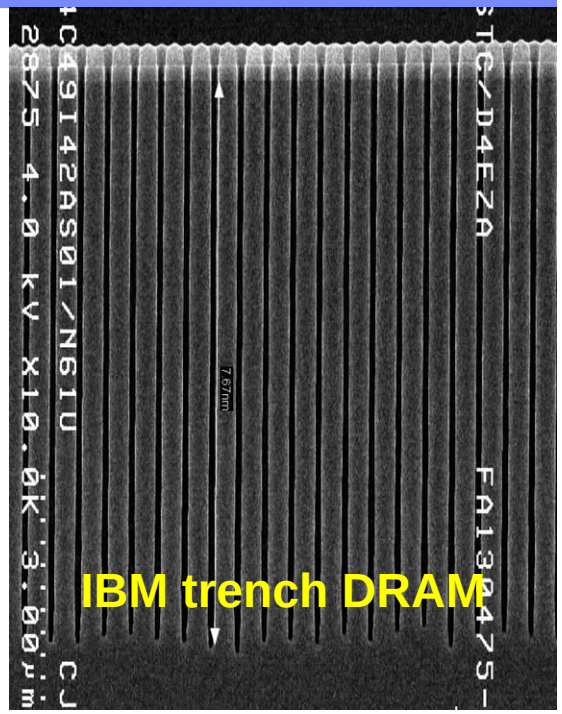
Magnetic Racetrack Memory Concept

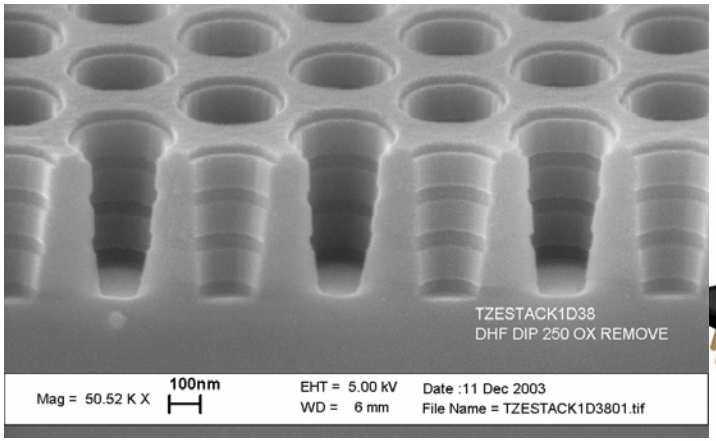


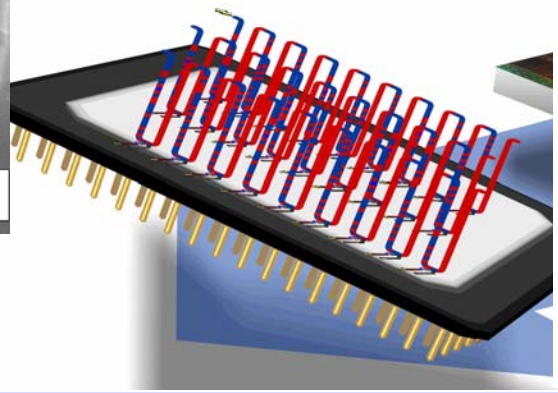


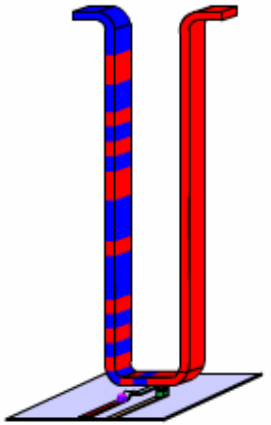
Magnetic Race-Track Memory

- **Information stored as domain walls in vertical "race track"**
  - Data stored in the third dimension in tall columns of magnetic material
- **Domains moved around track using nanosecond pulses of current**
- **10 to 100 times the storage capacity of conventional solid state memory**



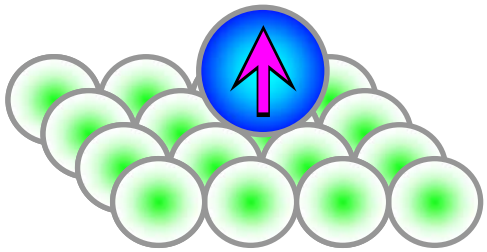






Magnetic Race Track Memory
S. Parkin (IBM), *US patents*
6,834,005 (2004) & 6,898,132 (2005)

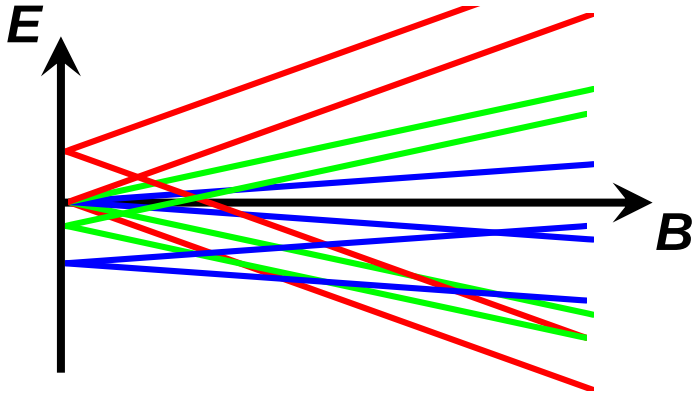
Magnetic anisotropy at a surface



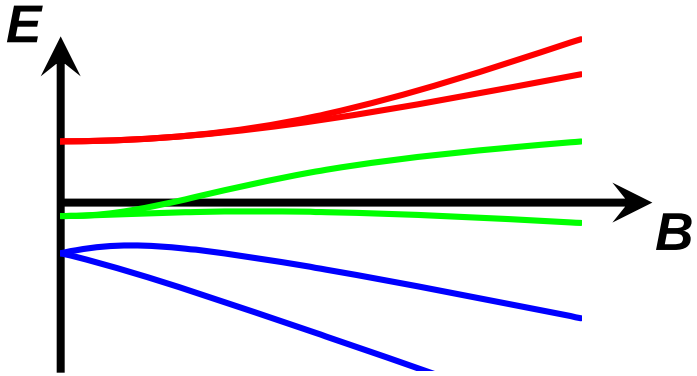
- **Free atomic spin is rotationally invariant: all spin orientations are degenerate.**
- **Loss of rotational symmetry breaks degeneracy of spin orientations.**

$$H = -g\mu_B \vec{B} \cdot \vec{S} + DS_z^2$$

B || z

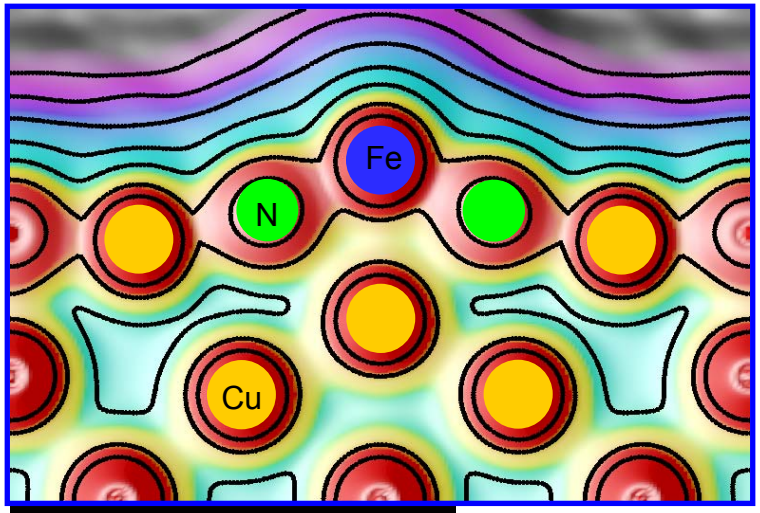


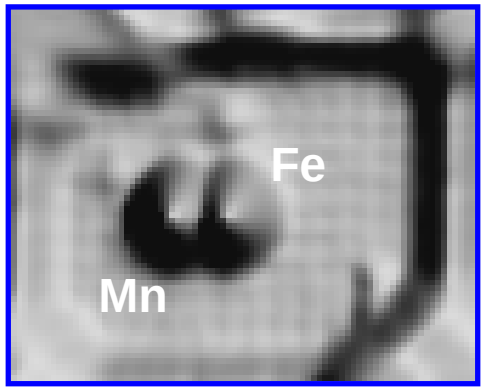
B ⊥ z

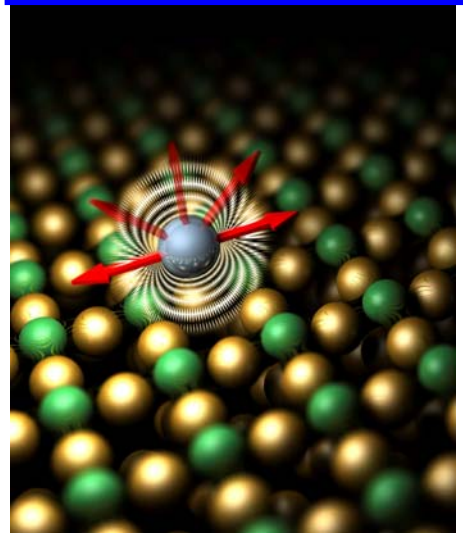


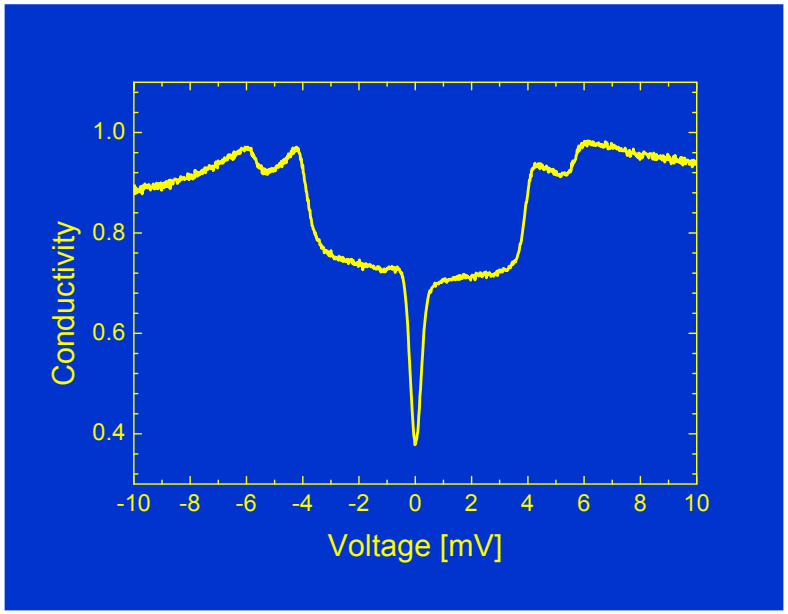
Magnetic field dependence varies with angle of magnetic field.

Future?: Large Magnetic Anisotropy for Single Atom Memory









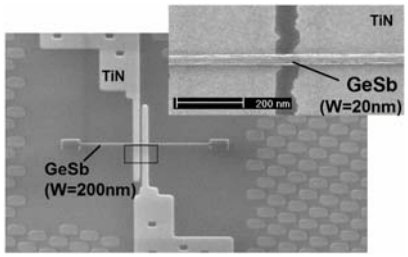
- The energy that is required to change the direction of a single spin on CuN measured .
- Large single-atom magnetic anisotropy for **iron of about 6 meV.**
- About 50x weaker anisotropy for manganese on same surface.
- Spin excitation spectroscopy reveals spin energy levels, including their magnetic field dependence.
- DFT calculations elucidate surface structure and leads to same total spin as experiment.
- **GOAL**: engineer very large magnetic anisotropy to demonstrate data storage.

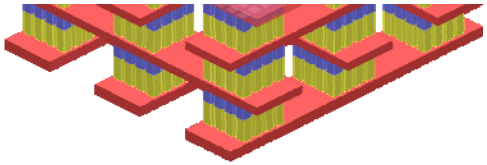
The Future of Memory?

Storage Class Memory:
solid-state non-volatile memory
at hard-drive prices

- **Phase-change memory** – low cost because >1 bit / $4F^2$

~2013?

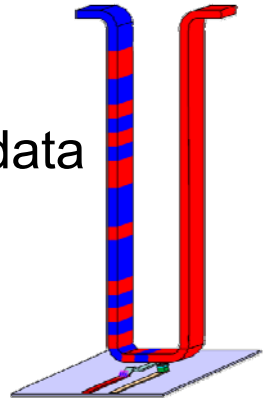




- **Racetrack memory**

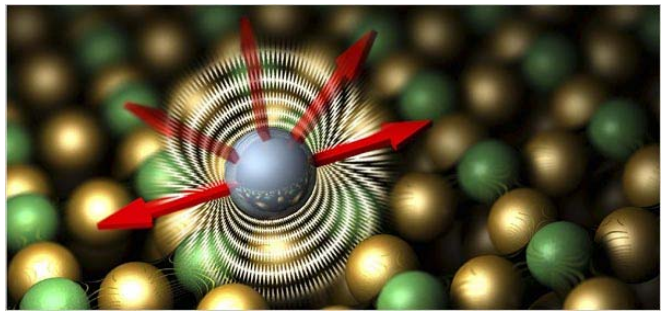
~2018?

– a 3-D nano-warehouse for data



- **Atomic memory** – "there's a lot of room at the bottom…"

~2030?



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Thank you!