

Conductive-bridge Memory (CBRAM[®]) with Excellent High-temperature Retention and Tolerance to High Levels of Gamma Radiation

Dr. Venkatesh P. Gopinath,
V.P. of CBRAM Technology
Adesto Technologies

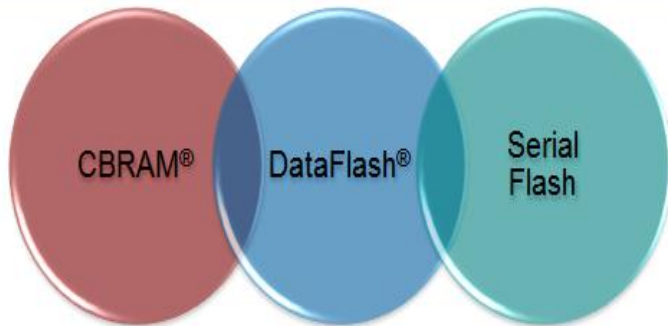


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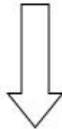
- **Introduction to Adesto Technologies**
- **Introduction to CBRAM**
- **CBRAM from Adesto®**
 - General characteristics
 - High-T retention
 - Radiation tolerance
- **Conclusions**

Adesto Technologies Corporate Overview

Adesto Provides Differentiated Memory Solutions in the Code and Data Storage Markets Using Our Proprietary Technology Platforms



Low Power High Performance Reliable Cost Effective



Overview:

Private company founded in 2007 by semiconductor industry veterans

Locations:

Headquarters in Silicon Valley, California / Offices in Asia, Europe

Employees:

100 (Engineering=70, Sales/Marketing=20, Other=10)

Status:

\$50M+ profitable business, supporting over 100 tier 1 customers

Business Model:

Discrete product manufacturing and technology licensing

Technologies:

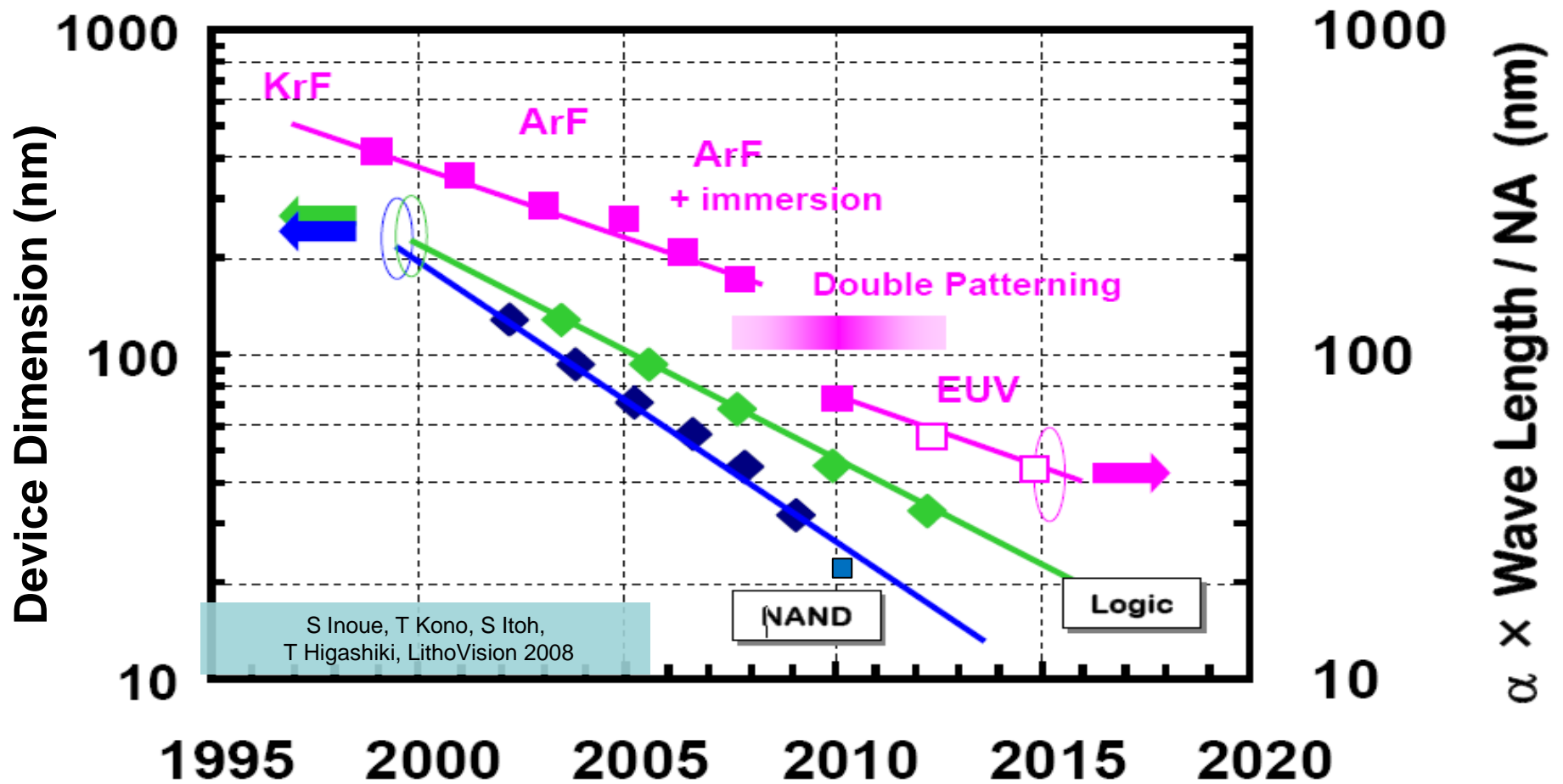
Serial Flash / DataFlash® / CBRAM®

Solid Intellectual Property Position: Over 100 patents granted or filed

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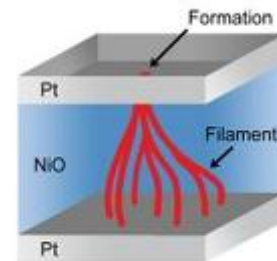
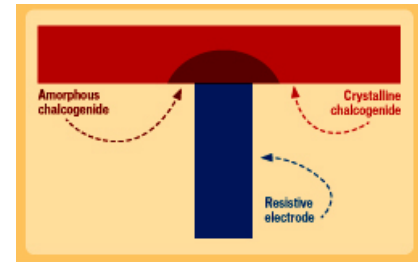
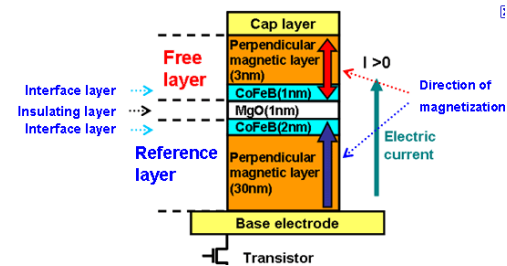
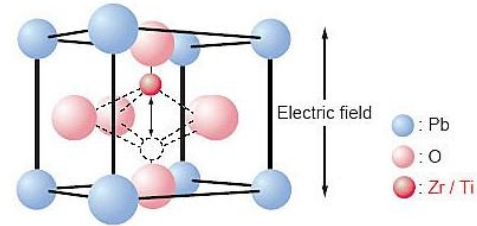
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Moore's Law

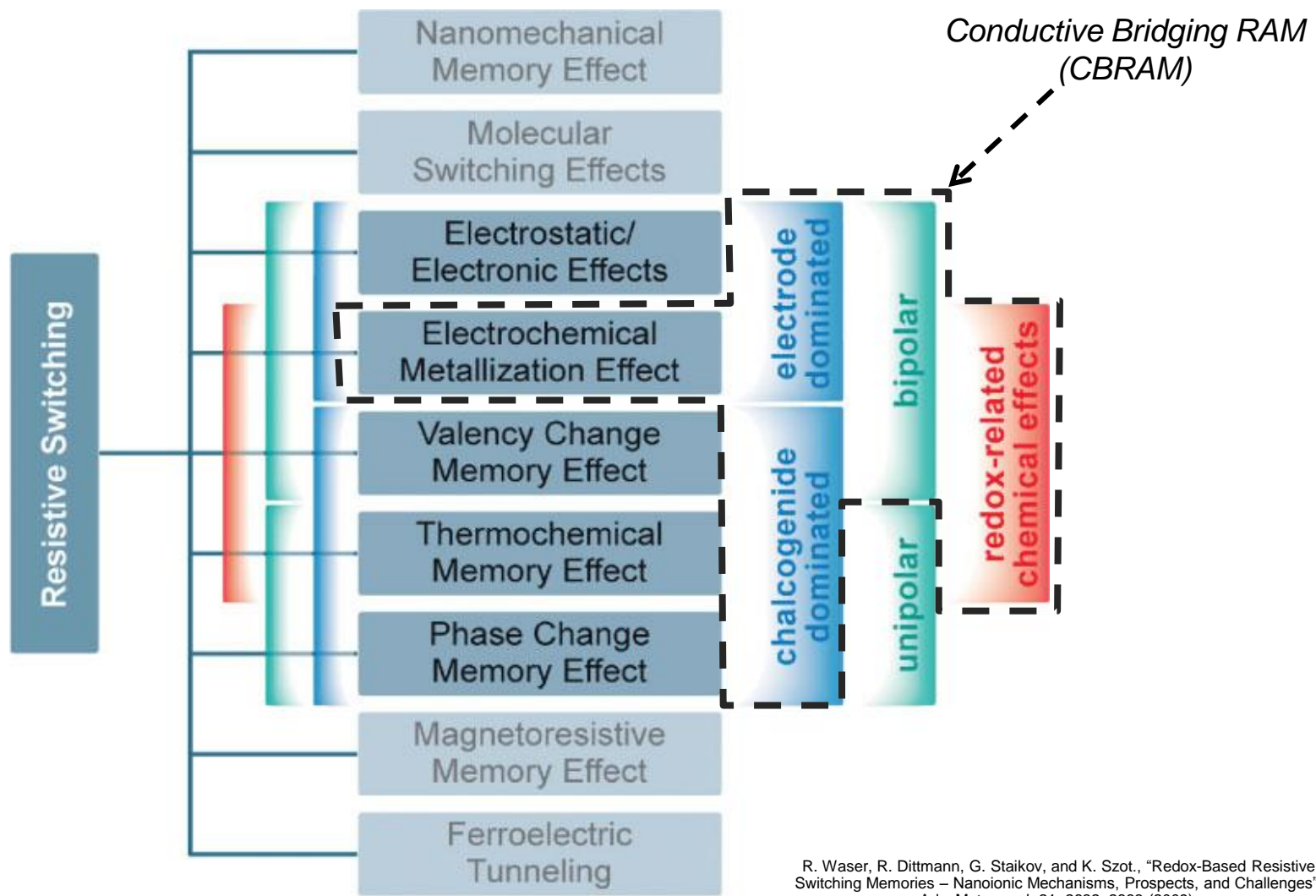


Candidates for Next Generation NVM

- **Ferroelectric RAM (FeRAM)**
- **Magnetic RAM (MRAM)**
- **Phase Change Memory (PCM)**
- **Resistance Change RAM (RRAM)**
(metal oxides)



Resistance Change Memory Taxonomy



R. Waser, R. Dittmann, G. Staikov, and K. Szot., "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges", Adv. Mater., vol. 21, 2632–2663 (2009).

Example of Electrochemical Memory Implementations

Table I. Summary of reported electrochemical metallization cells employing either Ag or Cu as an active electrode (AE) metal and various electrolytes and counter electrode (CE) metals.

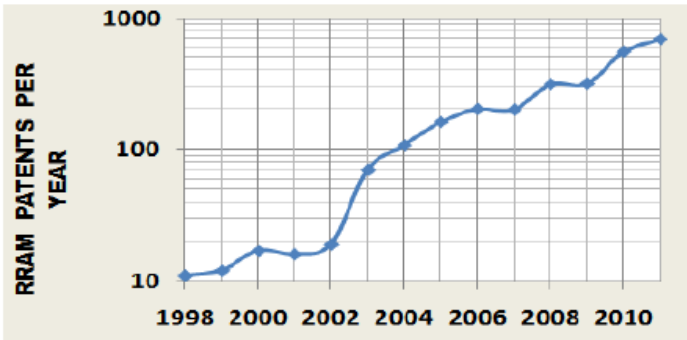
Electrolyte	Active electrode (AE) metals	
	Ag	Cu
Ge _x S _y	W ¹¹⁻¹⁹	W ¹⁵
Ge _x Se _y	W ^{11,16,20-23} Pt ²⁴ Ni ^{16,25-27}	W ¹⁵
Ge-Te	TiW ²⁸	TaN ²⁹
Ge-Sb-Te	Mo ³⁰	
As-S	Au ³¹	
Zn _x Cd _{1-x} S	Pt ^{32,33}	
Cu ₂ S		Pt ^{34,35} Ti ^{36,37}
Ta ₂ O ₅		Pt ³⁸⁻⁴⁰ Ru ⁴¹
SiO ₂	Co ⁴²	W ^{43,44} Pt ⁴⁵ Ir ⁴⁵
WO ₃	W ⁴³	W ^{43,46}
TiO ₂	Pt ^{47,48}	
ZrO ₂	Au ⁴⁹	
MSQ	Pt ^{50,51}	
GdO _x		W ⁵²
a-Si	Poly-Si ⁵³⁻⁵⁵ Cr ⁵⁶	
Ge _x Se _y /SiO _x		Pt ⁵⁷
Ge _x Se _y /Ta ₂ O ₅		W ⁵⁸
Cu _x S/Cu _x O		Pt ⁵⁹
Cu _x S/SiO ₂		Pt ⁵⁹

Electrolyte and CE materials are indicated in each row. For bilayer electrolytes, AE would be placed to the left of the electrolyte (e.g., Cu/A/B/Pt for a cell with a Cu AE metal and A/B bilayer electrolyte). Information compiled by John R. Jameson, Adesto Technologies Corp. Reprinted with permission from Reference 9. ©2011, IOP Publishing.

Table II. Summary of key performance data reported to date in electrochemical metallization arrays.

Material Systems	Cu/Cu ₂ S/Ti	Cu-Te/GdO _x /W	Ag/Ge _x S _y /W	Ag/Ge _x S _y or Ge _x Se _y
Reference	Kaeriyama et al. ³⁷	Aratani et al. ⁵²	Gopalan et al. ¹⁹	Dietrich et al. ⁴³
Array Size Tested	1 kbit	4 kbit	384 kbit, 1 Mbit	2 Mbit
Technology Node	250 nm	180 nm	180 & 130 nm	90 nm
SET Condition	1.1 V/5–32 μs	3 V/5 ns/110 μA	1.5 V/250 ns/30 μA	≥0.6 V/≤50 ns/10 μA
RESET Condition	1.1 V/5–32 μs	1.7 V/1 ns/125 μA	0.6 V/12 ms/20 μA	≤0.2 V/≤50 ns/20 μA
Endurance	10 ² –10 ⁴	10 ⁷	10 ⁵	10 ⁶
Retention (measured)	10 ² s @ 35 mV	100 hours @ 130°C	24 hours @ 110°C	10 ⁵ s @ 70°C
Retention (projected)	3 months	10 years	10 years @ 70°C	10 years

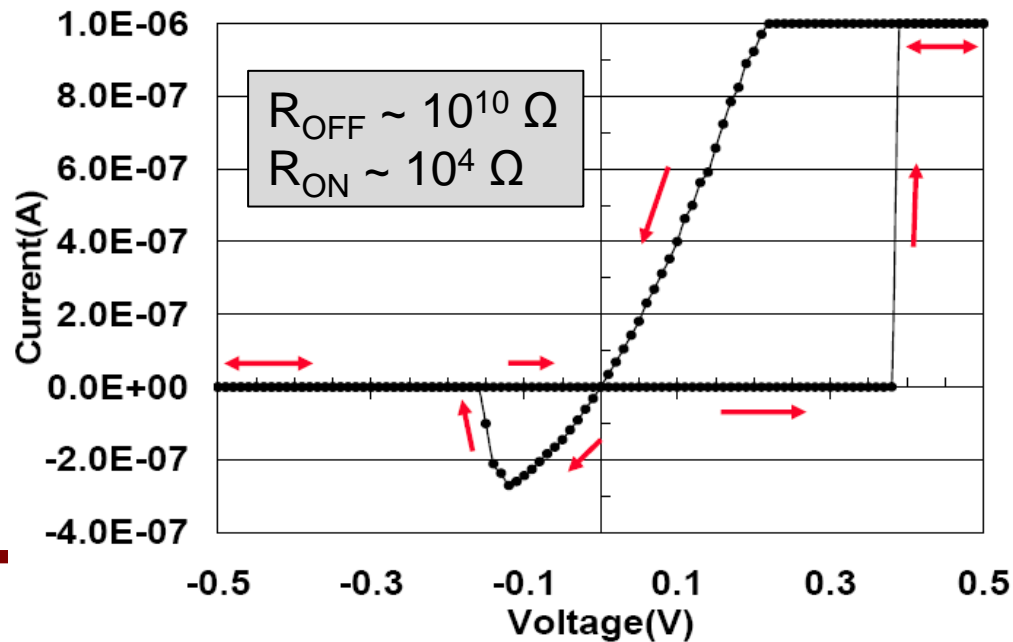
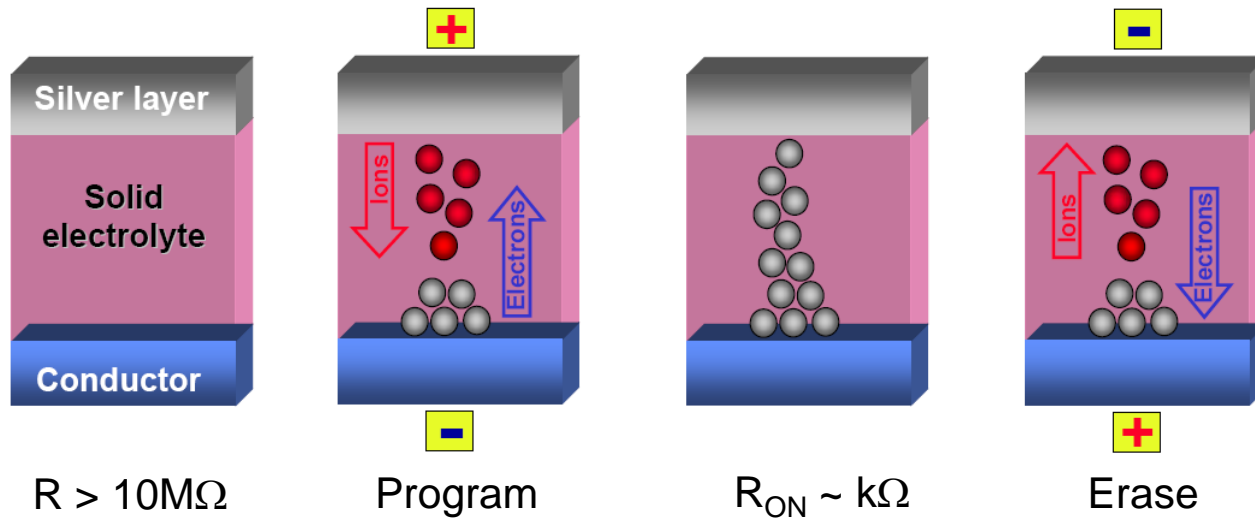
All arrays utilized 1T1R (one transistor for device selection and one resistive switching element) architecture. Compiled with information from Chen⁶² with the addition of data recently reported for Ag/Ge_xS_y/W cells.¹⁹



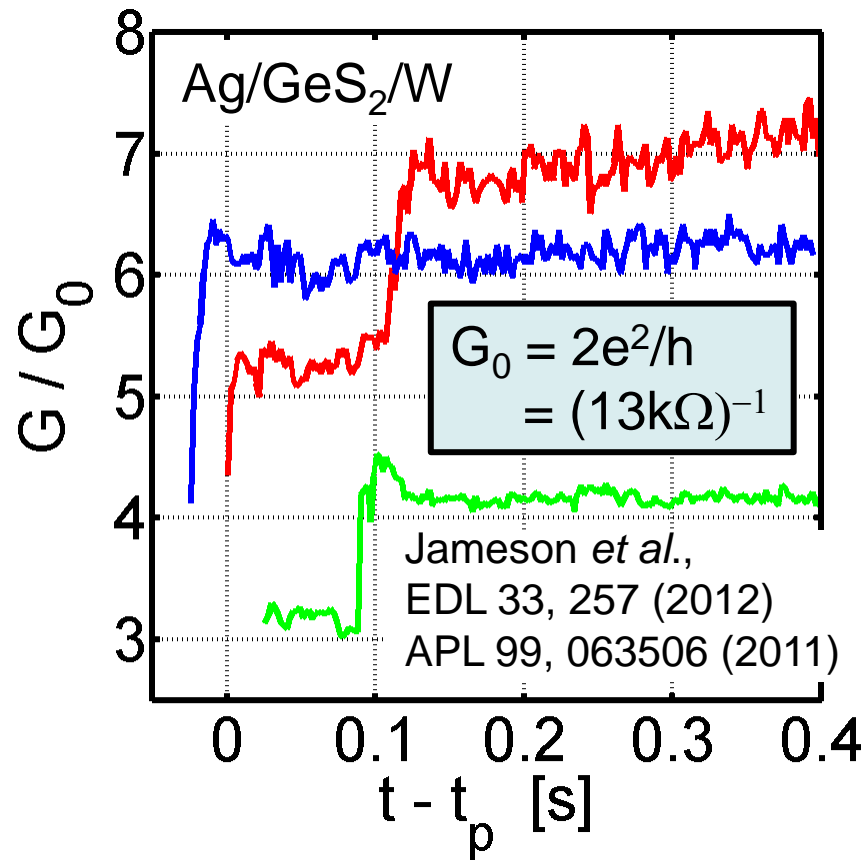
Patents by Category:	
Ionic/Electrolytic	204
Metal Oxide	169
Molecular/Polymer	74
Phase Change	961
Other/Unknown	1256

Figure 4 RRAM Patents per year [13]

Operating Principle of a CBRAM Cell



CBRAM cells as quantum point contacts (QPCs)



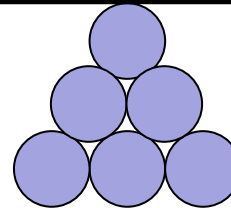
Similar observations in other systems:

Gap: Terabe *et al.*, Nature 433, 48 (2005)

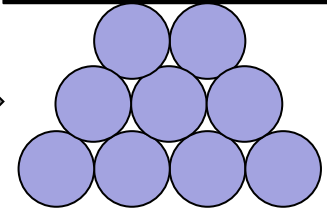
Non-gap: See paper for 8 refs from 2012/13

Physical picture is atomic:

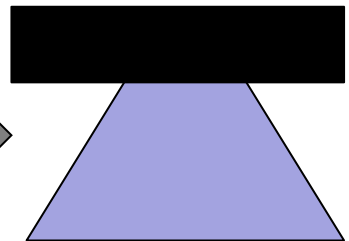
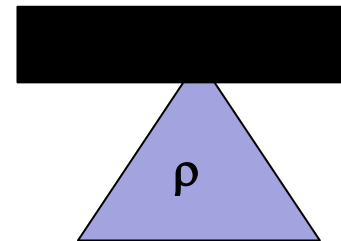
1 atom $\approx 1G_0$



2 atoms $\approx 2G_0$



Not continuum:



Summary of QPC-related device behavior:

“Conductive bridge random access memory (CBRAM) technology”, Jameson & Van Buskirk
- in -

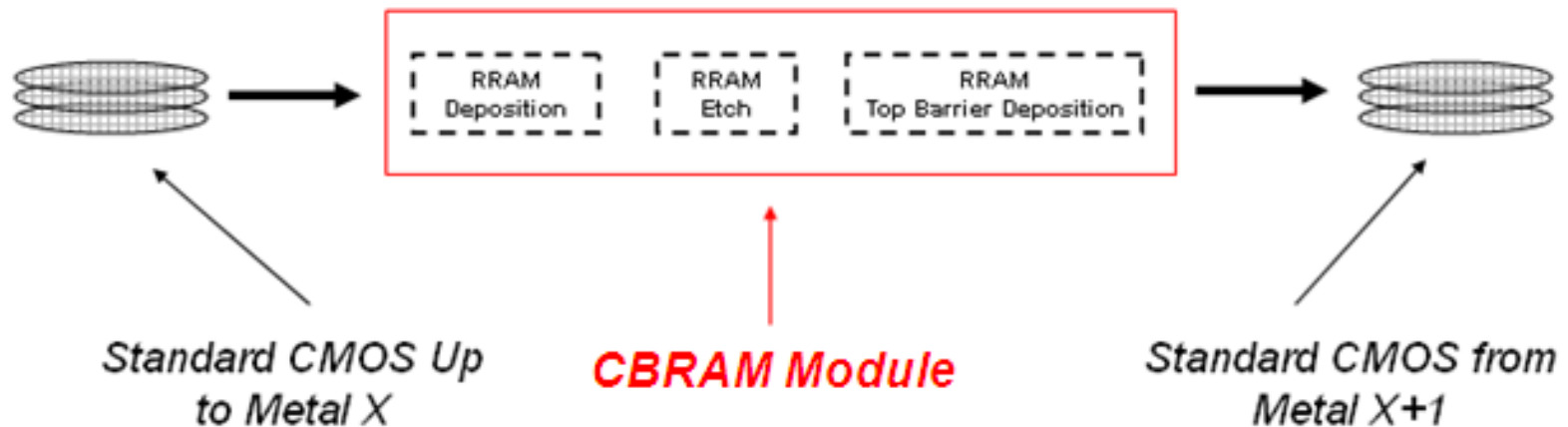
Advances in nonvolatile memory and storage technology, ed. Y. Nishi, Woodhead Pub.

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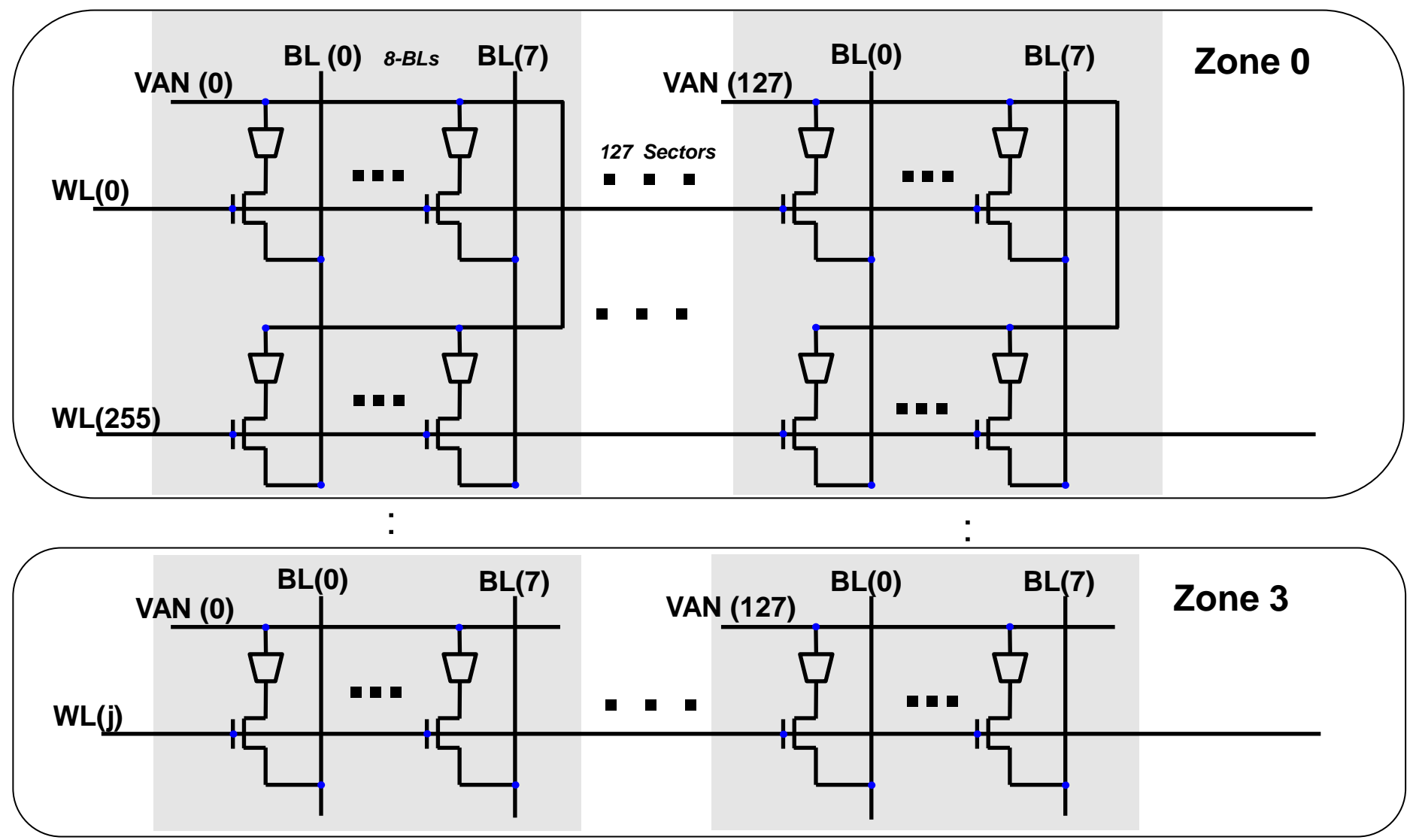
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CMOS Integration

- Adesto has successfully completed baseline integration flow in a standard CMOS Logic fab
- Adesto's process integration enables the introduction of CBRAM memory stack into CMOS BEOL without affecting the line
- Over **8000 wafers** processed so far without any issue on background CMOS process

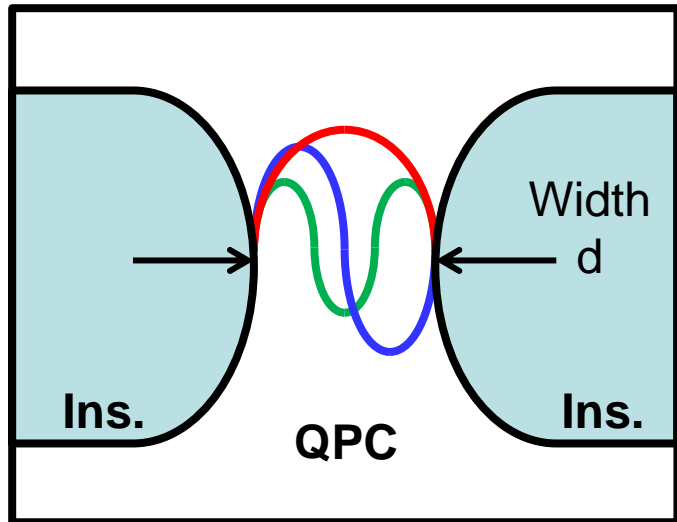


1Mb Array Architecture and Diagram



Importance of the Fermi wavelength in QPCs

To open **first** conductance channel ($R \sim 1/G_0$), need $d \sim \lambda_F$

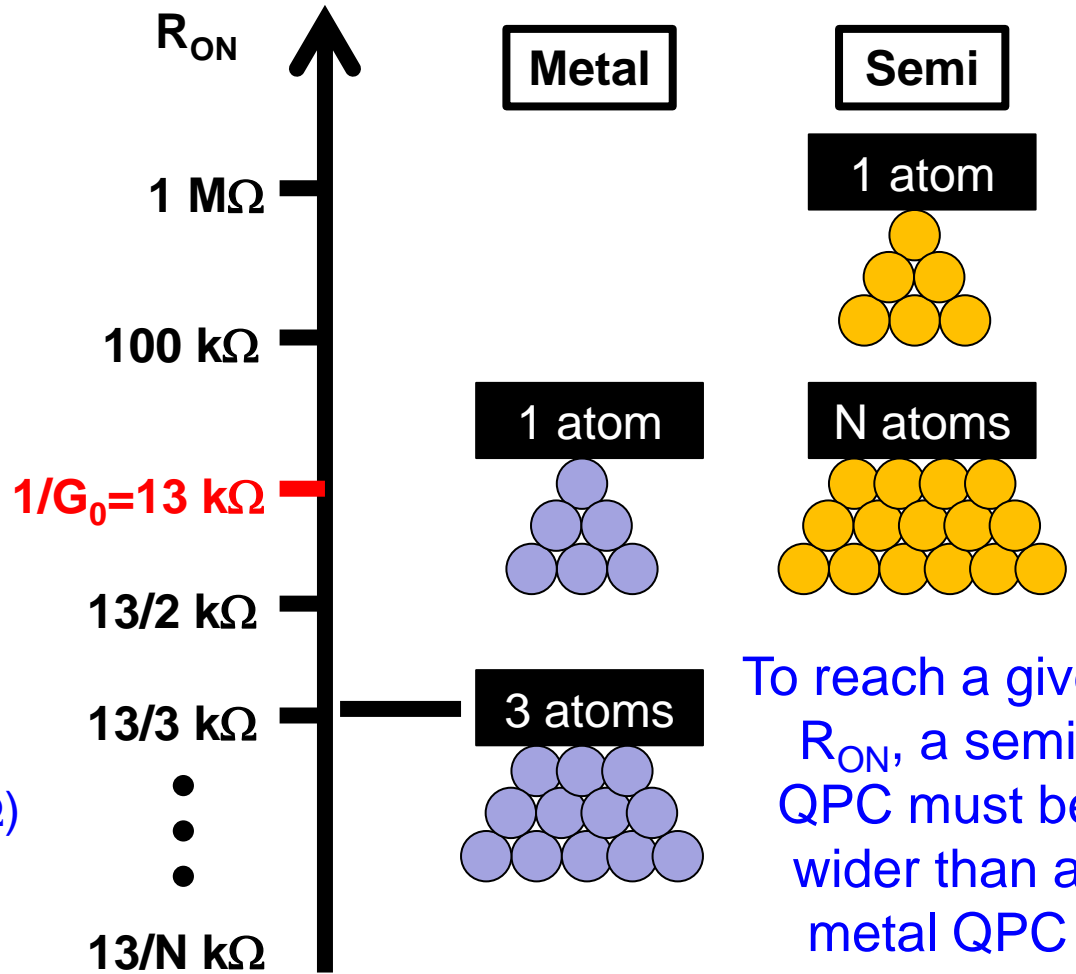


Metals:

$\lambda_F \sim 1 \text{ \AA} \rightarrow 1 \text{ atom} \sim 1 G_0 (13 \text{ k}\Omega)$

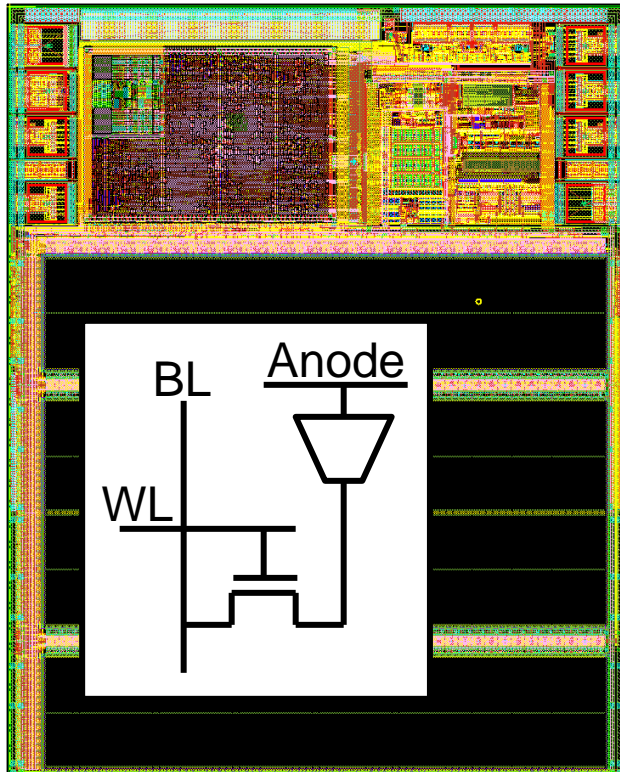
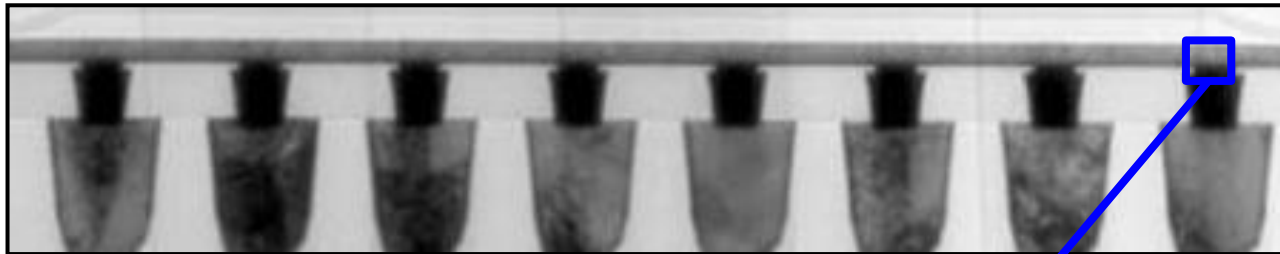
Semiconductors:

$\lambda_F \gg 1 \text{ \AA} \rightarrow 1 \text{ atom} \ll 1 G_0$



To reach a given R_{ON} , a semi QPC must be wider than a metal QPC

CBRAM: Cell Structure and Architecture



Amorphous alloy containing a semiconductor

Oxide

6 nm

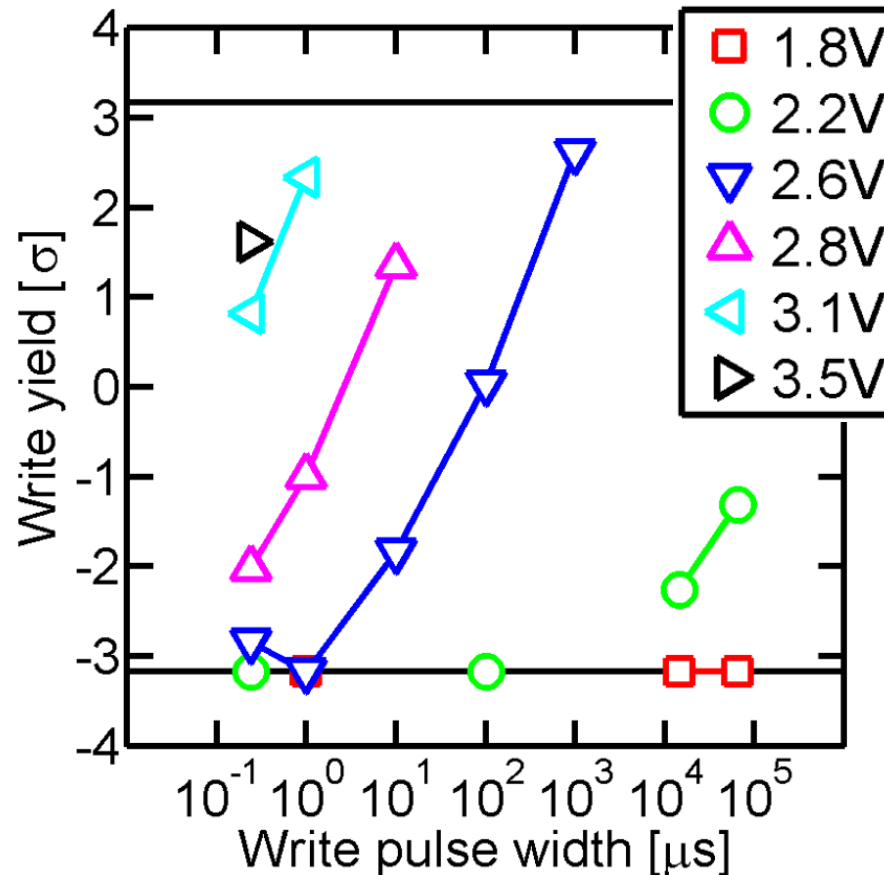
Metal cathode

- 128kb–1Mb EEPROM-compatible products
- I²C interface
- 1T1R
- 130nm Cu BEOL

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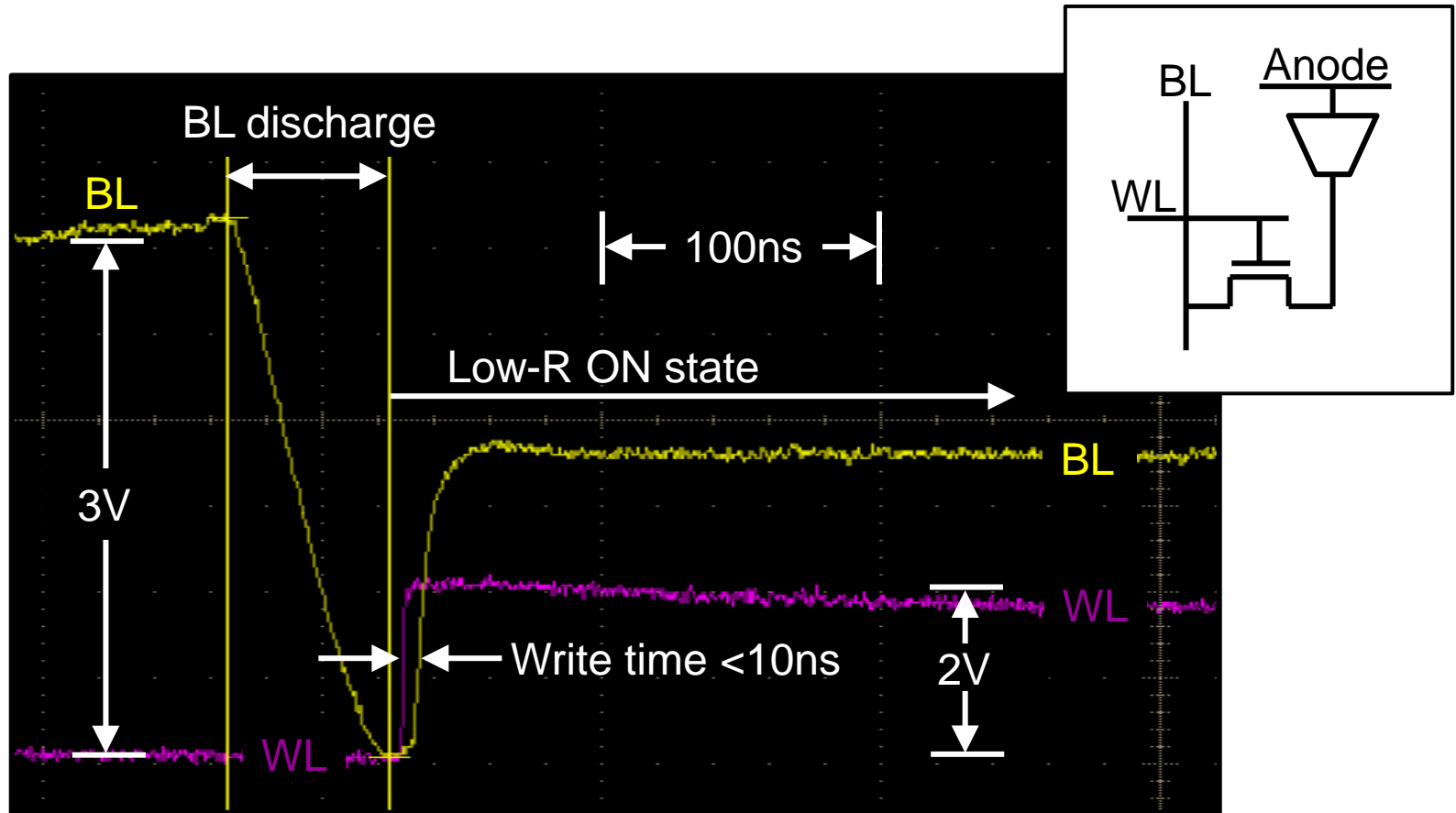
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CBRAM: Forming



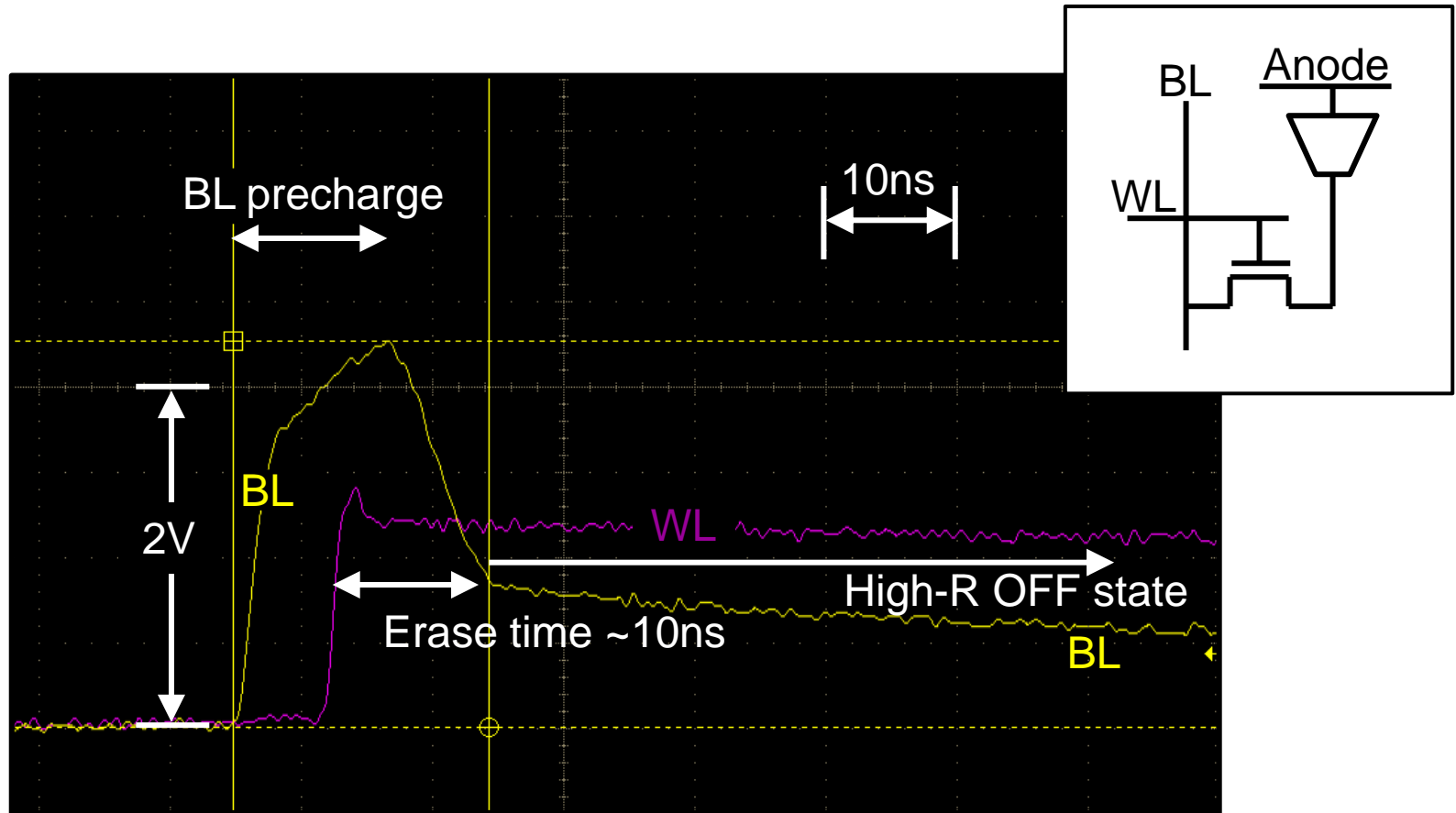
- In general, first write is slower than subsequent writes
- But, high yield still achievable with forming pulse of $10\mu\text{s}/3\text{V}$

CBRAM: Write Speed



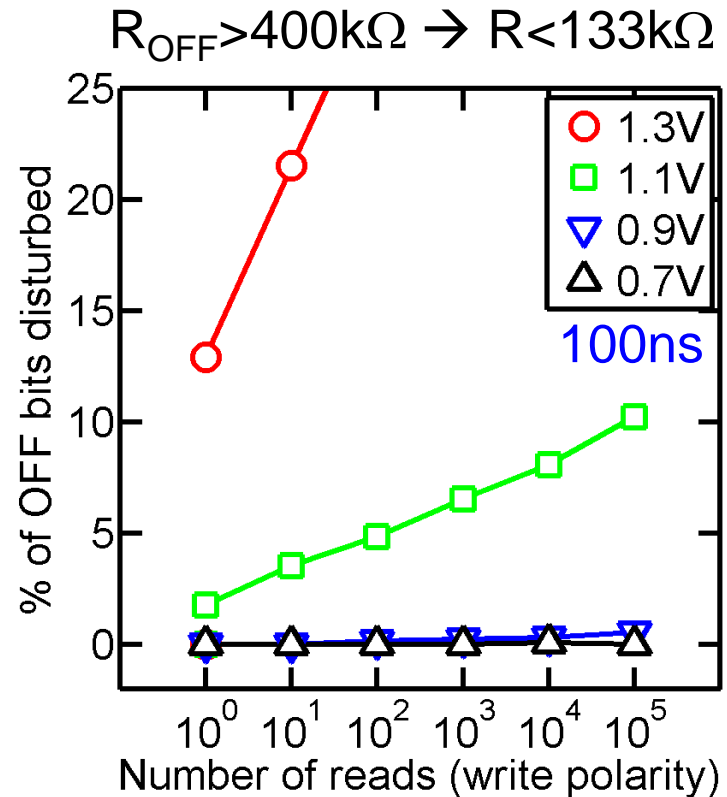
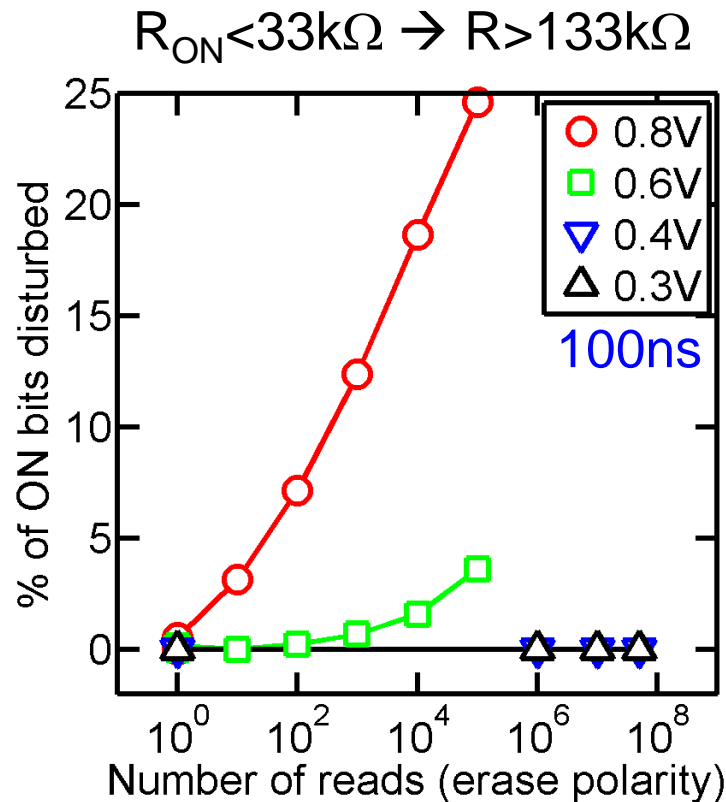
- Write speed depends “exponentially” on voltage
- At a write voltage of 3V, sub-10ns writes are possible
- Typical program uses ~2V/100ns-1us

CBRAM: Erase Speed



- Above a voltage of $\sim 2V$, sub-10ns erases are also possible
- Typical erase uses $\sim 1.5V/100ns-1\mu s$

CBRAM: Immunity to Read Disturbs



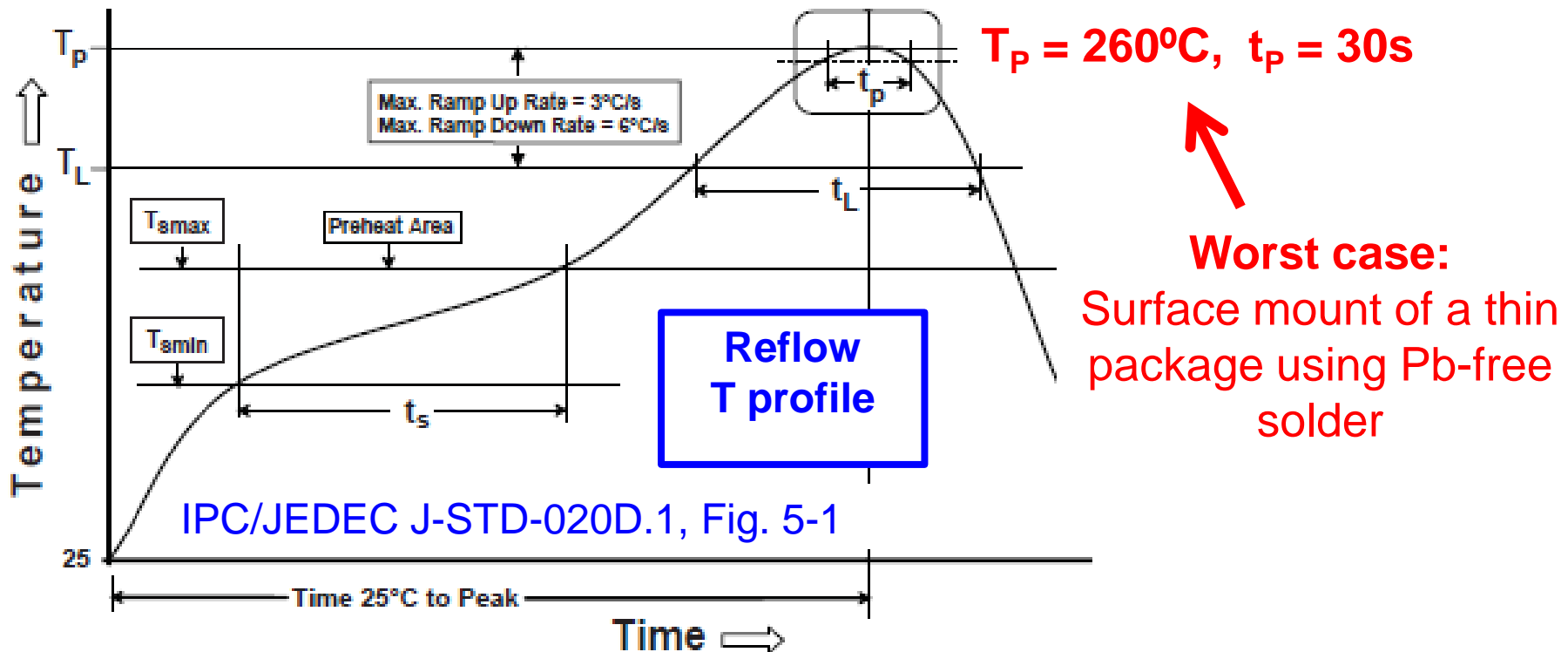
- The exponential dependence of speed on voltage allows read disturbs to be avoided
- Typical read uses $\sim 0.2V/100ns$

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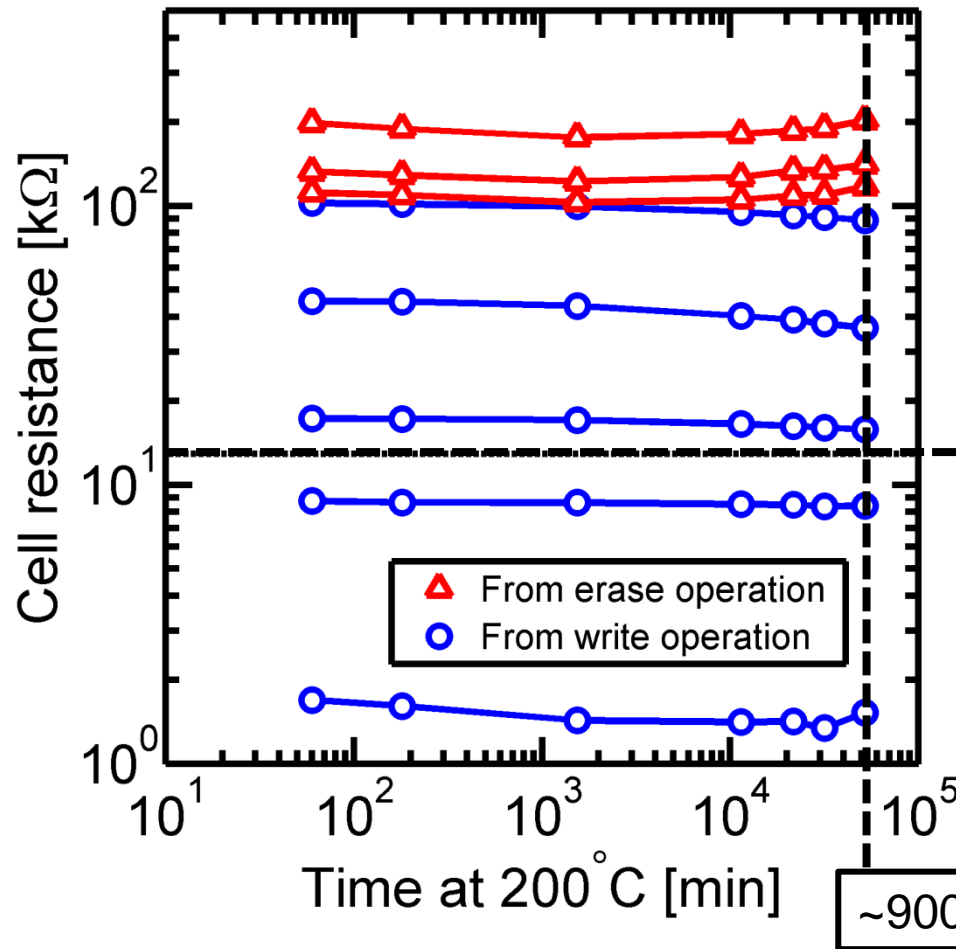
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The Need for High-T Retention in Emerging Memories

- Operational requirement for some applications (e.g., automotive)
- Other applications (e.g., code storage) utilize wafer-level or package-level programming, followed by solder reflow for board mount
- Low-density demonstrations to prove out new technology



CBRAM: Example of Long-term High-T Retention



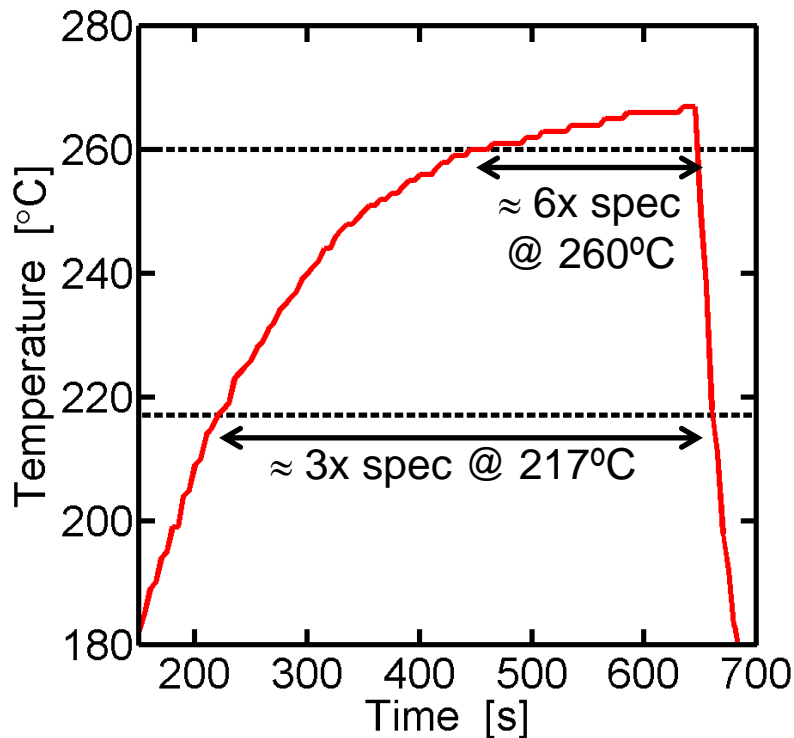
- Cells are stable at 10x greater R than that of a 1-atom point contact of a typical metal (*i.e.*, $\sim 1/G_0$)
- High-T retention of a given R state is insensitive to the operation used to obtain that state

$$R_{ON} = 1/G_0 = 13 k\Omega$$

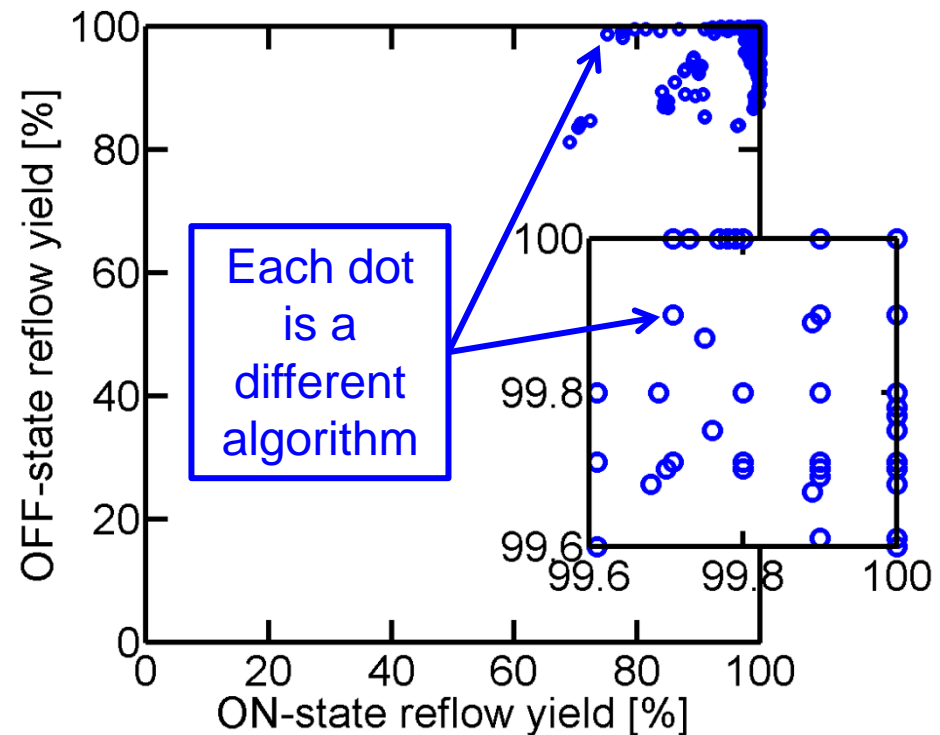
- Ongoing product-level retention tests at 110°C have shown no fails after more than 8 months

CBRAM: Retention through Simulated Solder Reflow

Anneal profile simulating high-T portion of multiple Pb-free solder reflows



Retention yields following simulated reflow



- Excellent retention is achievable at reflow-like times and temperatures
- Algorithm design is important, even with suitable materials system

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CBRAM – Robust in Extreme Environments

Recent News —

Collaboration with Adesto Technologies and Nordion Confirms Gamma Irradiation Tolerance of CBRAM® Non-Volatile Memory

Wednesday, October 16, 2013

Capability Opens New Market Opportunities to Ultra-Low Power Memory Products

Sunnyvale, CA, October 16, 2013 -- Adesto Technologies, a memory solutions provider delivering innovative products for code and data storage applications, and Nordion, with global expertise in the design and construction of commercial gamma irradiation systems, today announced the successful completion of gamma irradiation testing of Adesto's CBRAM non-volatile memory products. The results demonstrated CBRAM's tolerance for gamma testing with device function and data storage surviving gamma radiation exposure...

“Gamma irradiation is a proven technique for the sterilization of single use medical devices and other consumer products that require strict microbial decontamination.” — Emily Craven, Manager of Sterilization Science at Nordion

CBRAM® Gamma Tolerance Study

Study 1: (vs. Conventional Flash)

Device	Technology	DUT ID	Gamma Dose (krad Si)	Data Loss (# bit errors)	Result
AT25F512B	Floating Gate	1	447	859	FAIL
AT25F512B	Floating Gate	2	447	6519	FAIL
AT25F512B	Floating Gate	3	131	955	FAIL
AT25F512B	Floating Gate	4	131	4	FAIL
RM24EP128KS	CBRAM	1	447	0	PASS
RM24EP128KS	CBRAM	2	447	0	PASS
RM24EP128KS	CBRAM	3	131	0	PASS
RM24EP128KS	CBRAM	4	131	0	PASS

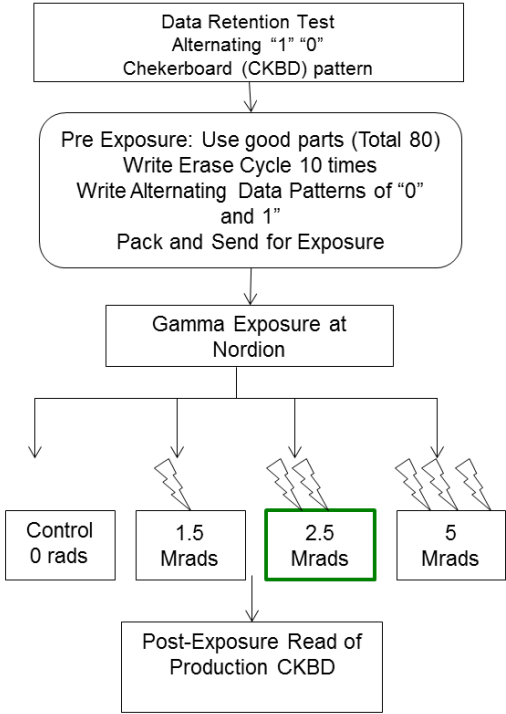
Conventional
Flash Memory
Devices

CBRAM
Devices

- Tests performed by ASU

CBRAM had no failure even at twice the normal dose used for Gamma Sterilization

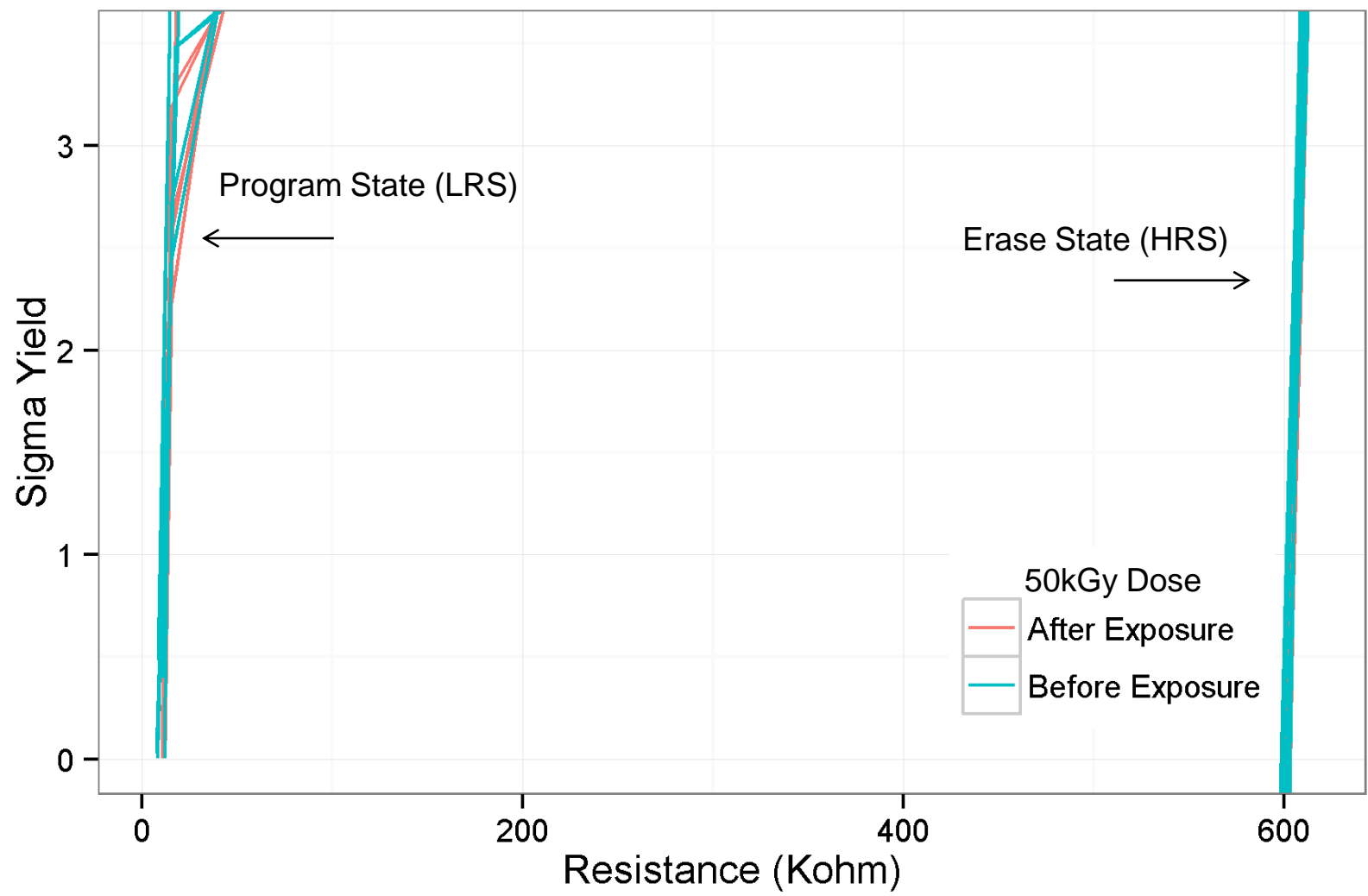
Study 2: (High Dose Gamma)



- Tests performed by Nordion – Leading provider of isotopes and radiation therapy services to the medical and health care industry
- Results : CBRAM PASSED Data Retention Test



CBRAM Cell Tolerance to Gamma Radiation – Resistance Distribution



Summary and Outlook for CBRAM

- **Field of emerging memory is diverse and vibrant**
- **CBRAM has been a leading candidate, and has recently made significant new advancements**
- **CBRAM has achieved high-T retention by using a combination of materials engineering & a properly designed algorithm**
 - **Opportunities for apps w/ high-T operation or requiring solder reflow**
- **Tolerance to gamma radiation has also been achieved**
 - **Opportunities for medical or aerospace applications**