## Hardware Revolution

August 2018

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**Si**Five

### **Timeline** From Invention to Today



**Si**Five







### SiFive **Global Presence and Reach**



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**Si**Five

### Team Inventors, Founders, Industry Leaders



**Si**Five

Naveed Sherwani CEO



Shiva Natarajan CFO



Sunil Shenoy VP HW Engineering



Shafy Eltoukhy VP Operations



Jack Kang VP Product



Mark Wright VP Custom SoC Sales



Yunsup Lee CTO



Krste Asanovic Chief Architect



Andrew Waterman Chief Engineer



Brad Holtzinger VP Sales



Jeff Mulhausen VP Marketing



Thomas Xu SiFive China Leader

The SiFive Management Team combines the inventors of the RISC-V ISA with seasoned industry executives.



## Hardware Laws and Consequences





**Si**Five

### **Going** Over the Edge



Based on SPECIntCPU. Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e. 2018 **Si**Five



# **Going** Over the Edge

# Going Over the Edge



More Custom Compute

More Custom Hardware

For Custom Workloads and Applications

SiFive

## Challenges of Custom Hardware

Too Expensive and Takes Too Long:

#### **Cost of Developing New Products**



# Challenges of Custom Hardware

	Architect	Logic	RTL	Provide Analog	Verification	Simulation
B	Emulation	Synthesis	Place & Route	Layout	ECO	Foundry
	Package	Test		14+	Discipline	es

#### **Too Many Experts Needed**



# How did Instagram turn into a \$1B acquisition with only 13 employees?







# The Lesson from Software Work at a Higher Level







## SiFive Designer IP Customization and Push-Button Configuration

ers Dashboard RISC-V Core IP Freedom SoC Staff Admin DG Pro   F	shboard RISC-V Core IP Freedom SoC Staff Admin DG Pro   Forums				
Customize E3 Series: E34 Base					
S ES SeriesCore Complex Local Interrupts	> Privilege Modes	Machine and User mode	0		
E3 Series Core	✓ Instruction Cache	16KB 4-way	0		
Color Field C	The instruction cache can b Instruction Tightly Integrate performance, predictable The E34 default is a 16KB 4 cache. 16KB 32KB 6/ 4-way Set Associative (E)	e partially reconfigured into an d Memory (TIM) to provides high- truction deliver, and the sub- way set associative instruction IKB 128KB 34 Default)			
	8-way Set Associative				
TileLink TileLink TileLink	16-way Set Associative				
	> Data Subsystem	64KB, no cache	0		
	> PMP	8 Regions	0		
	> PLIC	255 Interrupts, 7 Priorities	0		
	> Local Interrupts	14 Local Interrupts	0		
	> Debug Hardware	Included	0		
	> Instruction Trace Unit	Included	0		
	> Front Port Bus Interface	TileLink	0		
	Front Port Bue Interface	TiloLink Est. Speed: 326 emark Est. Performance: 1.44 Predicted Area: 0.70 GENERATE TV	o MHz 5 DMIPS/MHz 2 mm <sup>2</sup>		

**⇔** si⊧

### Freedom Unleashed 64-bit Multi-Core RISC-V Linux Platform



#### 1.5+ GHz U54-MC SiFive CPU

- ✓ 1x E51: 16KB L1I\$, 8KB DTIM with ECC support
- ✓ 4x U54: 32KB L1I\$, 32KB L1D\$ with ECC support
- Single- and Double-precision floating-point support
- ✓ 2MB Banked L2\$ with directory-based cache-coherence & ECC support

#### ChipLink

- Serialized Chip-to-Chip
  - Coherent TileLink Interconnect
- DDR3/4, GbE, Peripherals



# **Benefits**



- More Design Starts
- More IP Providers
- More Customization
- More Startups

- Reduced Level of Expertise
- Bring Excitement
- Democratize Access
- Focus on Creating Value
- Help Create a Trillion Dollar Industry

