Sign-based Zero-Forcing Adaptive Equalizer Control for High-Speed I/O

Yasuo Hidaka
Fujitsu Laboratories of America, Inc.
November 18, 2013

IEEE Circuits and Systems Society
Santa Clara Valley Chapter

Outline

- Background
- State-of-the-art Equalizer for High-Speed I/O
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
- Implementation and Evaluation Results
- Summary

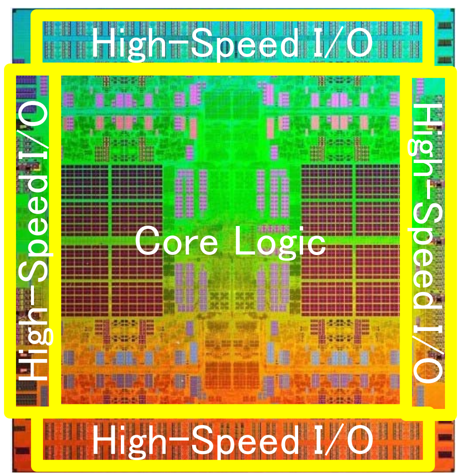
Outline

- Background
  - Applications of High-Speed I/O
  - Frequency-Dependent Channel Loss
  - Inter-Symbol Interference (ISI)
- State-of-the-art Equalizer for High-Speed I/O
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
- Implementation and Evaluation Results
- Summary

Applications of High-Speed I/O

- Application Channels
  - On-board: Chip to chip with no connector
  - Module I/F: Chip to module via 1 connector
  - Backplane: Board to board via 2 connectors
  - Cable: Rack to rack via 2 connectors

- Examples
  - Standard High-Speed Interfaces
    - OIF CEI, IEEE 802.3 Ethernet, PCI Express, etc
  - Proprietary High-Speed Interfaces
    - CPU I/F, Bridge chip I/F, Switch chip I/F, etc

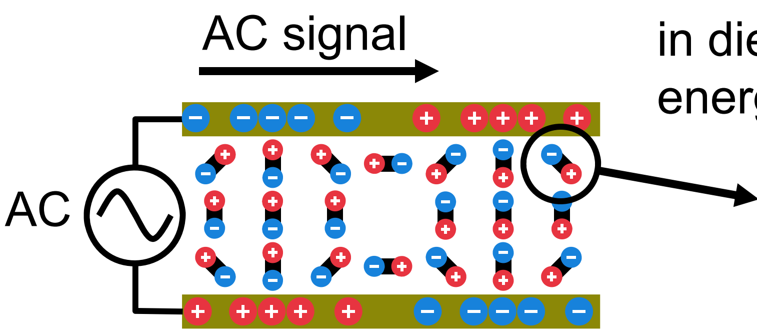


- State-of-the-art Performance of HSIO
  - Data rate 25~32Gbps per lane
  - Channel loss 35~40dB at Nyquist frequency
  - Channel length 0.3~1m PCB, 3~7m cable
  - HSIO density 20~100+ lanes per chip

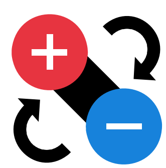
Frequency-Dependent Channel Loss[1,2]

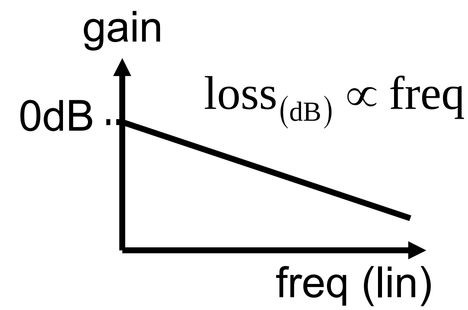
FUJITSU

Dielectric Loss

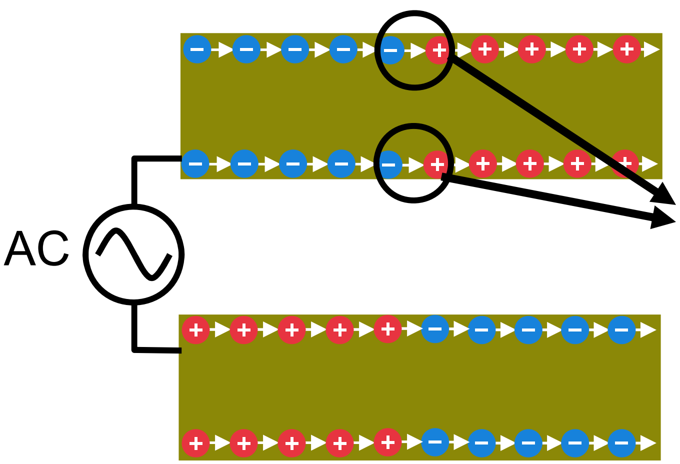


Rotation of dipoles in dielectric loses energy per every Hertz

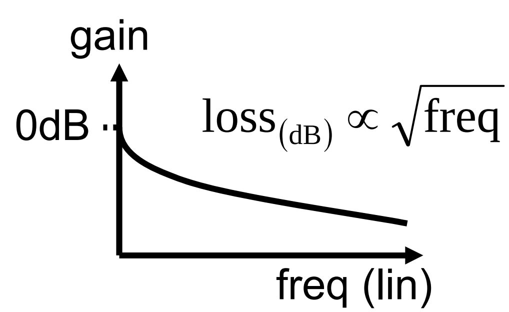




Skin Effect



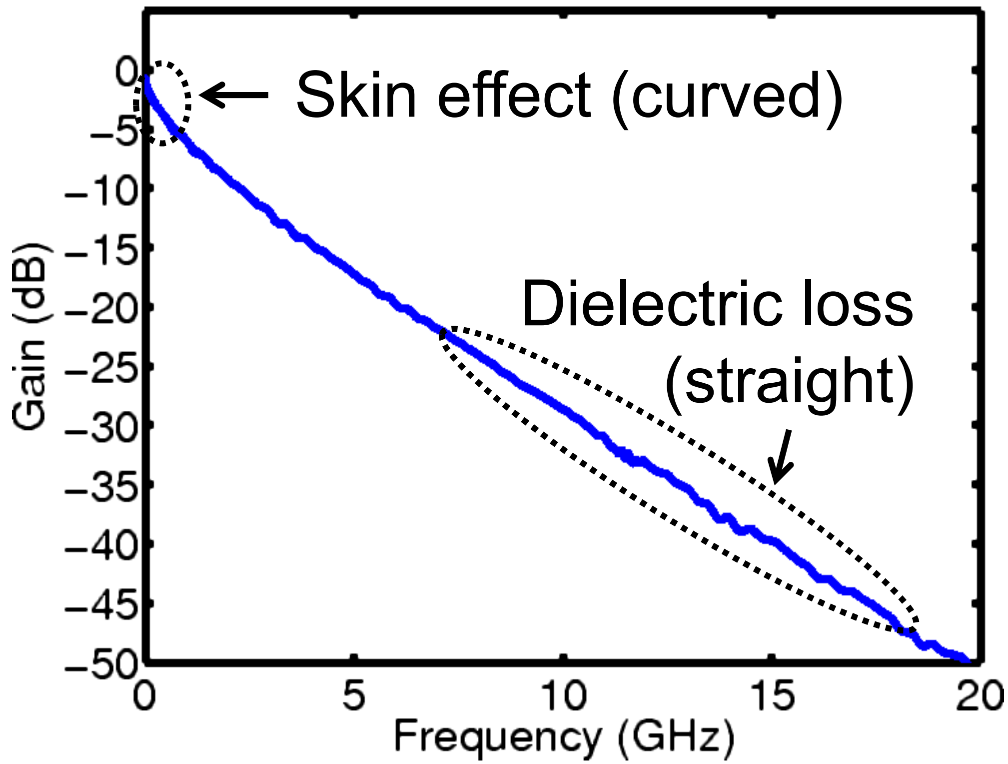
AC current **flows only in metal surface** with increased resistance



Channel Loss Example (Linear Frequency Axis)

FUJITSU

$$loss\ (dB) \propto \underbrace{k_1\sqrt{f}}_{\text{Skin Effect}} + \underbrace{k_2 f}_{\text{Dielectric Loss}}$$



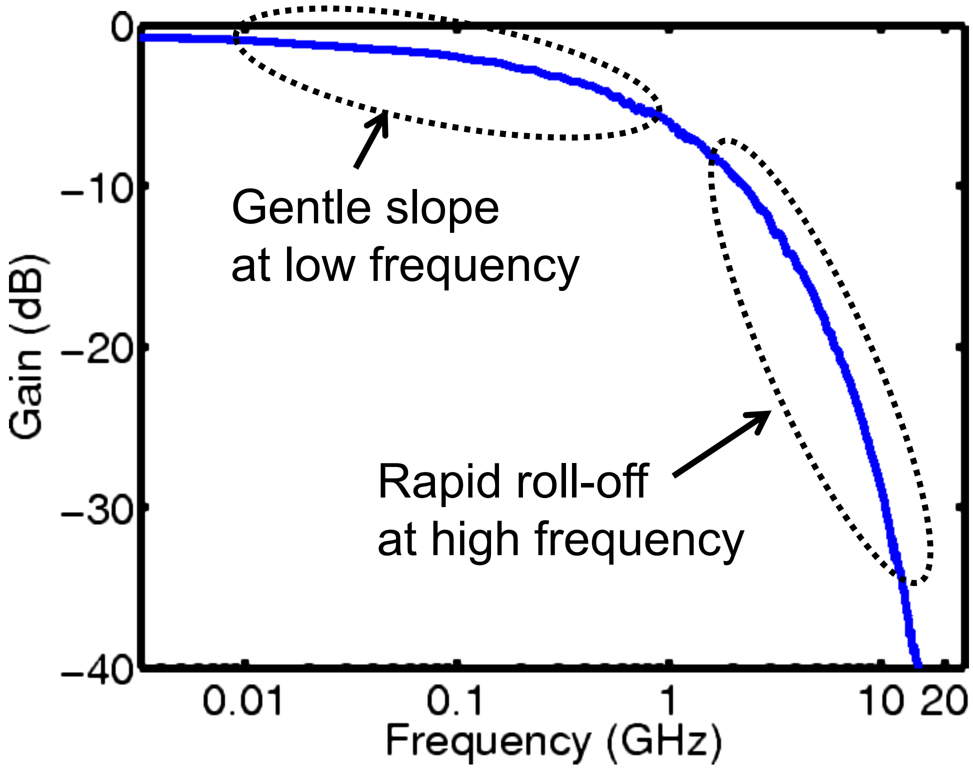
(Linear)

- **Skin effect**
  - Curved with concave up
  - Primary cause at low freq
- **Dielectric loss**
  - Straight line
  - Primary cause at high freq
- *We often overlook or neglect low-frequency loss*
  - Loss is small
  - Degenerated at DC and hardly recognized

Channel Loss Example (Log Frequency Axis)

FUJITSU

$$loss\ (dB) \propto \underbrace{k_1\sqrt{f}}_{\text{Skin Effect}} + \underbrace{k_2 f}_{\text{Dielectric Loss}}$$

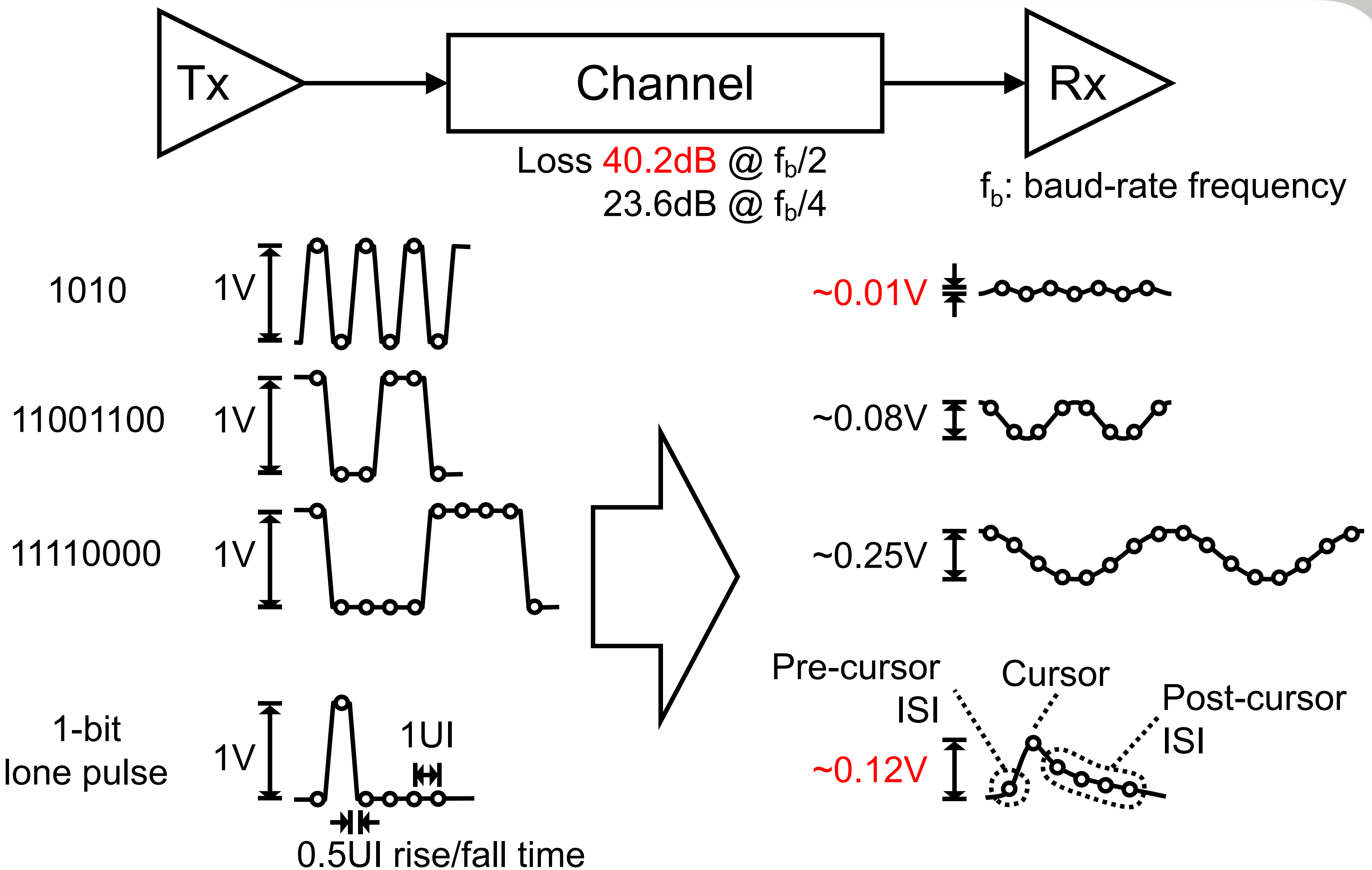


(Log)

- Always exponential roll-off
  - Regardless of skin effect or dielectric loss
- Low-frequency loss
  - Start as low as 10MHz
    - Skin depth 20um@10MHz
    - PCB trace thickness 35um
  - Gentle slope
    - < 3dB/dec

Inter-Symbol Interference (ISI)

FUJITSU



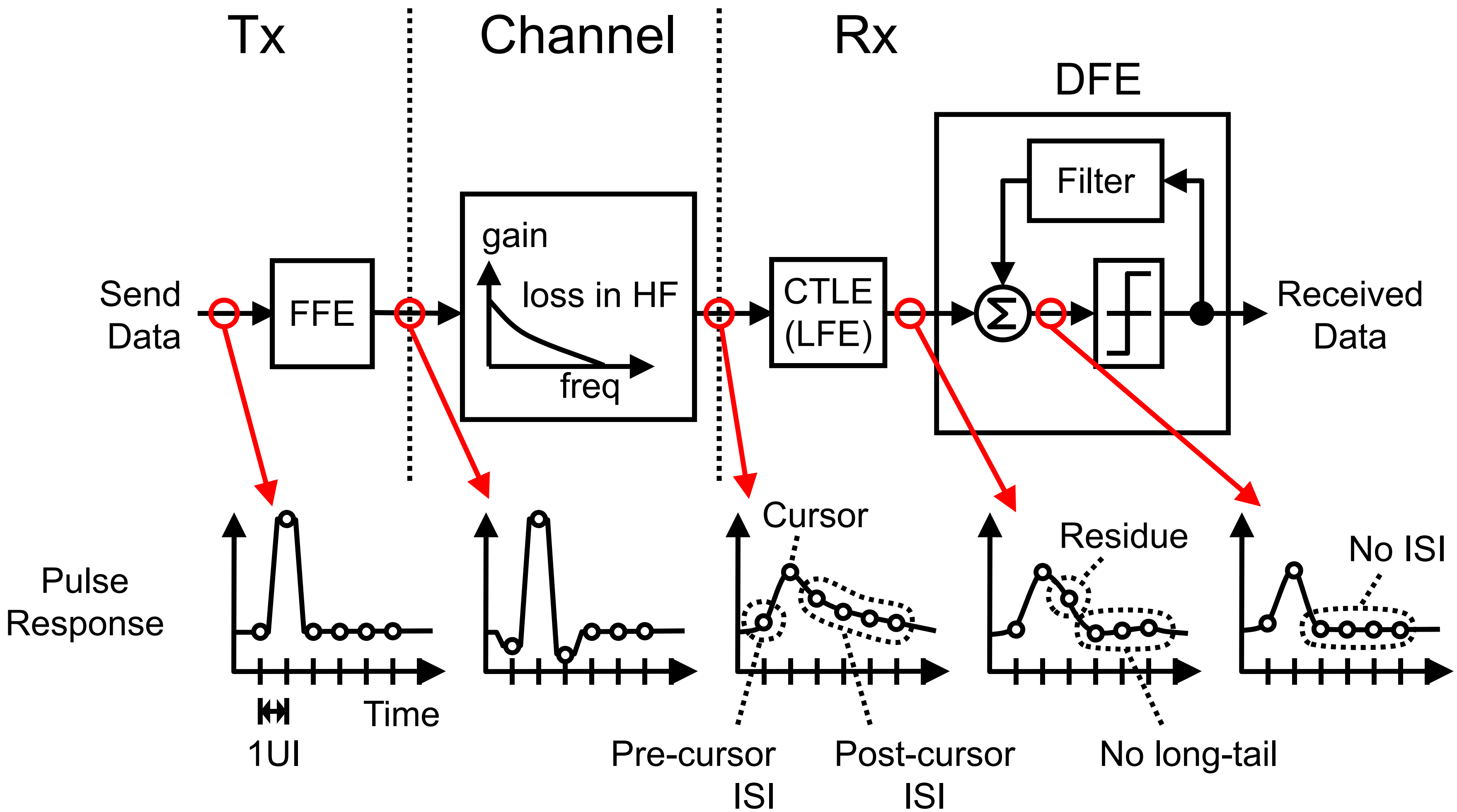
UI: Unit Interval

Outline

- Background
- State-of-the-art Equalizer for High-Speed I/O
  - Conventional High-Frequency Equalizers
    - Overview
    - CTLE (Continuous-Time Linear Equalizer)
    - FFE (Feed-Forward Equalizer)
    - DFE (Decision-Feedback Equalizer)
    - Speculative DFE
  - Low-Frequency Equalizer
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
- Implementation and Evaluation Results
- Summary

State-of-the-art Equalizer for High-Speed I/O

FUJITSU

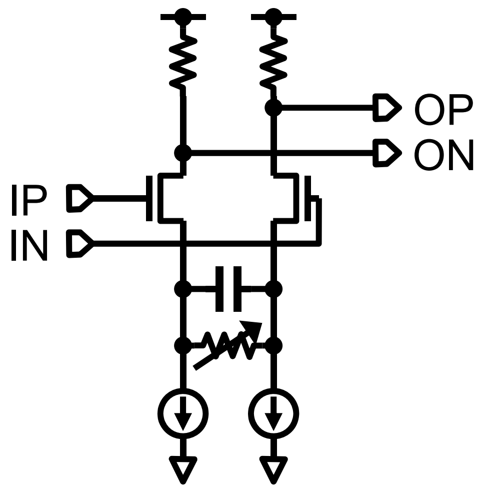


FFE: Feed-Forward Equalizer

CTLE: Continuous-Time Linear Equalizer
LFE: Low-Frequency Equalizer
DFE: Decision-Feedback Equalizer

CTLE (Continuous-Time Linear Equalizer)[3-7]

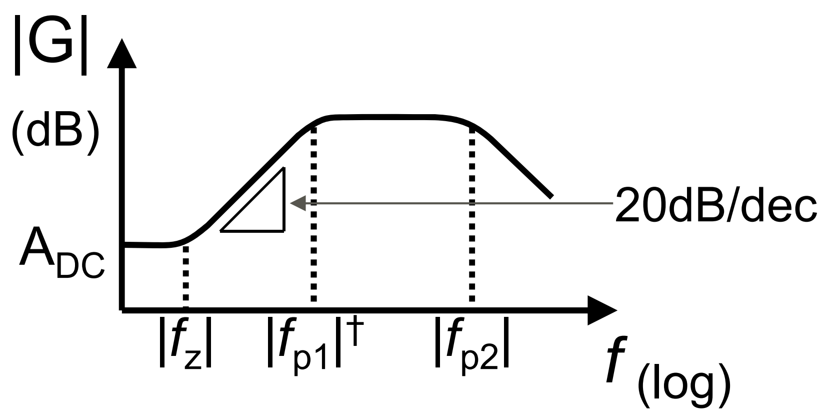
- Continuous-time high-pass filter
- Example
  - 1st order CTLE



Transfer Function in s domain:

$$G(s) = A_{DC} \frac{1 - \frac{s}{2\pi f_z}}{\left(1 - \frac{s}{2\pi f_{p1}}\right)\left(1 - \frac{s}{2\pi f_{p2}}\right)}$$

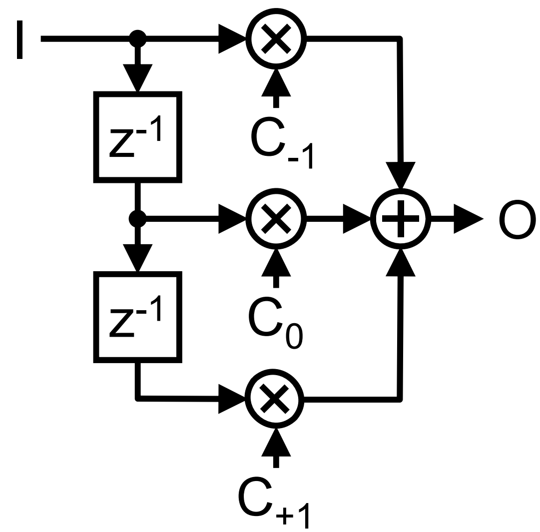
1 zero
2 poles



† : $|f_{p1}|$ is ¼ ~ ½ of baud-rate frequency.

FFE (Feed-Forward Equalizer)[8-10]

- Discrete-time high-pass filter
- Example
  - 3-tap FFE

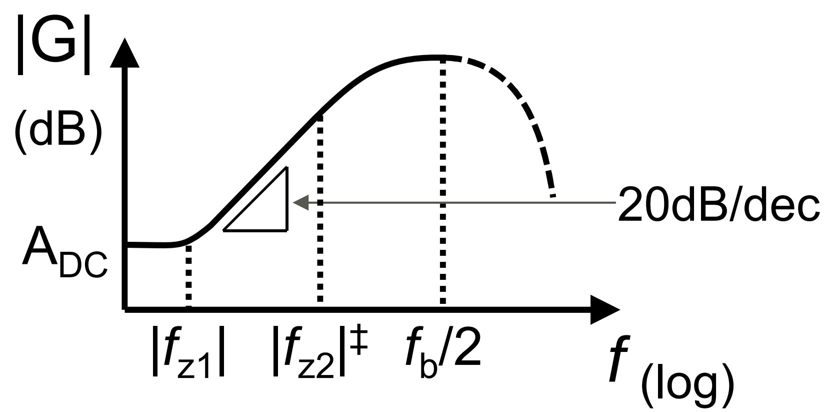


Transfer Function in z domain:

$$G(z) = C_{-1} + C_0 z^{-1} + C_{+1} z^{-2} = C_{-1} \frac{(z - z_1)(z - z_2)}{z^2}$$

$$z = \exp(s/f_b)$$
$$z_1 = \exp(2\pi f_{z1}/f_b)$$
$$z_2 = \exp(2\pi f_{z2}/f_b)$$

2 zero
0 poles†

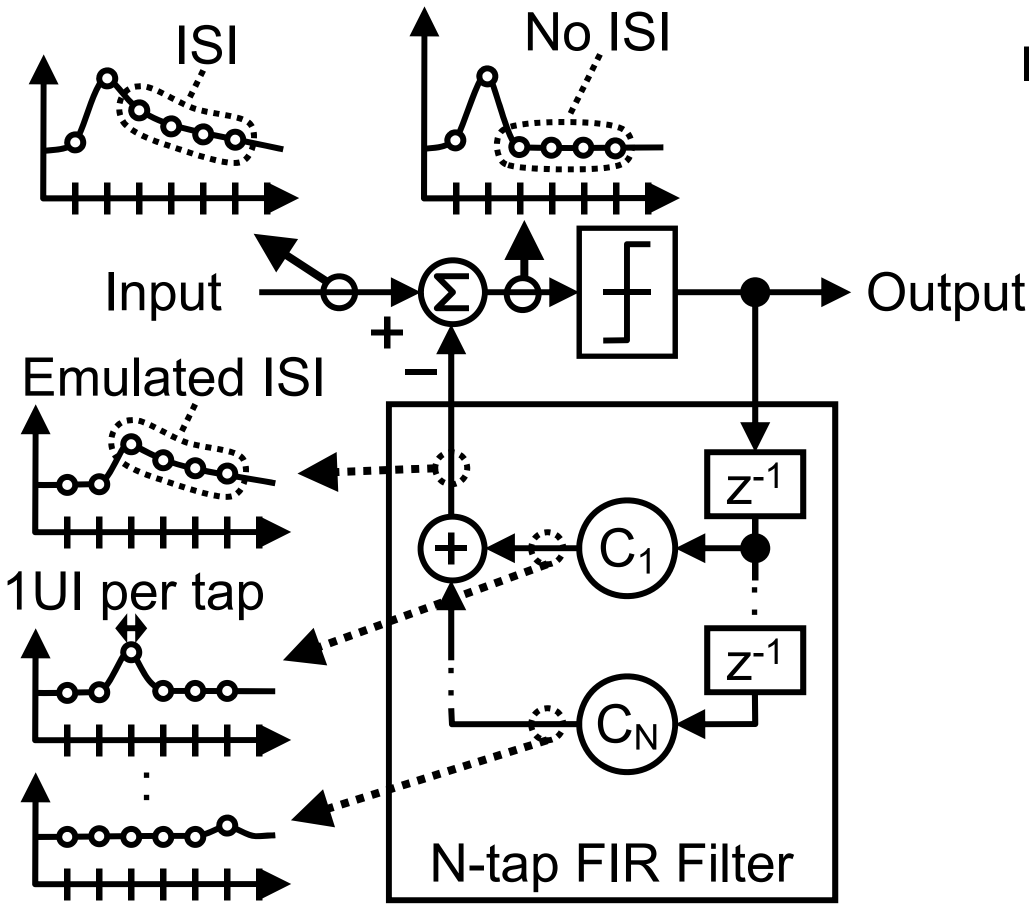


† : An FIR filter cannot have a pole. $f_b/2$ is not a pole, but the max effective frequency.
‡ : f_{z1} (<0) on left half of s plane boosts gain. f_{z2} (>0) on right half of s plane adjusts phase.

DFE (Decision-Feedback Equalizer)[11,12]

FUJITSU

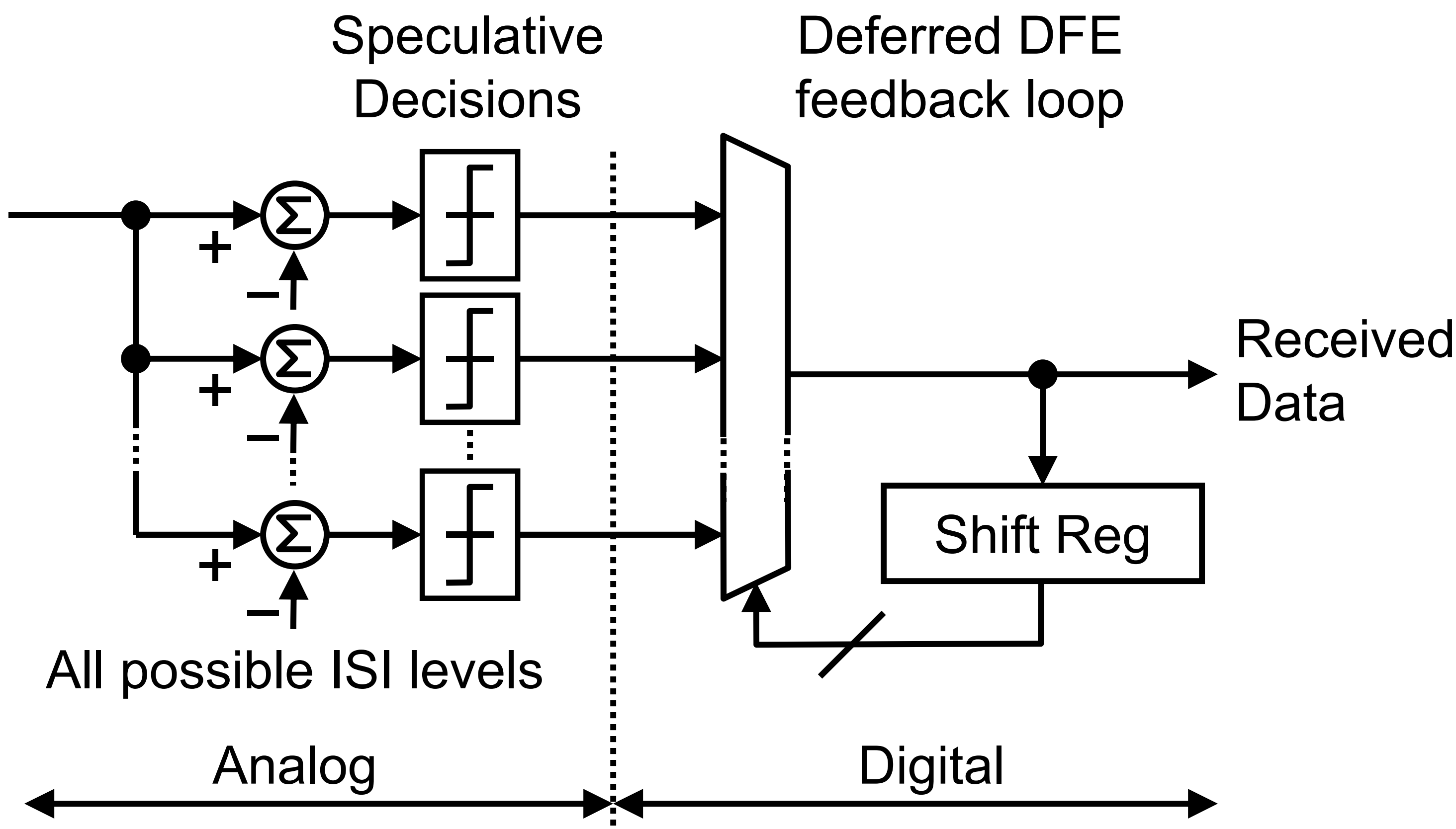
- Emulate ISI from previous decisions, and subtract it from input
- Example
  - N-tap DFE



ISI: Inter-Symbol Interference

Speculative DFE[13,14]

- Defer DFE feedback loop using speculative decisions



- Trade-off area/power for timing critical path

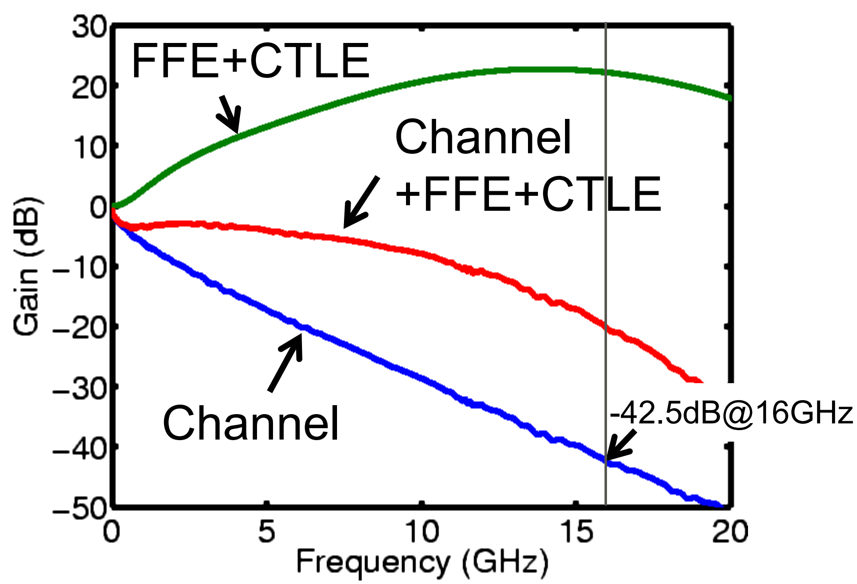
Outline

- Background
- State-of-the-art Equalizer for High-Speed I/O
  - Conventional High-Frequency Equalizers
  - Low-Frequency Equalizer
    - Performance Limit of Conventional High-Frequency Equalizers
    - Architecture of Low-Frequency Equalizer
    - Effect of Low-Frequency Equalizer
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
- Implementation and Evaluation Results
- Summary

Performance Limit of Conventional Equalizers

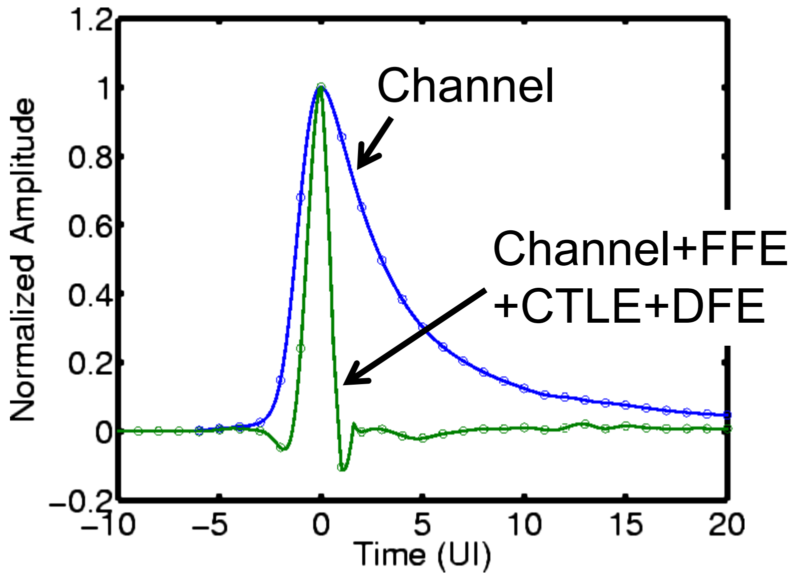
FUJITSU

Frequency-domain response



(Linear)

Time-domain pulse response

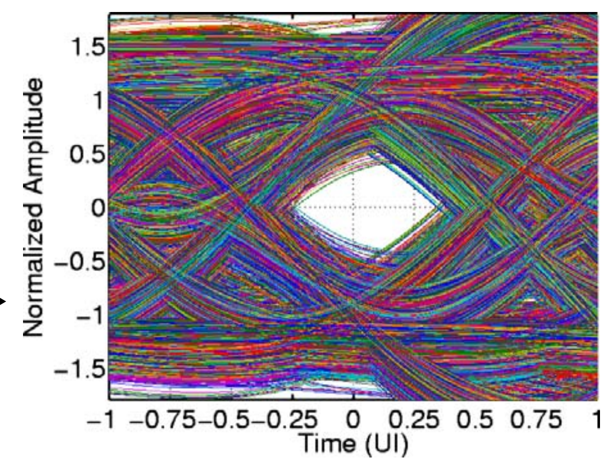


32Gbps, 4-tap FFE, 1st-order CTLE, 1-tap DFE

- EQ parameters are the best values

Why is this eye so bad? ⟶

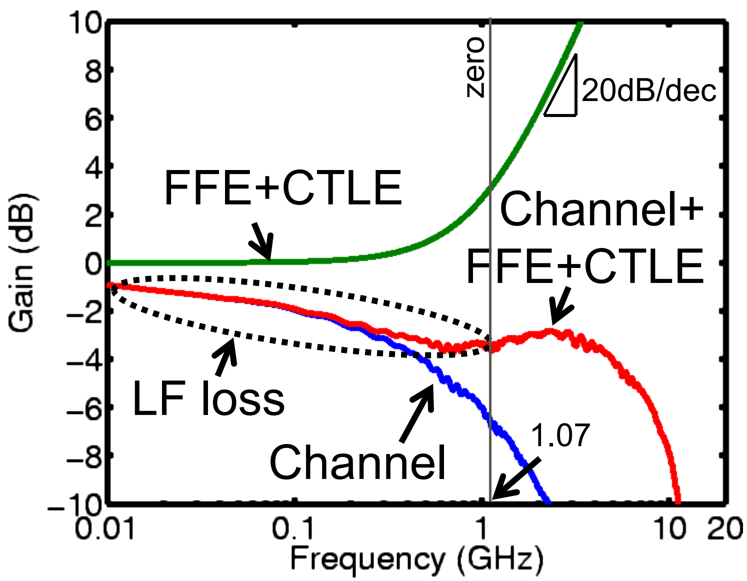
Eye diagram (PRBS31)



Uncompensated Low-Frequency Loss

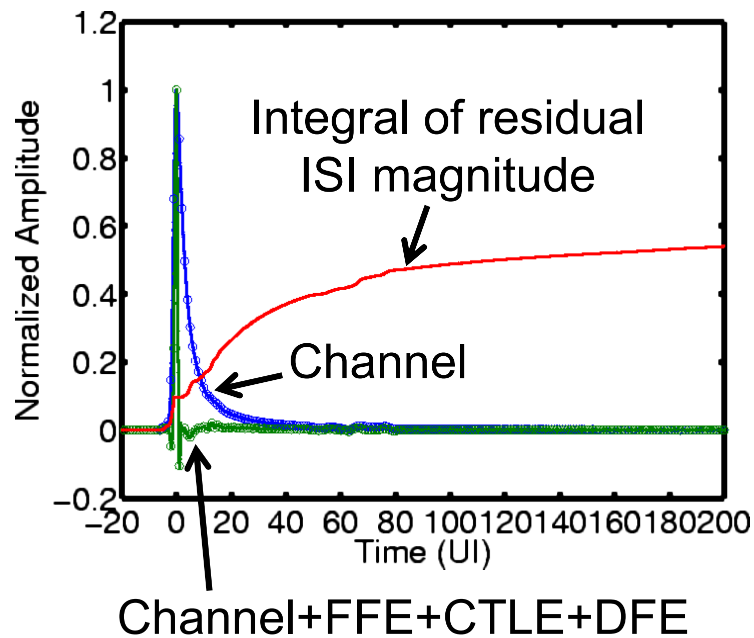
FUJITSU

Frequency-domain response



(Log)

Time-domain pulse response

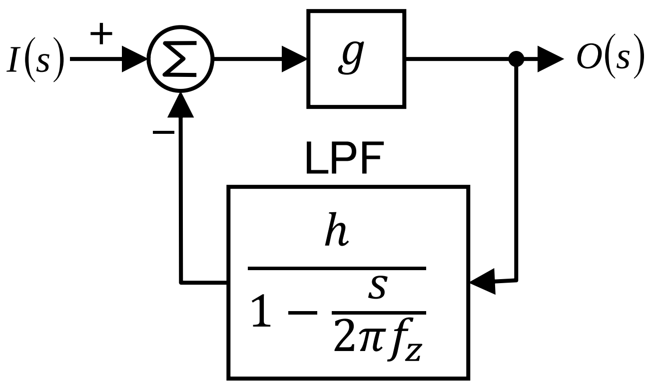


32Gbps, 4-tap FFE, 1st-order CTLE, 1-tap DFE

- Conventional EQs cannot compensate for low-frequency loss
  - CTLE and FFE have too steep slopes (20dB/dec)
    - If zero is moved to lower frequency, too much gain at high frequency
  - DFE can compensate for only short-term ISI (i.e. high-frequency loss)

Low-Frequency Equalizer (LFE)[15,16]

- Amplify low-frequency by a small amount (compared to DC)
  - Closely spaced a pair of pole and zero in low frequency
  - A variant of CTLE for low frequency
  - Easy to implement in analog, but maybe difficult in digital
- Example
  - Feedback with LPF



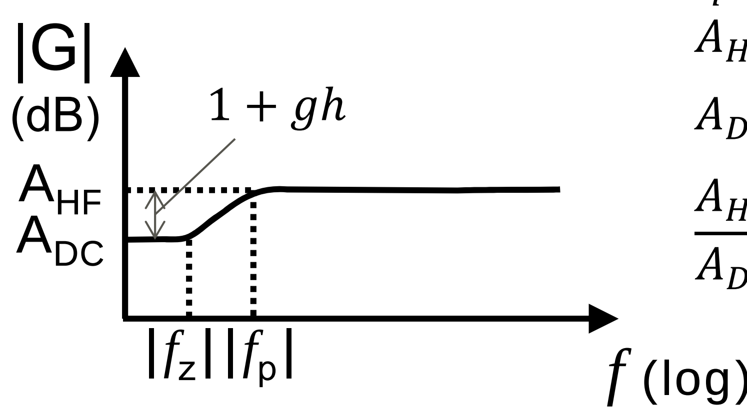
Feed-forward with LPF is an alternative option

Transfer Function in s domain:

$$G(s) = A_{DC}\frac{1-\frac{s}{2\pi f_z}}{1-\frac{s}{2\pi f_p}}$$

1 zero
1 pole

$$s = j\omega = j2\pi f$$



$$f_p = (1+gh)f_z$$

$$A_{HF} = g$$

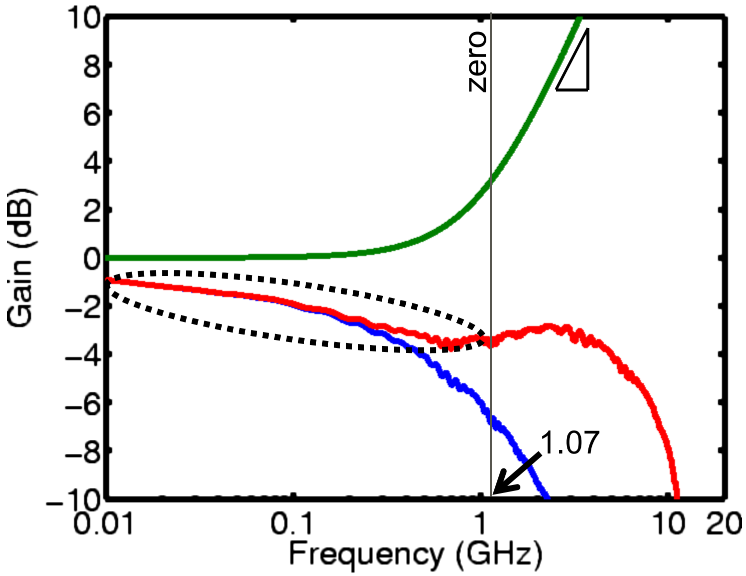
$$A_{DC} = \frac{g}{1+gh}$$

$$\frac{A_{HF}}{A_{DC}} = 1+gh$$

Effect of LFE in Frequency Domain

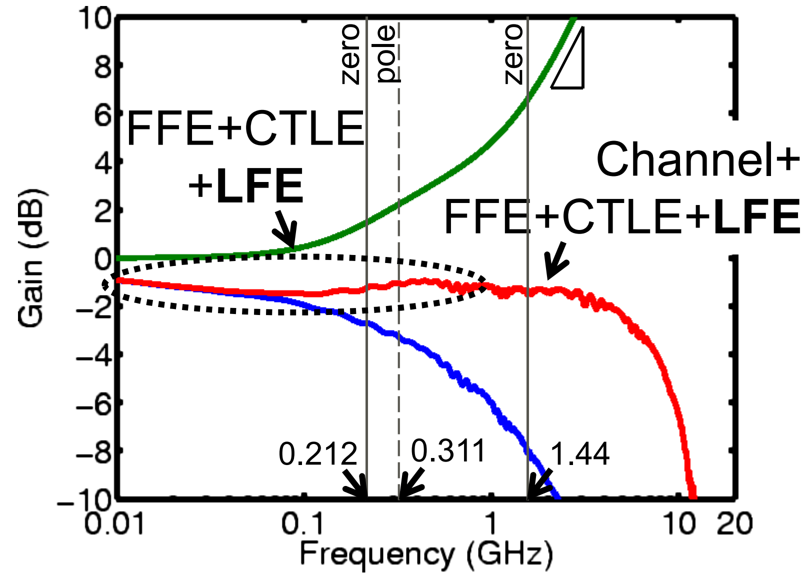
FUJITSU

Only Conventional

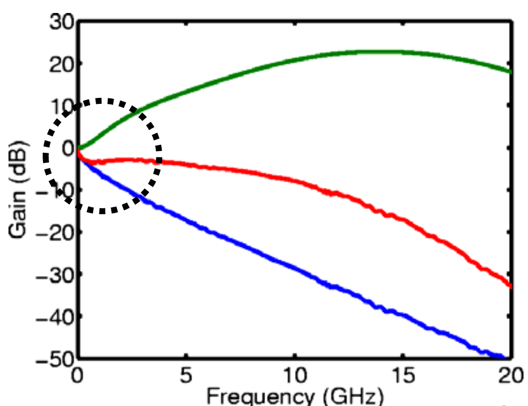


(Log)

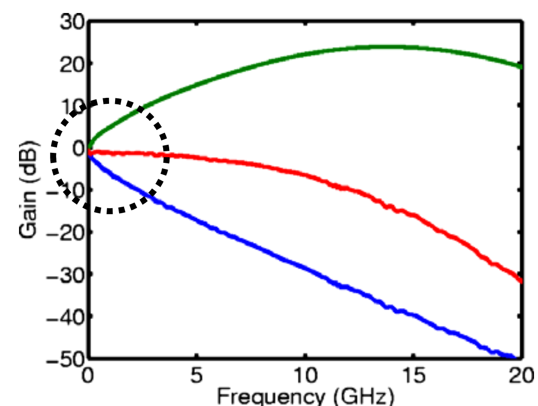
With LFE



(Log)



(Linear)

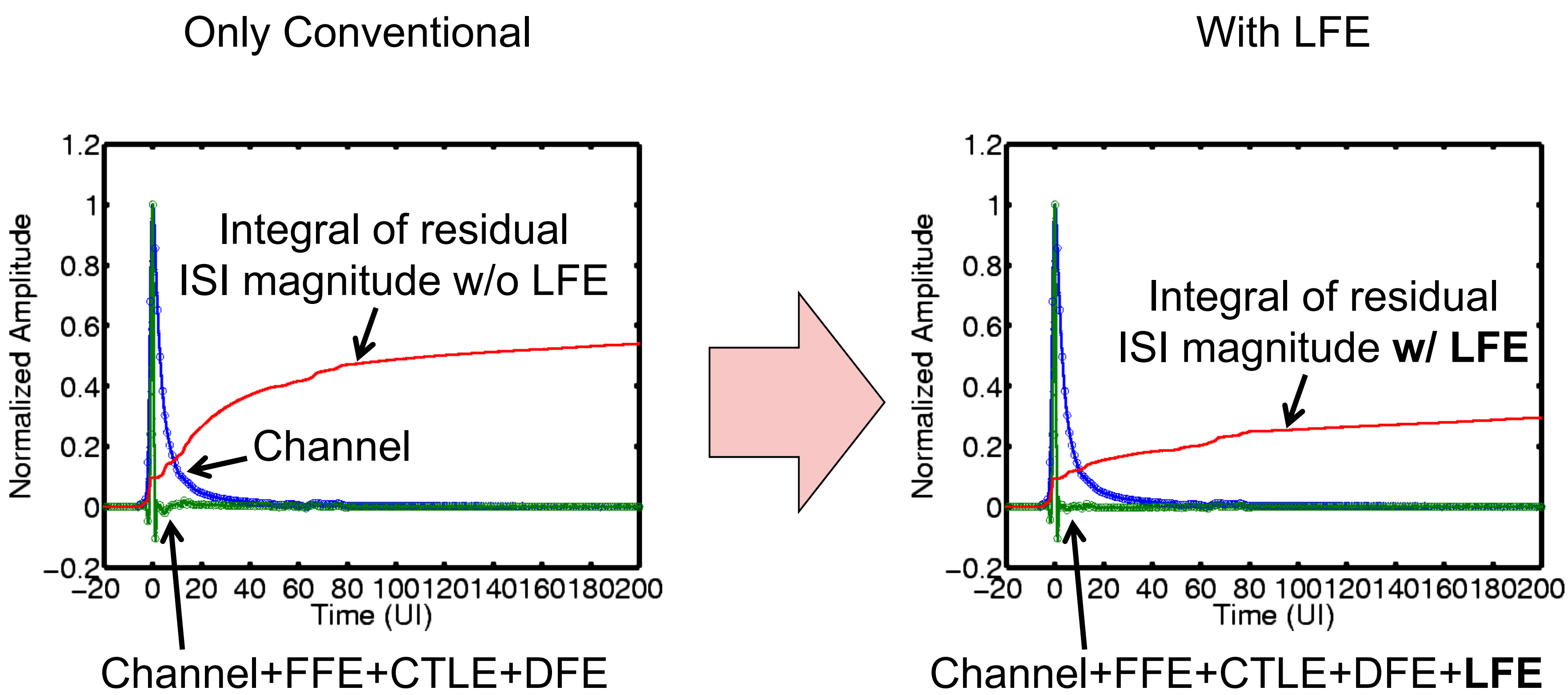


(Linear)

32Gbps, Chan. loss 42.5dB@16GHz
4-tap FFE, 1st-order CTLE, 1-tap DFE

Effect of LFE in Time Domain

FUJITSU

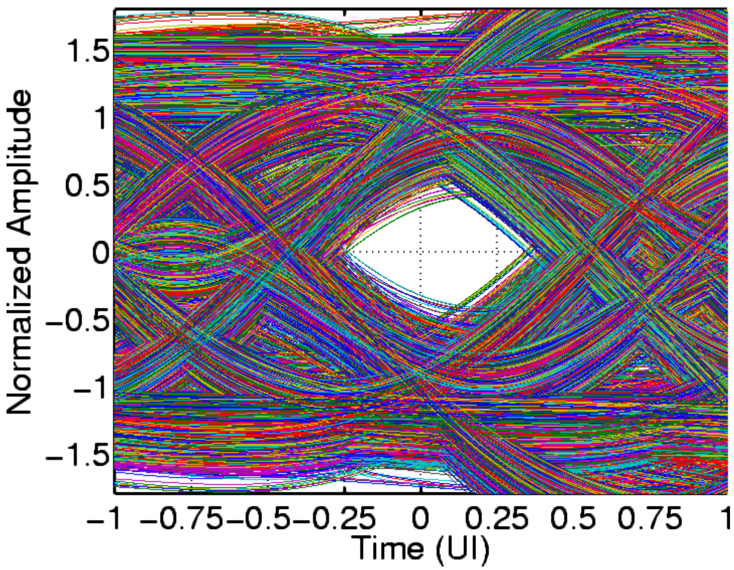


32Gbps, Chan. loss 42.5dB@16GHz
4-tap FFE, 1st-order CTLE, 1-tap DFE

Effect of LFE on Eye Diagram (PRBS31)

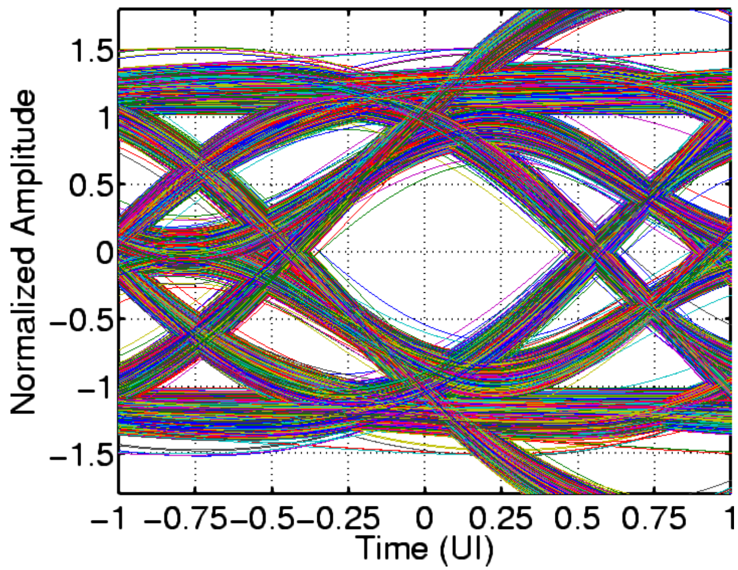
FUJITSU

Only Conventional



DDJ=0.42UI

With LFE



DDJ=0.21UI

32Gbps, Chan. loss 42.5dB@16GHz
4-tap FFE, 1st-order CTLE, 1-tap DFE

Outline

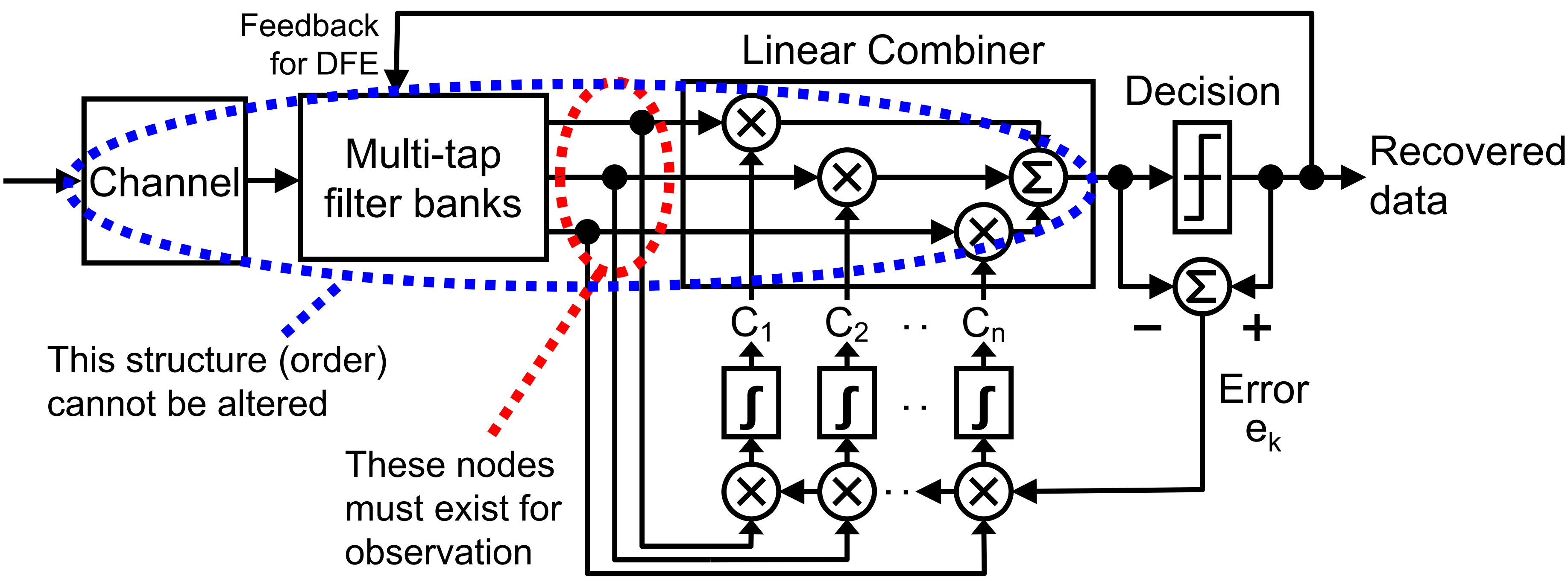
FUJITSU

- Background
- State-of-the-art Equalizer for High-Speed I/O
- Conventional Adaptive Equalizer Control for High-Speed I/O
  - Least Mean Square (LMS and SS-LMS)
  - Zero Forcing (ZF)
  - Max Eye Opening
  - Spectrum Matching
- Sign-based Zero-Forcing Adaptive Equalizer Control
- Implementation and Evaluation Results
- Summary

Least Mean Square† (LMS[17], SS-LMS[18])

FUJITSU

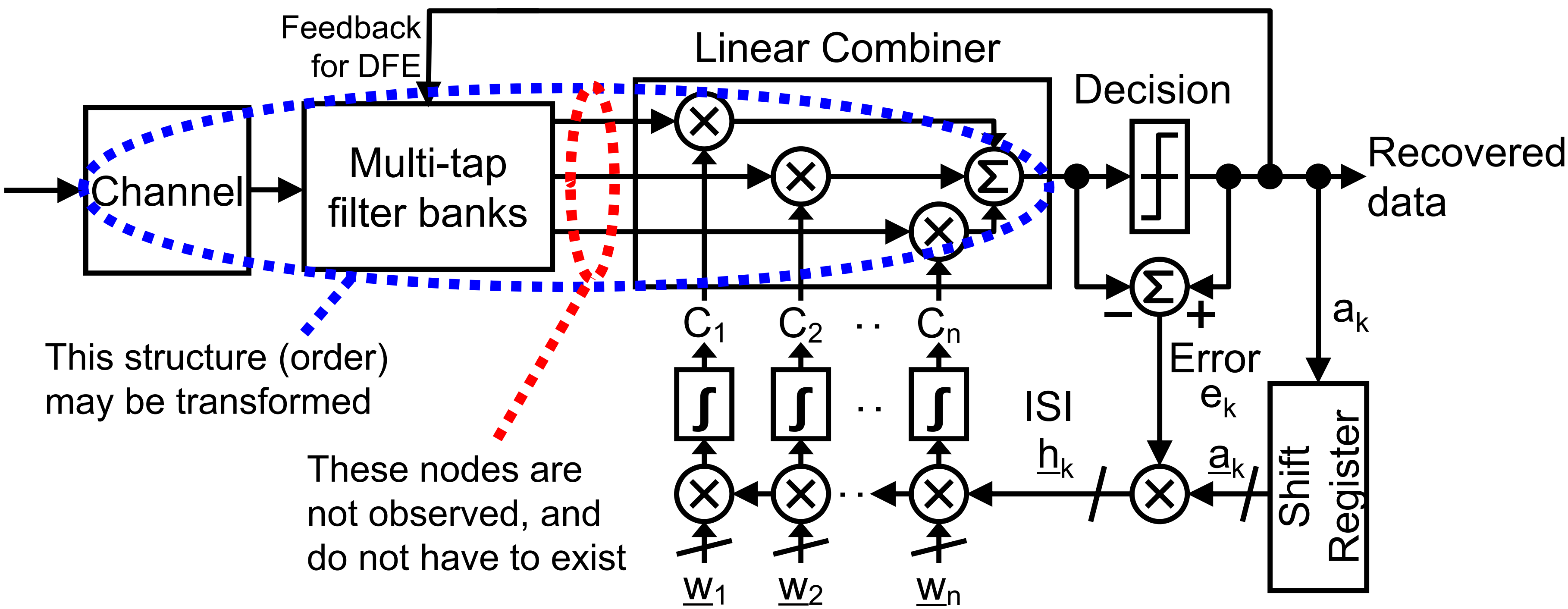
- Automatically achieve *Minimum Mean-Square Error* (Wiener Filter)
- Widely used in Digital Signal Processing (DSP)
- Strong restriction on filter structure (filter must be in below form)
  - Applicable to DFE, but often NOT to CTLE or LFE
  - NOT applicable to Tx FFE



† A.k.a. Stochastic Steepest Descent Method

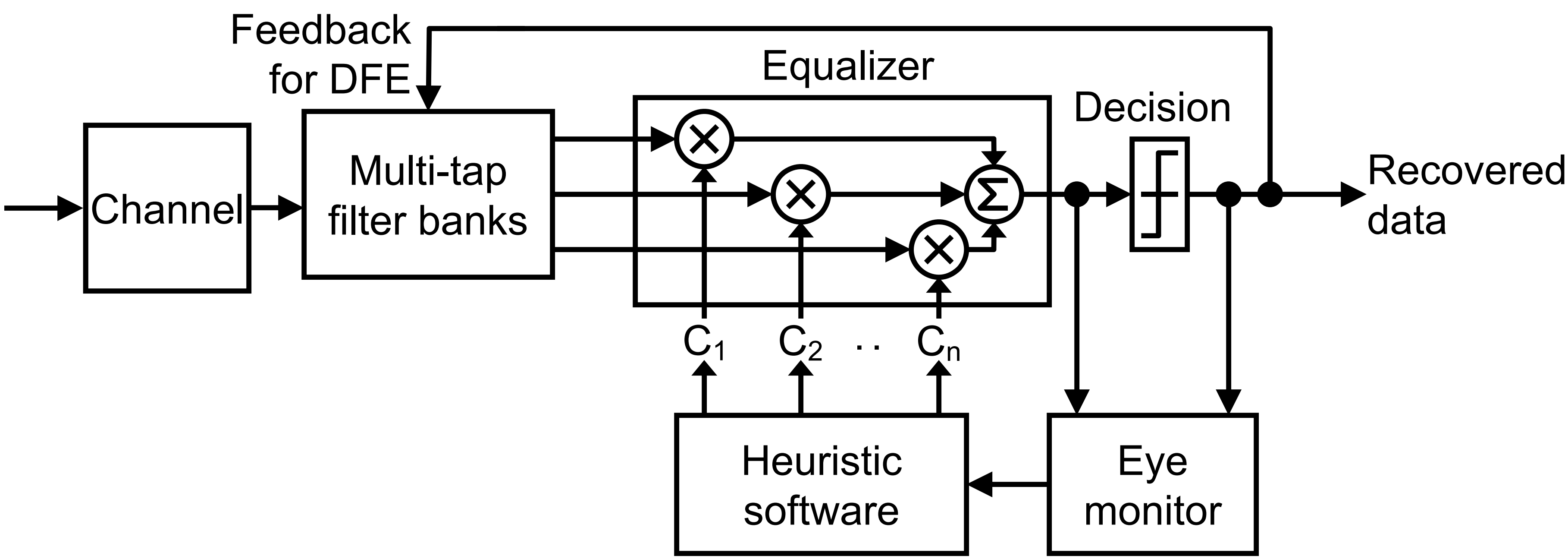
Zero Forcing (ZF)[19,20]

- Force *weighted* sum of ISI towards zero
  - Also capable to achieve almost *Minimum Mean-Square Error* (Wiener Filter)
    - For the target (worst) channel, with proper weight vectors (e.g. Jacobian Matrix)
      - Not optimal for other channels, but it is usually acceptable for wide range of variation
    - Equivalent to LMS, if applied to DFE
- Flexible filter structure
  - Applicable to CTLE, LFE and Tx FFE



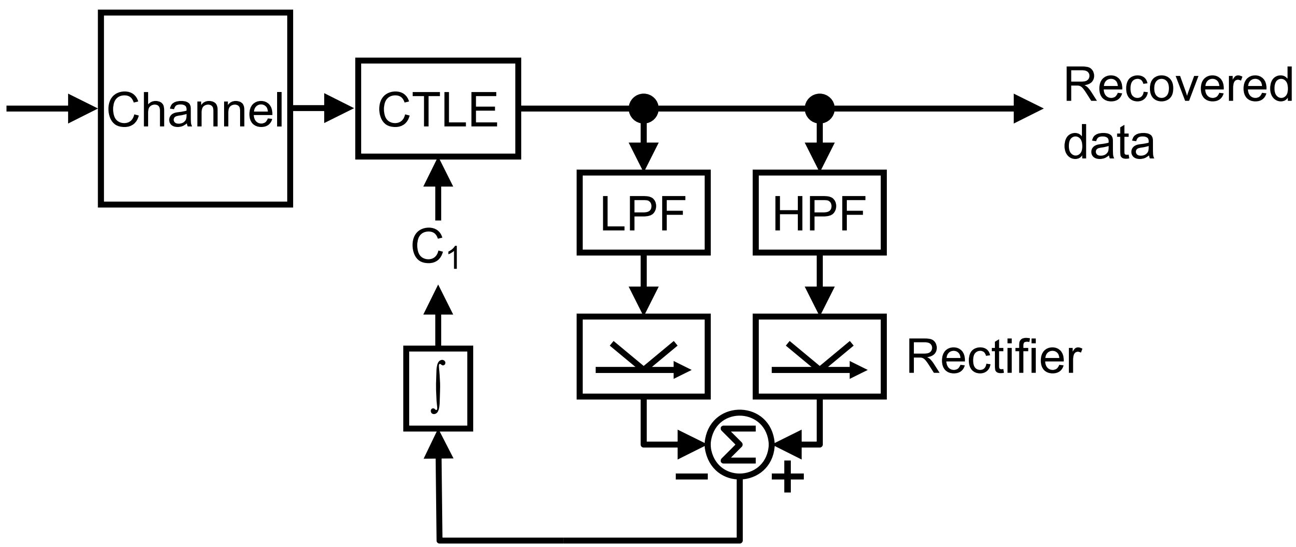
Max Eye Opening[21]

- Maximize eye opening by adjusting EQ parameters
- Flexible filter structure
- Slow or inaccurate
  - Similar eyes for slightly different parameters must be compared
  - Precision eye measurement takes quite a long time



Spectrum Matching[3,6]

- Force imbalance of spectrum towards zero
- Options to measure imbalance of spectrum
  - Multiple filters with different bands (e.g. LPF and HPF)
  - Slicer may be optionally used to generate the reference
  - Edge slew rate or pulse width may be used instead of spectrum
- Difficult to control more than one parameter
- Only for CTLE



Outline

- Background
- State-of-the-art Equalizer for High-Speed I/O
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
  - Problems of Conventional Adaptive Equalizer Control
  - Pattern Filtering
  - Convolution and De-convolution of ISI
  - Sign-based Zero-Forcing
  - Extension of S-ZF for Low-Frequency Equalizer
- Implementation and Evaluation Results
- Summary

Problems of Conventional Adaptive EQ Control

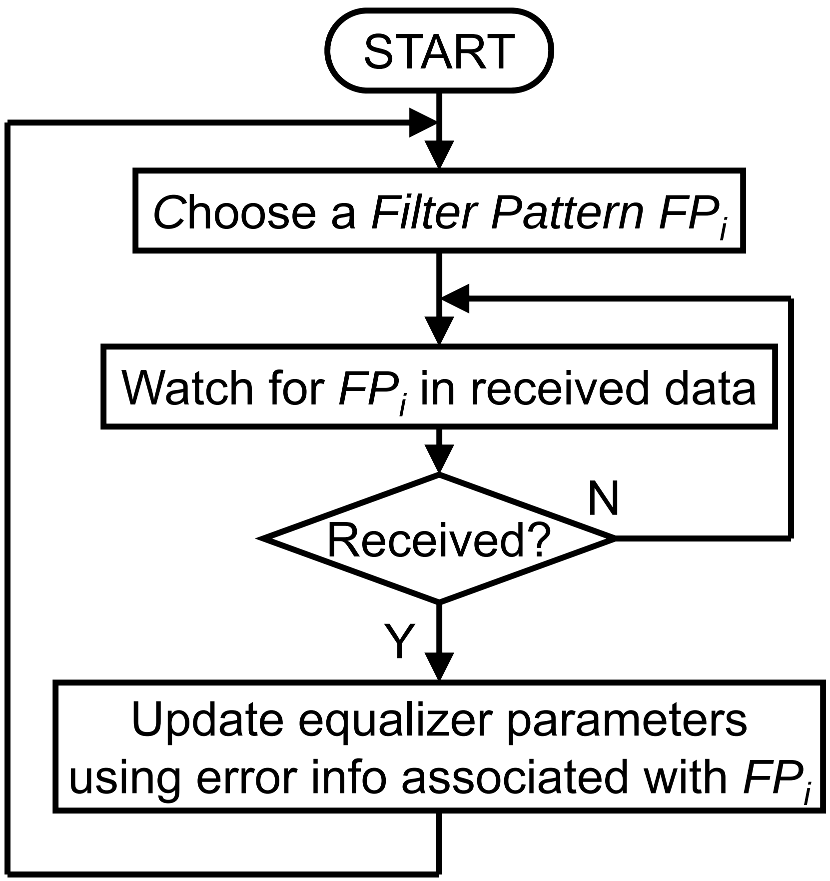
- Need random data
  - If data is not random, equalizer parameter can drift
  - Some wireline standards use 8B10B code
    - With 8B10B, data sequence can be periodic such as continuous 1010
    - Idle sequence in 8B10B has limited randomness
- Limited flexibility or accuracy (except ZF)
  - LMS/SS-LMS easily achieve MMSE, but are not flexible
  - Max Eye Opening is flexible, but inaccurate or slow
  - Spectrum Matching is not flexible
  - ZF is attractive, because it is flexible and able to achieve almost MMSE
    - But not well studied in DSP context, because LMS is better than ZF for DSP
    - Conventional ZF for DSP requires ADC which we would like to avoid

Outline

- Background
- State-of-the-art Equalizer for High-Speed I/O
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
  - Problems of Conventional Adaptive Equalizer Control
  - Pattern Filtering
  - Convolution and De-convolution of ISI
  - Sign-based Zero-Forcing
  - Extension of S-ZF for Low-Frequency Equalizer
- Implementation and Evaluation Results
- Summary

Pattern Filtering[22] (1/3)

- Do not passively use all received error information
- Actively choose error information to use



Pattern Filtering (2/3)

- Keep watching for the selected *Filter Pattern* FP_i (no timeout)
  - If the *Filter Pattern* FP_i is missing in the sequence, just wait forever
    - The sequence will eventually change
    - Do not update EQ parameters, when spectrum may be inadequate
      - Not halting updates for non-random data may cause parameter drift

- *Pattern Filtering* works with limited random data
  - For mostly periodic patterns, adaptation works slowly but steadily by catching limited random data
    - E.g. Ethernet frame with short random header and long payload filled by periodic 8B10B data

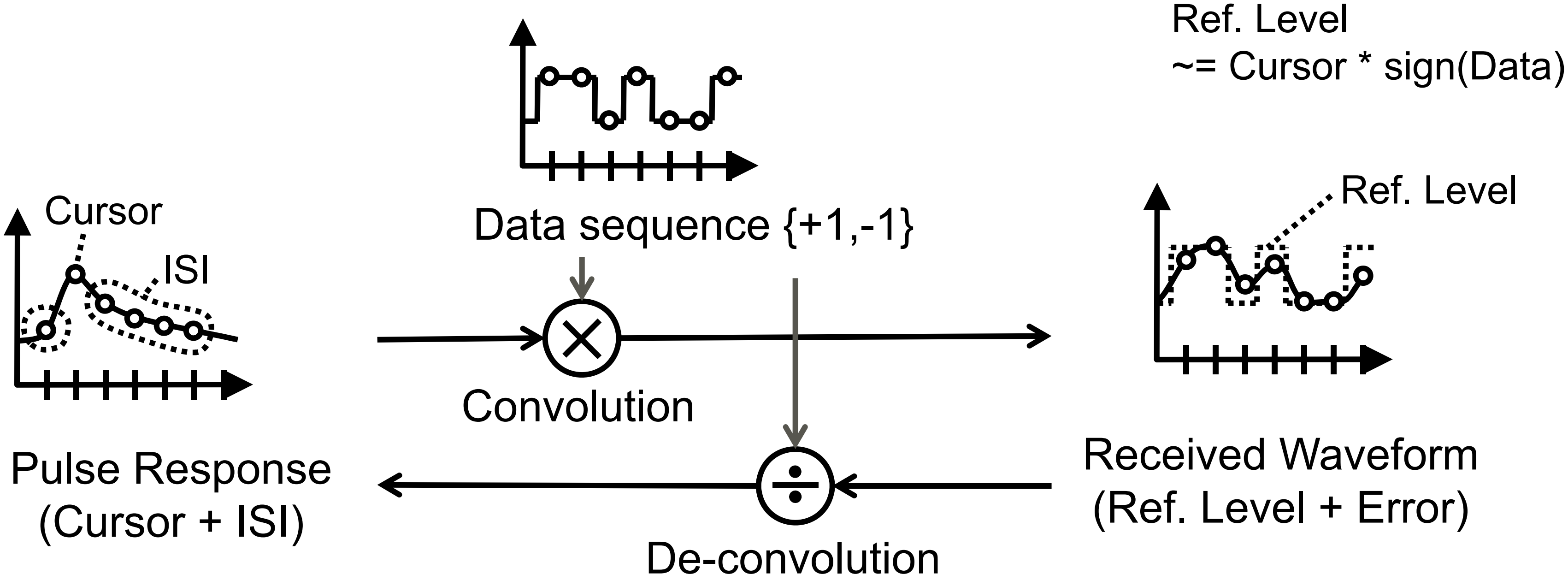
Pattern Filtering (3/3)

- Two options to choose a *Filter Pattern* FP_i
  - Randomly (similar to conventional adaptive control)[22]
    - Make conventional adaptive controls operable for non-random data
  - From a specific set of patterns, in some specific way[23]
    - Enable De-convolution of ISI and S-ZF adaptation scheme

Outline

- Background
- State-of-the-art Equalizer for High-Speed I/O
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
  - Problems of Conventional Adaptive Equalizer Control
  - Pattern Filtering
  - Convolution and De-convolution of ISI
  - Sign-based Zero-Forcing
  - Extension of S-ZF for Low-Frequency Equalizer
- Implementation and Evaluation Results
- Summary

Convolution and De-convolution of ISI



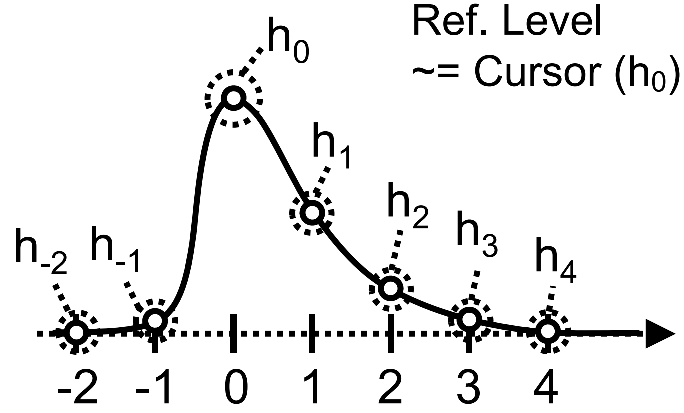
	Convolution	De-convolution
Time Domain	Convolution	De-convolution
	$A(f) \rightarrow \otimes \rightarrow C(f) = A \times B$, with $B(f)$	$A(f) = C \div B \leftarrow \div \leftarrow C(f)$, with $B(f)$
Frequency Domain	Multiplication	Division

Convolution : ISI × Data → Error

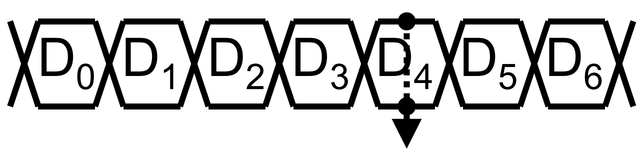
FUJITSU

Pulse response
= Cursor (h_0) + ISI

Ref. Level
~= Cursor (h_0) * sign(Data)



Data Sequence:



Ref. Level + Error (E_4)

Error is convolution of *Data* and *ISI*

$$\text{Error } E_4 = \text{sign}(D_6)*h_{-2} + \text{sign}(D_5)*h_{-1} + \cancel{(\text{sign}(D_4)*h_0 - \text{Ref. Level})} + \text{sign}(D_3)*h_1 + \text{sign}(D_2)*h_2 + \text{sign}(D_1)*h_3 + \text{sign}(D_0)*h_4$$

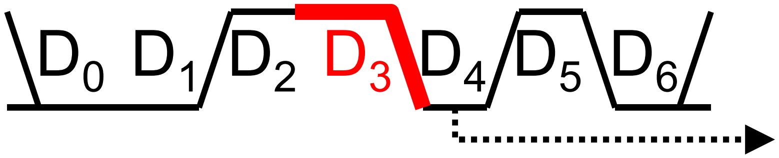
$\text{sign}(D_n) : \{+1, -1\}$

De-convolution : ISI ← Error ÷ Data[23]

FUJITSU

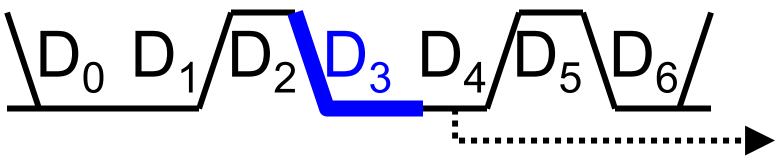
ISI is de-convolution of *Data* out of *Error*

FP0: 0 0 1 1 0 1 0



$$E_4^{FP0} = -\cancel{h_{-2}} + \cancel{h_{-1}} - \cancel{h_0} - \cancel{\text{Ref. Level}} + h_1 \cancel{+ h_2} \cancel{- h_3} \cancel{- h_4}$$

FP1: 0 0 1 0 0 1 0



$$E_4^{FP1} = -\cancel{h_{-2}} + \cancel{h_{-1}} - \cancel{h_0} - \cancel{\text{Ref. Level}} - h_1 \cancel{+ h_2} \cancel{- h_3} \cancel{- h_4}$$

FP: Filter Pattern

$$E_4^{FP0} - E_4^{FP1} = 2 * h_1$$

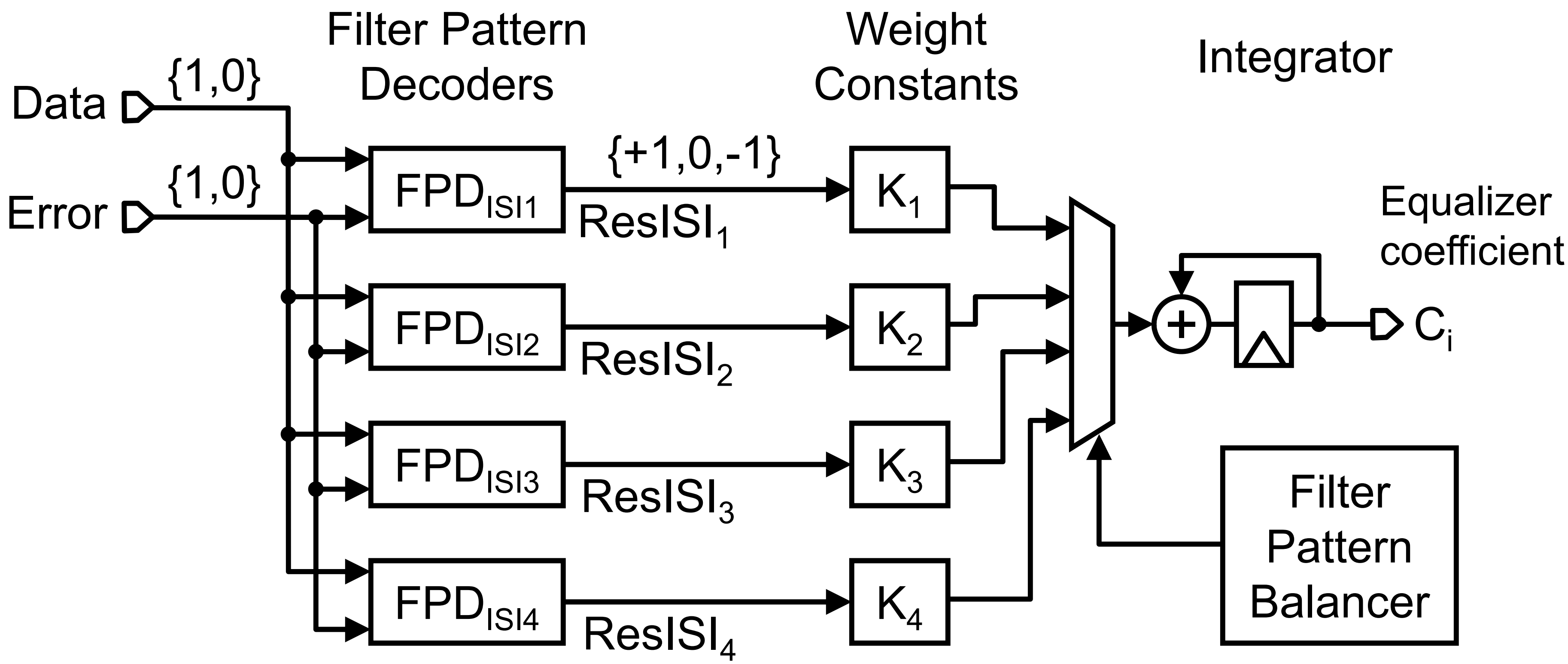
Residual ISI h_1 can be calculated as the difference between error E_4 values for FP0 and FP1 which differ only at D_3

Outline

- Background
- State-of-the-art Equalizer for High-Speed I/O
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
  - Problems of Conventional Adaptive Equalizer Control
  - Pattern Filtering
  - Convolution and De-convolution of ISI
  - Sign-based Zero-Forcing
  - Extension of S-ZF for Low-Frequency Equalizer
- Implementation and Evaluation Results
- Summary

Sign-based Zero-Forcing (S-ZF)[23]

FUJITSU



- FPD statistically de-convolves Data out of Error to ResISI$_n$
  - Average of {+1,-1} of ResISI$_n$ indicates quantity of residual ISI at n UI

- Force weighted sum of average ResISI$_n$ towards Zero

Sign-based ISI De-convolution by FPD

FUJITSU

- FPD performs $E_4^{FP0} - E_4^{FP1}$ statistically in a long term using *only error signs* without error quantities

Truth Table in FPD

<table>
<tr><th>Filter Pattern</th><th>D_0</th><th>D_1</th><th>D_2</th><th>D_3</th><th>D_4</th><th>D_5</th><th>D_6</th><th>E_4</th><th>$ResISI_1$
$(sign(h_1)=sign(E_4)*sign(D_3))$</th></tr>
<tr><td rowspan="2">FP0</td><td rowspan="4">0</td><td rowspan="4">0</td><td rowspan="4">1</td><td rowspan="2">1</td><td rowspan="4">0</td><td rowspan="4">1</td><td rowspan="4">0</td><td>1</td><td>+1</td></tr>
<tr><td>0</td><td>-1</td></tr>
<tr><td rowspan="2">FP1</td><td rowspan="2">0</td><td>1</td><td>-1</td></tr>
<tr><td>0</td><td>+1</td></tr>
</table>

  - Average $ResISI_1$ shows difference of E_4 between FP0 and FP1
  - $ResISI_1$ is correlation between D_3 and E_4 : same as conventional ZF which measures correlation between D_3 and E_4 for random data
- Data values other than D_3 are chosen a priori
  - Error value should NOT be always 1 or 0
  - Filter patterns should be always received during adaptation period

Key Operations in FPD and FPB

- Filter Pattern Decoder checks FP0/FP1 equally
  - To perform statistical subtraction correctly
  - Implemented by *alternately* watching for FP0 and FP1

- Filter Pattern Balancer checks multiple FPDs equally
  - To define adaptation characteristics only by weight const.
  - Implemented by watching for *FPDs randomly*

- FPD/B keep watching for the FP until it is received
  - *No timeout* to guarantee above statistics
  - Pattern tolerant
    - Will not drift for any non-random data sequence

Outline

- Background
- State-of-the-art Equalizer for High-Speed I/O
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
  - Problems of Conventional Adaptive Equalizer Control
  - Pattern Filtering
  - Convolution and De-convolution of ISI
  - Sign-based Zero-Forcing
  - Extension of S-ZF for Low-Frequency Equalizer
- Implementation and Evaluation Results
- Summary

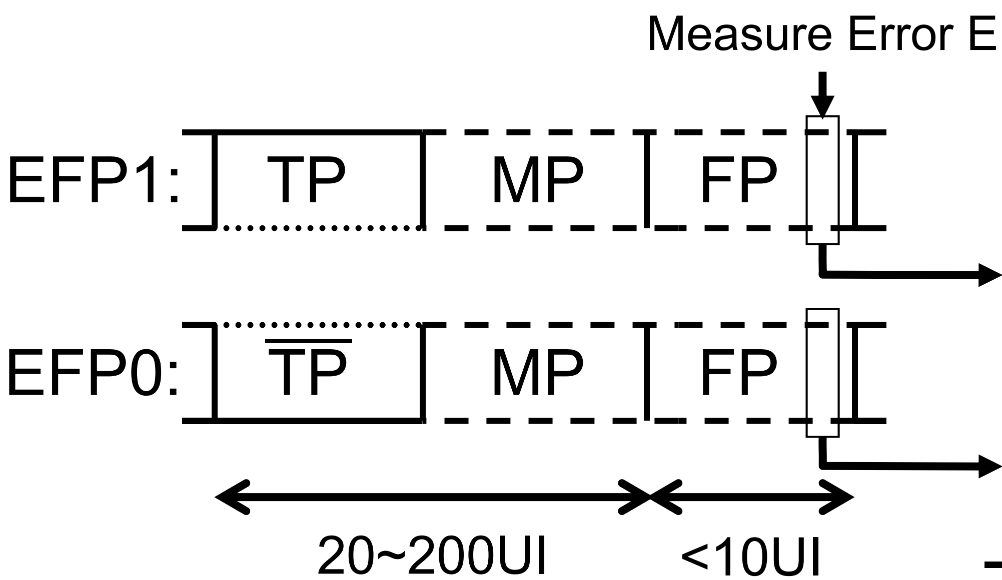
A Problem of Sign-based Zero Forcing

- Not applicable to Low-Frequency Equalizer
  - Filter Pattern must be very long to detect long-term ISI for LFE
    - LFE cancels long-term ISI in the range of 20~100 UI
  - Adaptation speed is too slow for Low-Frequency Equalizer
    - 50bit FP is received once every 31 hours for random data at 10Gb/s
    - 100bit FP is received once every 4×10^{12} years for random data at 10Gb/s

Extension of S-ZF for Low-Freq Equalizer[24]

- Basic idea:
  - Handle Long-term ISI collectively in an aggregate manner
    - ISI for each individual bit is similar and not important for long-term ISI
    - Low-frequency equalizer cancels long-term ISI collectively

Extended Filter Pattern (EFP)



h_{FP} : aggregate ISI from FP
h_{MP} : aggregate ISI from MP
h_{TP} : aggregate ISI from TP

$$E^{EFP1} = +\cancel{h_{FP}} + \cancel{h_{MP}} + \mathbf{h_{TP}}$$

$$E^{EFP0} = +\cancel{h_{FP}} + \cancel{h_{MP}} - \mathbf{h_{TP}}$$

$$E^{EFP1} - E^{EFP0} = 2 * \mathbf{h_{TP}}$$

- FP (Filter Pattern) : Fixed 0/1 sequence (balanced ISI)
  - Minimize h_{FP}
- MP (Middle Pattern) : Equal 0/1 count (balanced 0/1)
  - Minimize h_{MP}
- TP (Tail Pattern) : Non-equal 0/1 count (imbalanced 0/1)
  - Maximize h_{TP}

Example of Extended Filter Pattern

	Earlier		Later		
	Tail Pattern	Middle Pattern	Filter Pattern	Error	ResISI
	50 bits	20 bits	D_0~D_6	E_4	
EFP1	# of 1 >= 34 bits # of 0 <= 16 bits	# of 0 = 10 bits # of 1 = 10 bits	0 1 0 1 0 1 0	1	+1
				0	-1
EFP0	# of 0 >= 34 bits # of 1 <= 16 bits			1	-1
				0	+1

Probability to receive above EFP0 or EFP1 in random sequence

$$P = \sum_{k=0}^{16} \frac{C(50,k)}{2^{50}} \times \frac{C(20,10)}{2^{20}} \times \frac{1}{2^7} = 0.0077 \times 0.1762 \times 0.0078 = 1.06 \times 10^{-5}$$

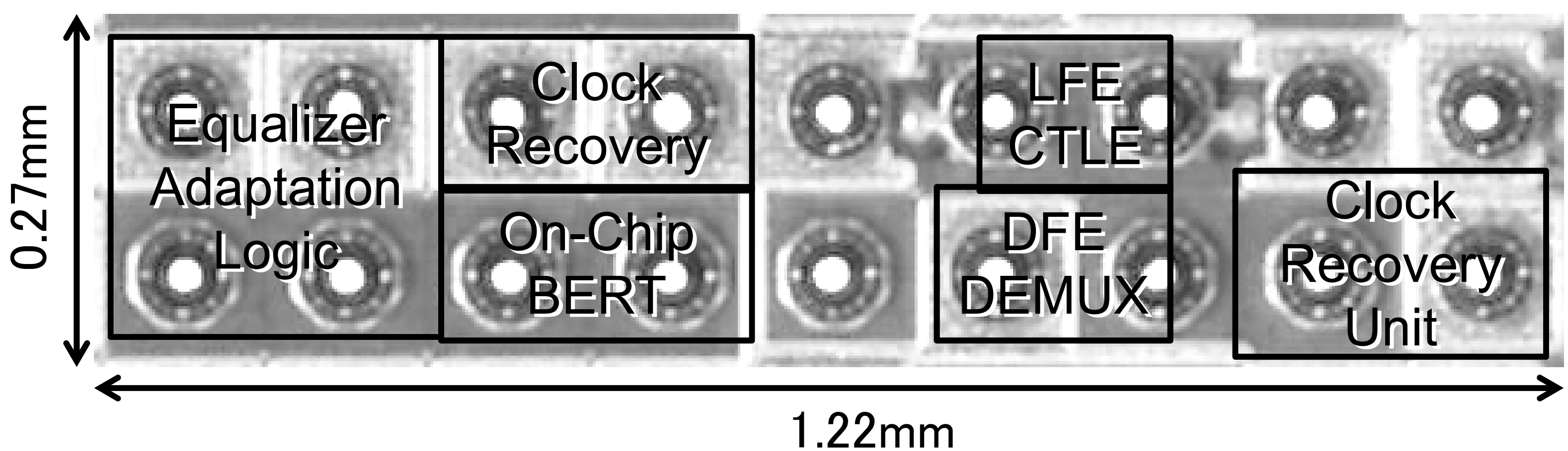
For example, if logic clock is 1GHz, we can detect > 10k EFPs per second.

Outline

- Background
- State-of-the-art Equalizer for High-Speed I/O
- Conventional Adaptive Equalizer Control for High-Speed I/O
- Sign-based Zero-Forcing Adaptive Equalizer Control
- Implementation and Evaluation Results
- Summary

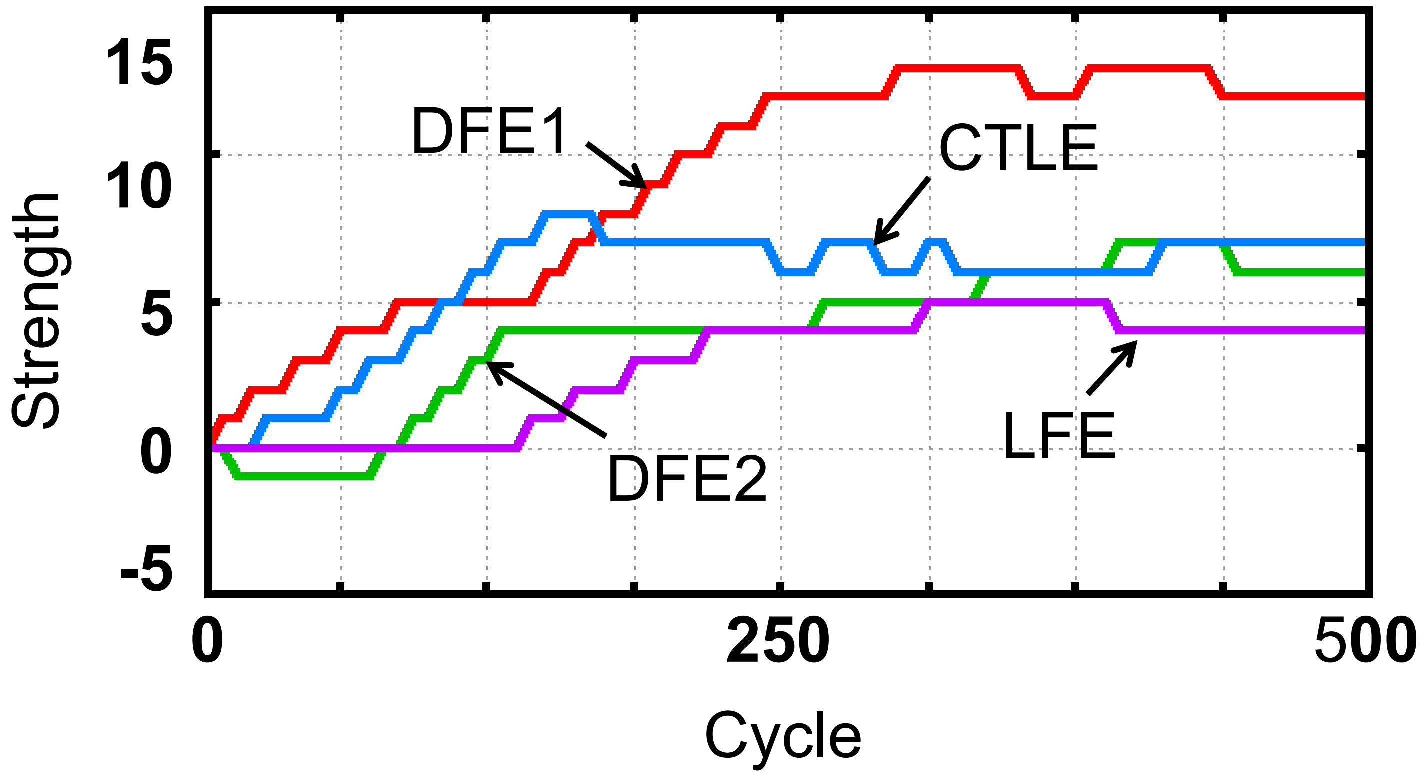
Implementation Example

- Equalizer: CTLE + LFE + 2-tap Speculative DFE
- Process technology: 28nm CMOS
- Data date: 25Gb/s
- Power supply: 1.0V
- Power consumption: 240mW (RX)
- Area: 0.33mm^2 (RX)



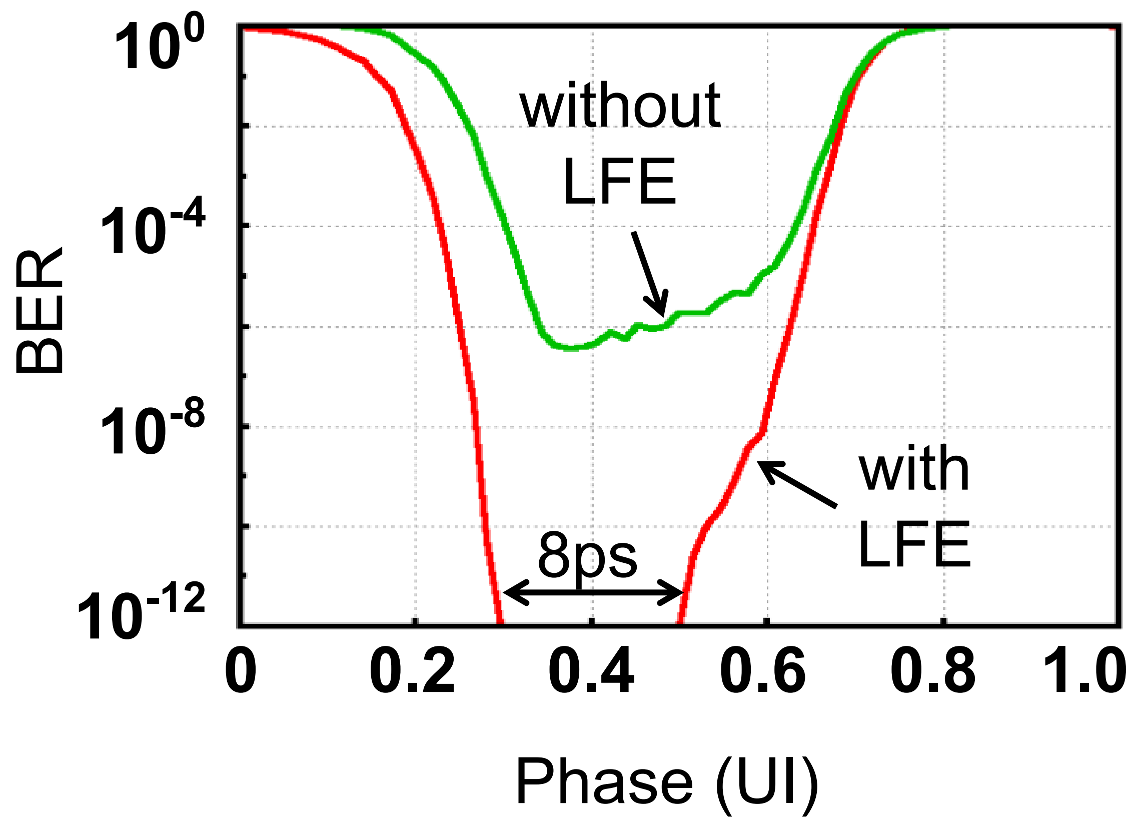
Measured Adaptation of Equalizer Parameters

FUJITSU



Convergence time < 5 msec in real-time operation.

Measured BER for PRBS31



Channel loss : 25dB at Nyquist Frequency

Summary

- LMS automatically achieves MMSE (Wiener Filter)
  - Because of this beauty of LMS, ZF is hardly used in DSP context
- However, ZF is much more attractive in mixed-signal HSIO context
  - ZF is more flexible than LMS regarding to mixed-signal circuit architecture
  - ZF is also capable to achieve almost MMSE regarding to observed ISI
    - For the target channel, with proper weight vectors
- S-ZF is enabled by accurate ISI detection using Filter Pattern
  - ISI is accurately detected by explicit de-convolution of Data out of Error
  - FP also solves the problem of parameter drift due to non-random data
- Low-frequency loss has significant effects and should be equalized
- S-ZF is extended for LFE by handling long-term ISI collectively

References

[1] S. Hall, H. L. Heck, “Advanced signal integrity for high-speed digital designs,” John Wiley & Sons, Inc., 2009.

[2] E. Bogatin, “Signal integrity—simplified,” Prentice Hall Professional Technical Reference, Pearson Education Inc., 2004.

[3] M. H. Shakiba, “A 2.5Gb/s adaptive cable equalizer,” ISSCC Dig. Tech. Papers, pp.396-397, Feb. 1999.

[4] W. Gai, et al., “A 4-channel 3.125Gb/s/ch CMOS transceiver with 30dB equalization,” VLSI Circuits Dig. Tech. Papers, pp.138-141, June 2004.

[5] H. Higashi, et al., “A 5-6.4Gb/s 12-channel transceiver with pre-emphasis and equalizer,” JSSC, vol.40, no.4, pp.978-985, Apr. 2005.

[6] J. Lee, “A 20-Gb/s Adaptive Equalizer in 0.13-um CMOS Technology,” JSSC, vol.41, no.9, pp. 2058-2066, Sep. 2006.

[7] S. Gondi and B. Razavi, “Equalization and Clock and Data Recovery Techniques for 10-Gb/s CMOS Serial-Link Receivers,” JSSC, vol.42, no.9, pp.1999-2011, Sep. 2007.

[8] R. W. Lucky, “Automatic Equalization for Digital Communication,” Bell Syst. Tech. J., vol.44, no.4, pp.547-588, Apr. 1965.

[9] W. J. Dally and J. Poulton, “Transmitter Equalization for 4-Gbps Signaling,” IEEE Micro, Vol.17, No.1, pp.48-56, Jan. 1997.

[10] R. F.-Rad, et al., “A 0.3-um CMOS 8-Gb/s 4-PAM Serial Link Transceiver,” JSSC, Vol.35, No.5, pp.757-764, May 2000.

[11] M. E. Austin, “Decision-Feedback Equalization for Digital Communication over Dispersive Channels,” M.I.T. Lincoln Lab., Tech. Rep. 437, Aug. 1967.

References

[12] C. A. Belfiore and J. H. Park, Jr., “Decision Feedback Equalization,” Proc. IEEE, Vol.67, No.8, pp.1143-1156, Aug. 1979.

[13] K. K. Parhi, “Pipelining in algorithms with quantizer loops,” IEEE Trans. Circuits Syst, vol.38, pp.745-753, Jul. 1991.

[14] S. Kasturia and J. H. Winters, “Techniques for high-speed implementation of nonlinear cancellation,” IEEE J. on Selected Areas in Communications, vol.9, no. 5, pp.711-717, Jun. 1991.

[15] J. Savoj, et al., “A Wide Common-Mode Fully-Adaptive Multi-Standard 12.5Gb/s Backplane Transceiver in 28nm CMOS,” VLSI Circuits Dig. Tech. Papers, pp.104-105, June 2012.

[16] S. Parikh, et al., “A 32Gb/s Wireline Receiver with a Low-Frequency Equalizer, CTLE and 2-Tap DFE in 28nm CMOS,” ISSCC Dig. Tech. Papers, pp.28-29, Feb. 2013.

[17] B. Widrow, et al., “Stationary and nonstationary learning characteristics of the LMS adaptive filter,” Proc. IEEE, vol.64, pp.1151-1162, Aug. 1976.

[18] S. Dasgupta, et al., “Sign-sign LMS convergence with independent stochastic inputs,” IEEE Trans. Inf. Theory, vol.36, pp.197-201, Jan. 1990.

[19] R. W. Lucky, “Automatic equalization for digital communication,” Bell System Technical Journal, vol.44, pp.547-588, Apr. 1965.

[20] J. W. M. Bergmans, “Digital Baseband Transmission and Recording,” Boston, MA, Kluwer Academic Publishers, 1996.

[21] K. Krishna, et al., “A multigigabit backplane transceiver core in 0.13-um CMOS with a power-efficient equalization architecture,” JSSC, vol.40, no.12, pp.2658-2666, Dec. 2005.

References

[22] Y. Hidaka, et al., “A 4-channel 3.1/10.3Gb/s transceiver macro with a pattern-tolerant adaptive equalizer,” ISSCC Dig. Tech. Papers, pp. 442-443, Feb. 2007.

[23] Y. Hidaka, et al., “A 4-channel 1.25-10.3 Gb/s backplane transceiver macro with 35dB equalizer and sign-based zero-forcing adaptive control,” JSSC, vol.44, no.12, pp.3547-3559, Dec. 2009.

[24] T. Nakao, et al., “An Equalizer-Adaptation Logic for a 25-Gb/s Wireline Receiver in 28nm CMOS,” ASSCC Dig. Tech. Papers, Nov. 2013.

shaping tomorrow with you