All-Digital Transmitter

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All-Digital Transmitter

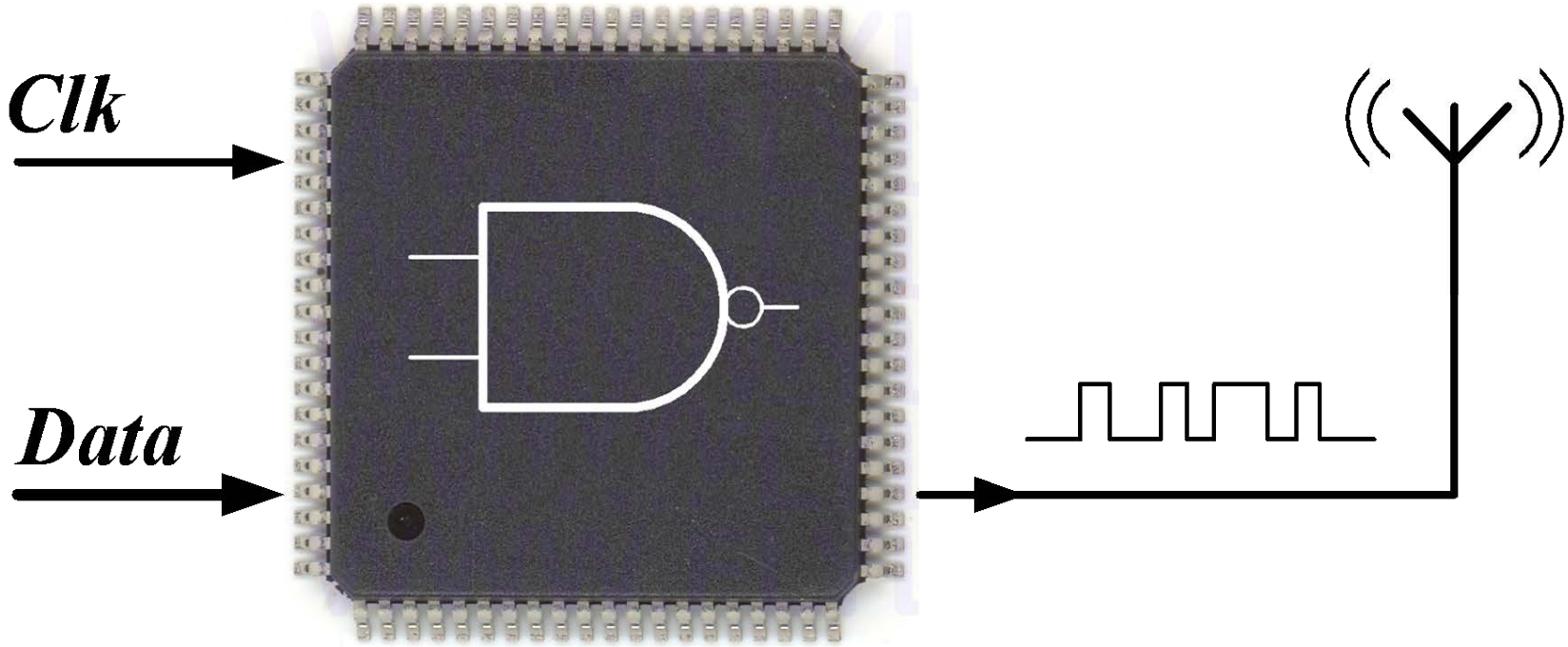
Presentation outline

- Theoretical overview of the proposed techniques:
  - Direct All-Digital Synthesis
  - Spurs Reduction Using Dithering
  - All-Digital modulation techniques
  - Nearly All-Digital analog data acquisition

- Live demo presentation:
  - FM radio transmitter
  - AM radio transmitter

➢This is the first implementation of a practical and purely digital rf transmitter.

What is an All-Digital Transmitter?



- Radio transmitter with (ideally) *no* analog components.
- Based on Direct All-Digital Frequency Synthesis & Modulation techniques.
- **Inputs**: A) Clock signal, B) Digital Data sequence
- **Output**: 1-bit digital sequence driving directly A) a (tuned) antenna, Or,
  B) a switching (class-D) power RF amplifier.

Why All Digital Transmitter?

Advantages

… compared to analog / mixed signal architectures

- Consumes significantly lower power
- Occupies significantly smaller chip area
- All advantages of digital circuit design
    - portability, scalability, reconfigurability, CAD tools

    (VHDL/Verilog - layout (APR) - test flow (BIST))
- Very short concept-to-market time.
- Compact, relatively simple, flexible architectures

Why *not* All Digital Transmitter?

Disadvantages

… compared to analog/ mixed signal architectures

- Worse Spurious Free Dynamic Range (SFDR) and/or noise floor
- Lower frequency range

Why *not* All Digital Transmitter?

Disadvantages

… compared to analog/ mixed signal architectures

- Worse Spurious Free Dynamic Range (SFDR) and/or noise floor
- Lower frequency range

→ *But with I.C. technologies downscaling,*

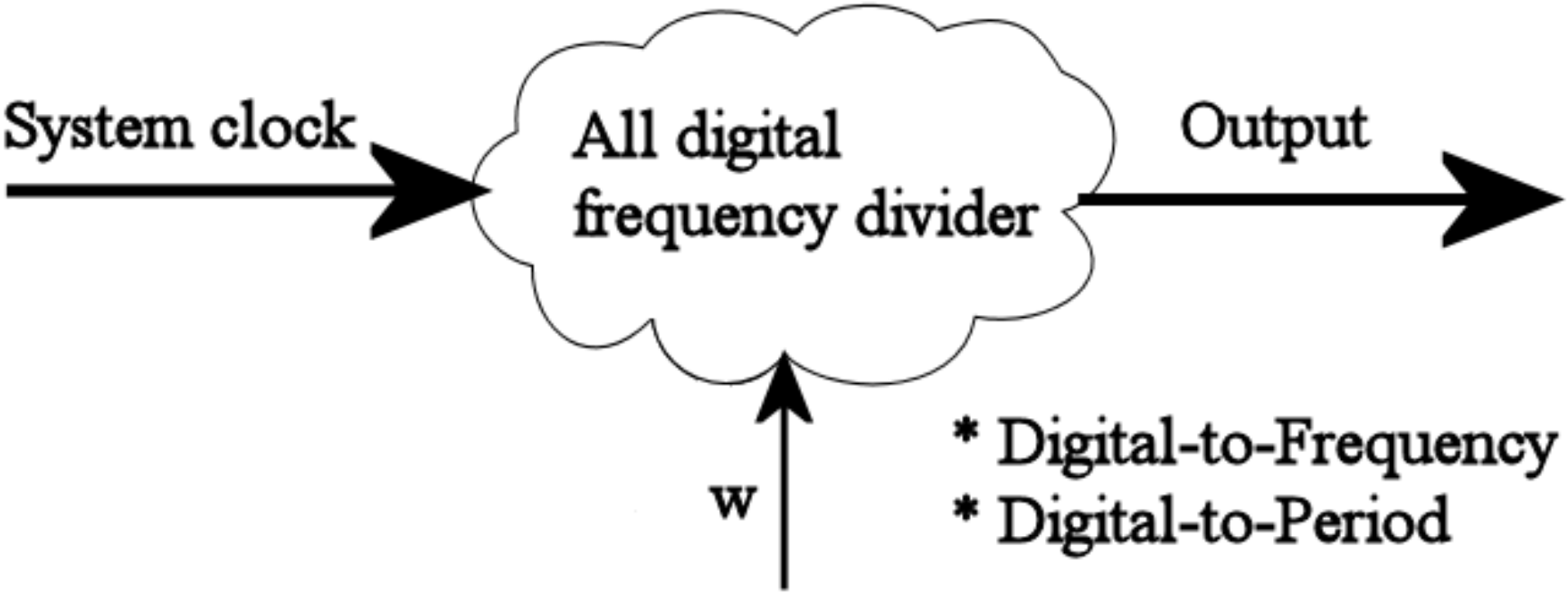
→ *Digital circuits become faster, of lower power, smaller.*

→ *Analog circuits become harder to design / migrate.*

→ *Also, higher operating frequencies improve SFDR and jitter !*

Direct All-Digital Synthesizer

… the core of all-digital transmitter

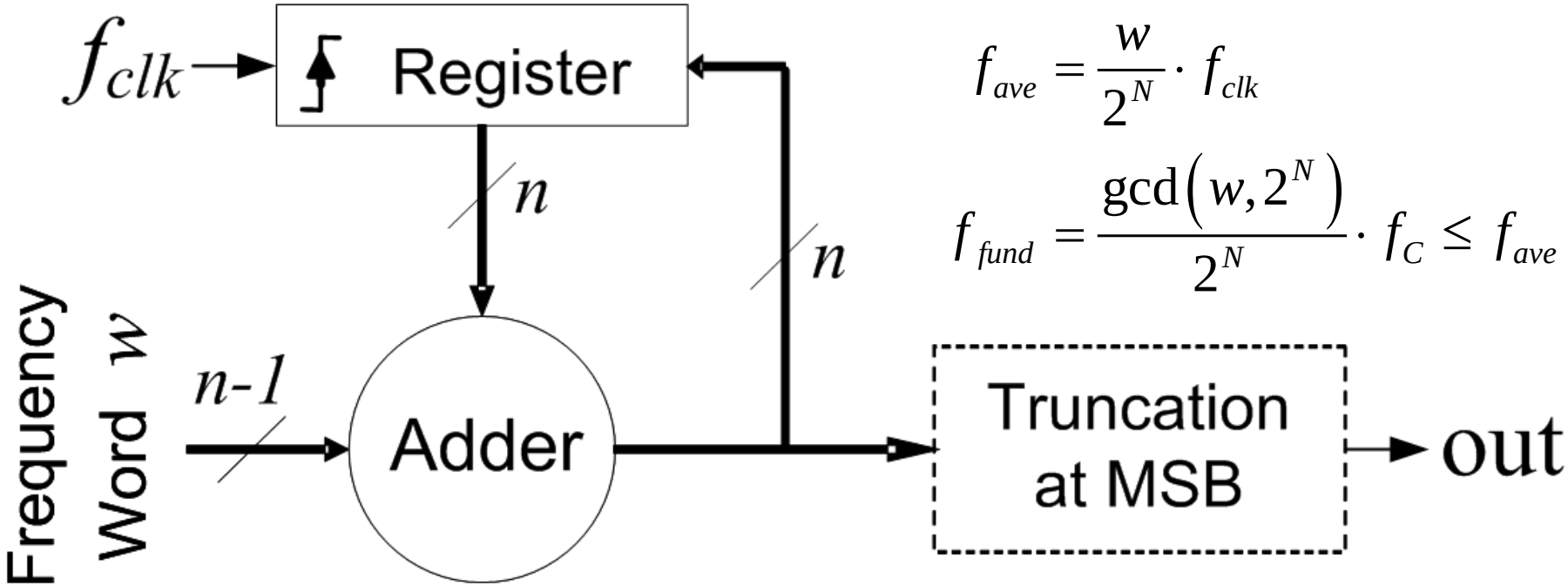


- Clock is fractionally divided to produce the output signal.
- Frequency Control Word (FCW) *w* sets the output Average Frequency
- Typical output is not a regular periodic signal

(Output flips value on System clock edges)

Pulse Direct Digital Synthesizer

..type of Direct All-Digital Synthesizer



$$f_{ave} = \frac{w}{2^N} \cdot f_{clk}$$

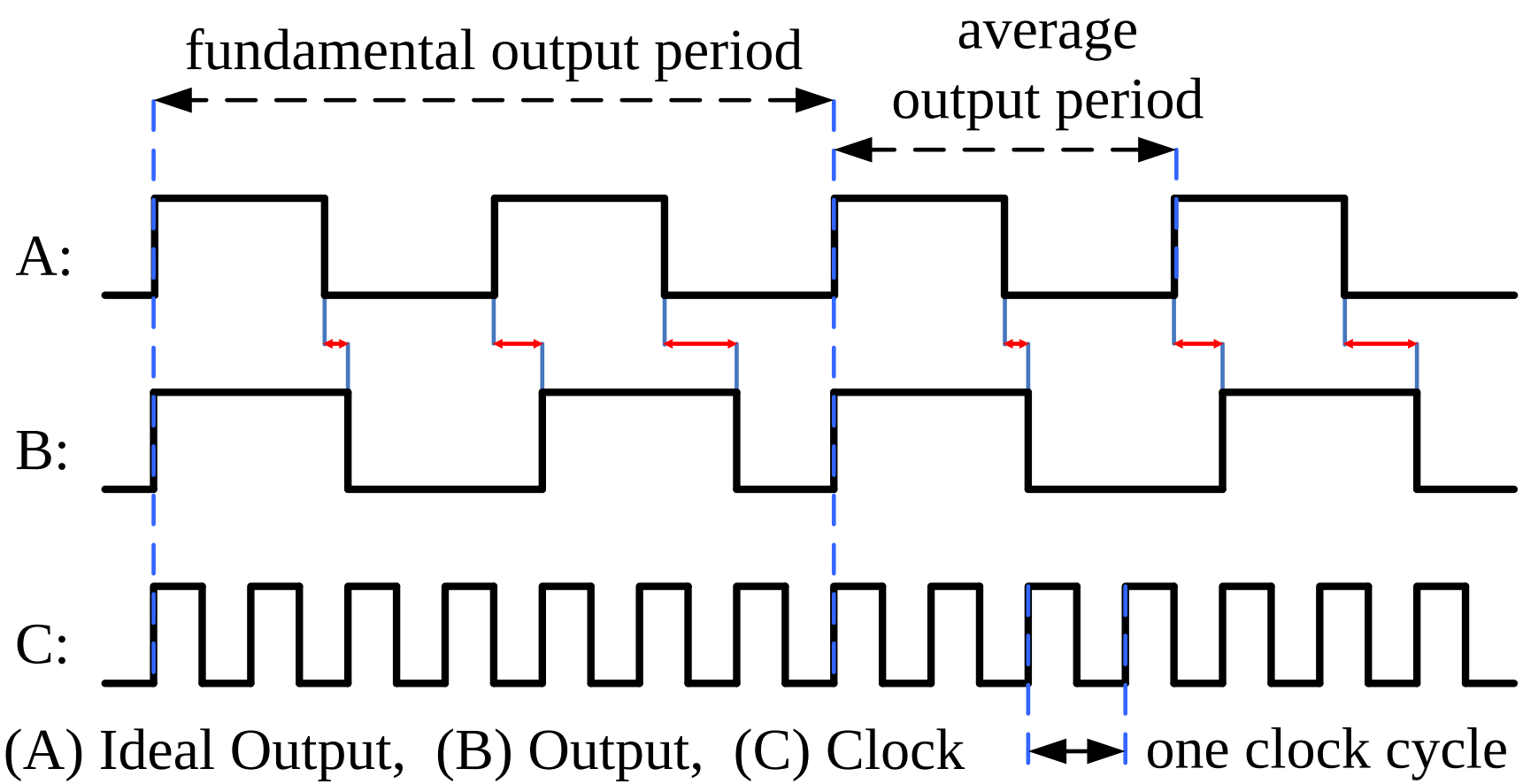
$$f_{fund} = \frac{\gcd\left(w, 2^N\right)}{2^N} \cdot f_C \leq f_{ave}$$

FCW is n-1 bit wide while a n-bit accumulator is used.

- V.S. Reinhardt, “Direct digital synthesizers”, *Technical Report*, Hughes Aircraft Co, Space and Communications Group, 1985.
- C. E. Wheatley, III and D. E. Phillips, “Spurious Suppression in Direct Digital Synthesizers”, Freq. Control Symp, May, 1981.

Pulse Direct Digital Synthesizer

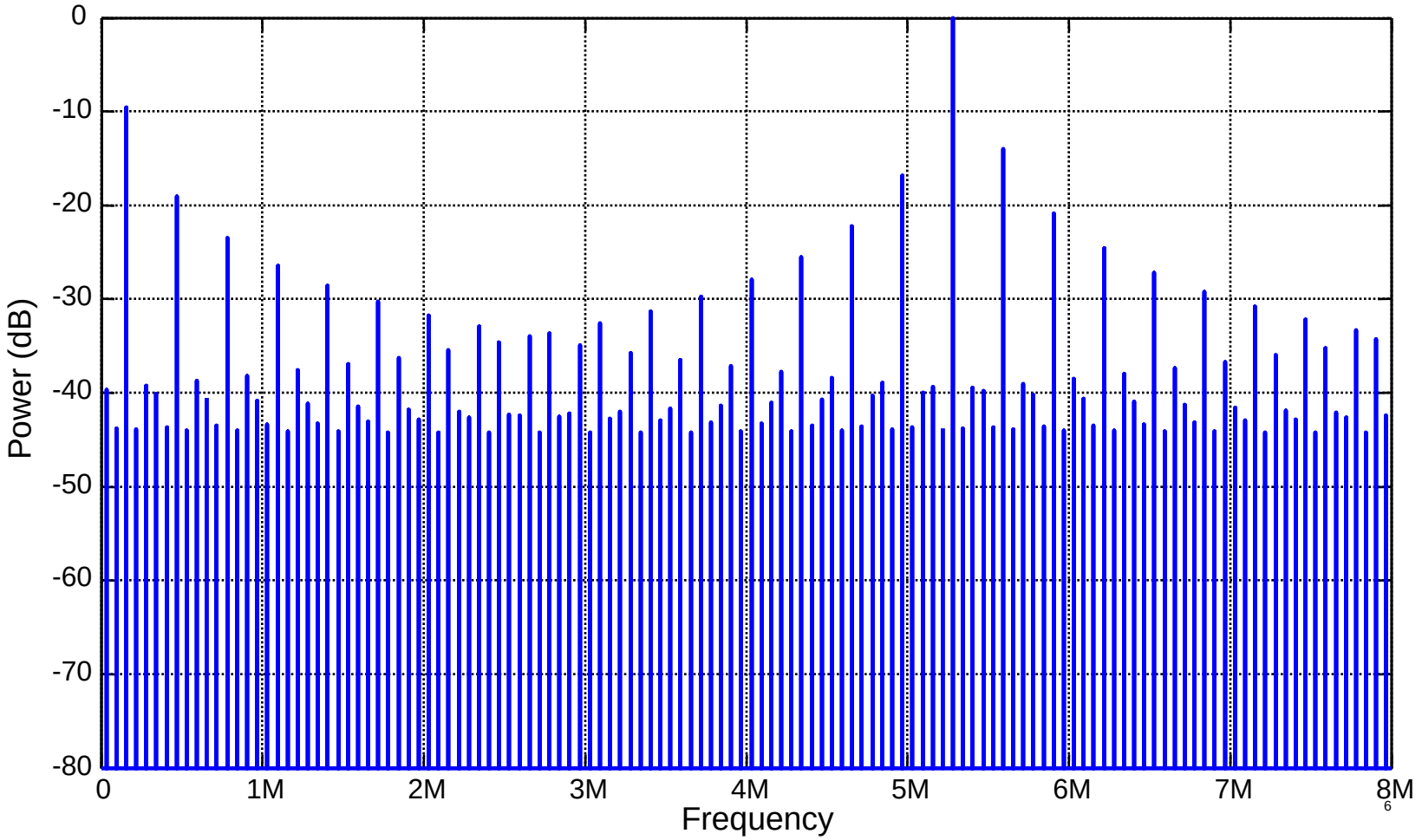
Output Timing Irregularity



- PDDS is a synchronous FSM, so…
- Output has timing irregularities (deterministic jitter) for most frequencies
- (deterministic) Jitter ≤ ½ Clock Cycle.

Pulse Direct Digital Synthesizer

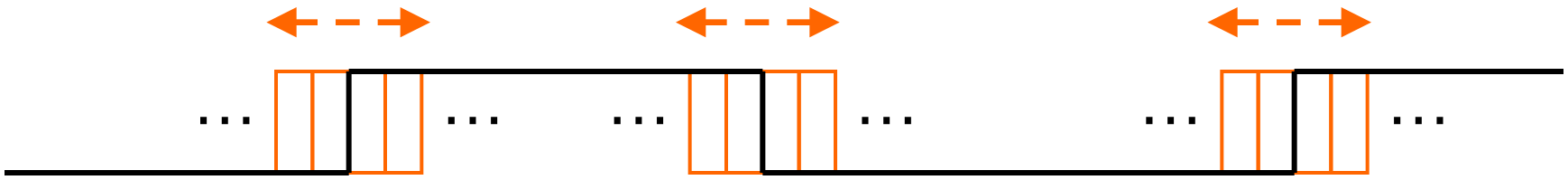
Output spectrum (*simulation* with a 16MHz clk)



- Timing irregularities imply many & strong (undesirable) frequency spurs!

Spurs Suppression using Dithering

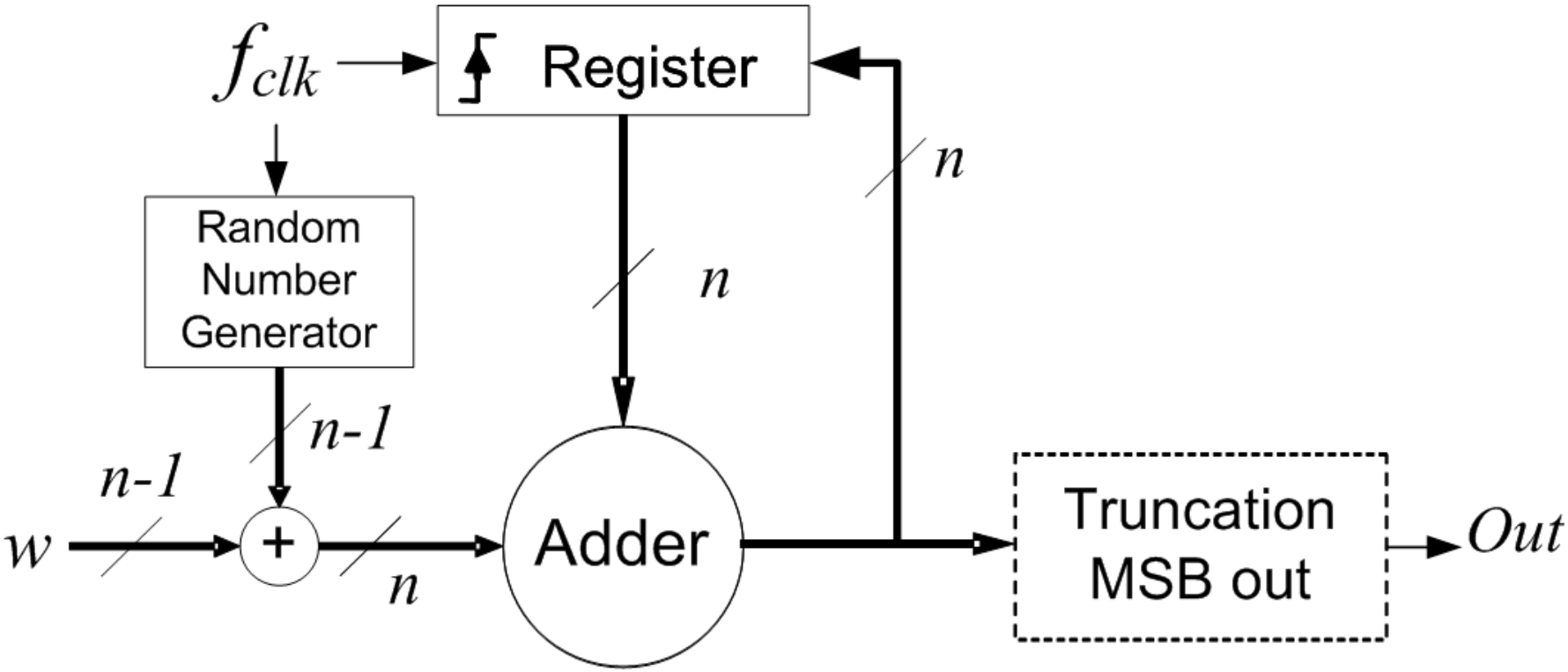
Edge Positions (random) variations



- Output is still a **pulse** sequence of the same average frequency.
- The power of the spurs spreads in the frequency domain.
- Output is not periodic anymore.

PDDS with Frequency Dithering

Block diagram

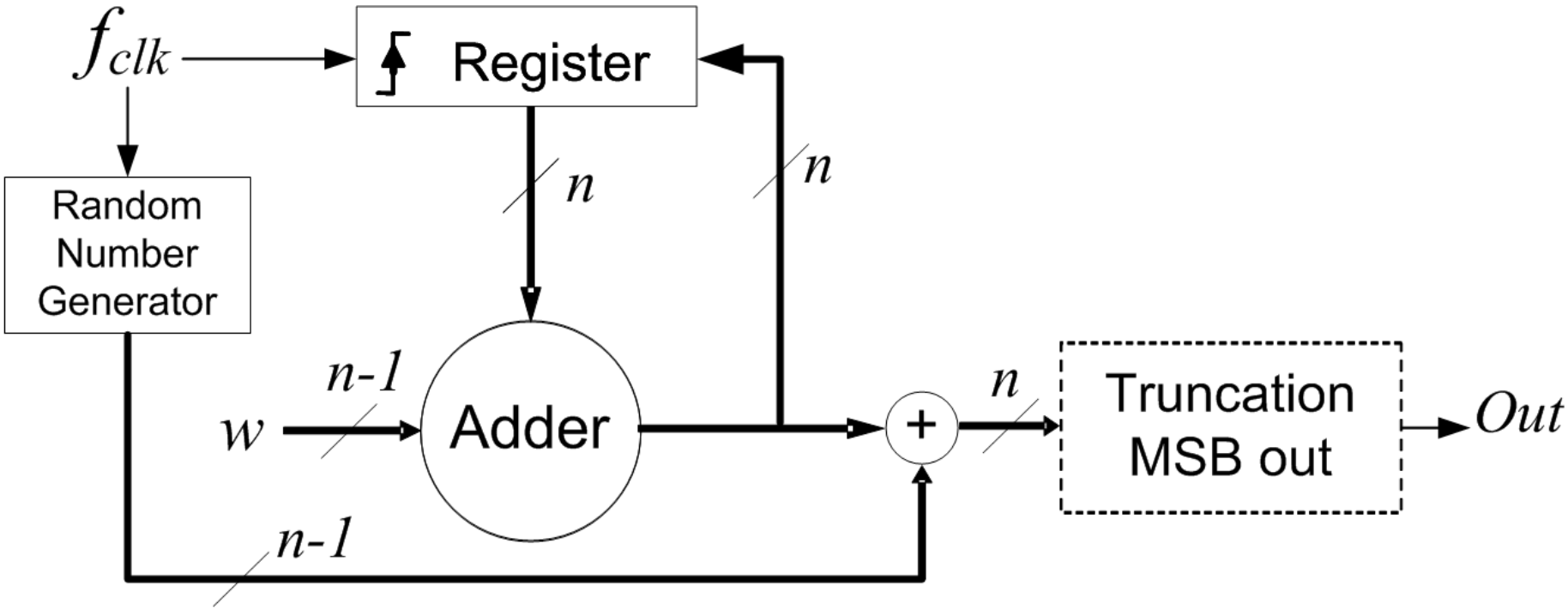


A random sequence is added to the FCW input of the PDDS.

- V.S. Reinhardt, “Direct digital synthesizers”, *Technical Report*, Hughes Aircraft Co, Space and Communications Group, 1985.
- C. E. Wheatley, III and D. E. Phillips, “Spurious Suppression in Direct Digital Synthesizers”, Freq. Control Symp, May, 1981.

PDDS with Phase Dithering

Block diagram

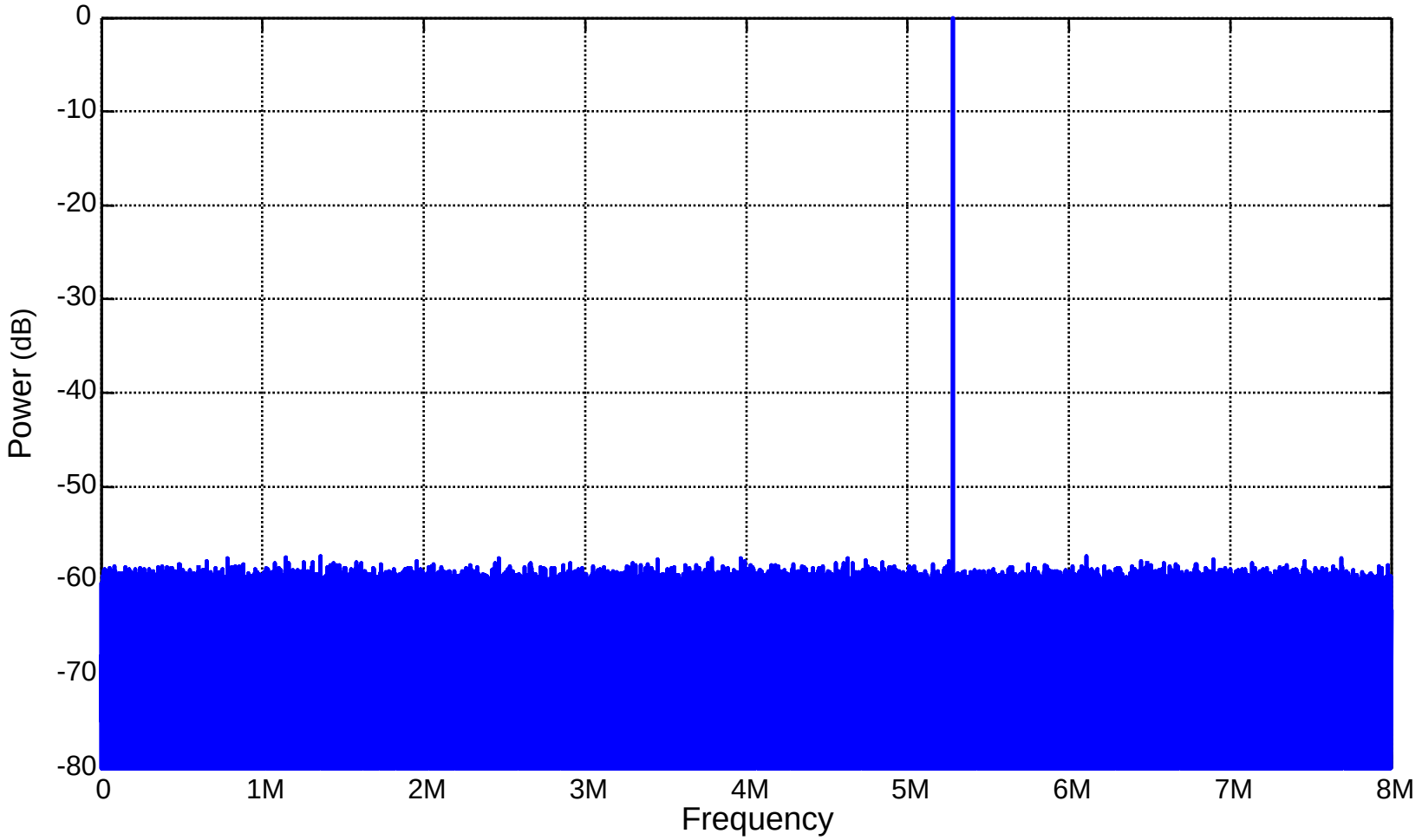


A random sequence is added to the Output of the Phase Accumulator.

• V.S. Reinhardt, “Direct digital synthesizers”, *Technical Report*, Hughes Aircraft Co, Space and Communications Group, 1985.
• C. E. Wheatley, III and D. E. Phillips, “Spurious Suppression in Direct Digital Synthesizers”, Freq. Control Symp, May, 1981.

PDDS with Frequency / Phase Dithering

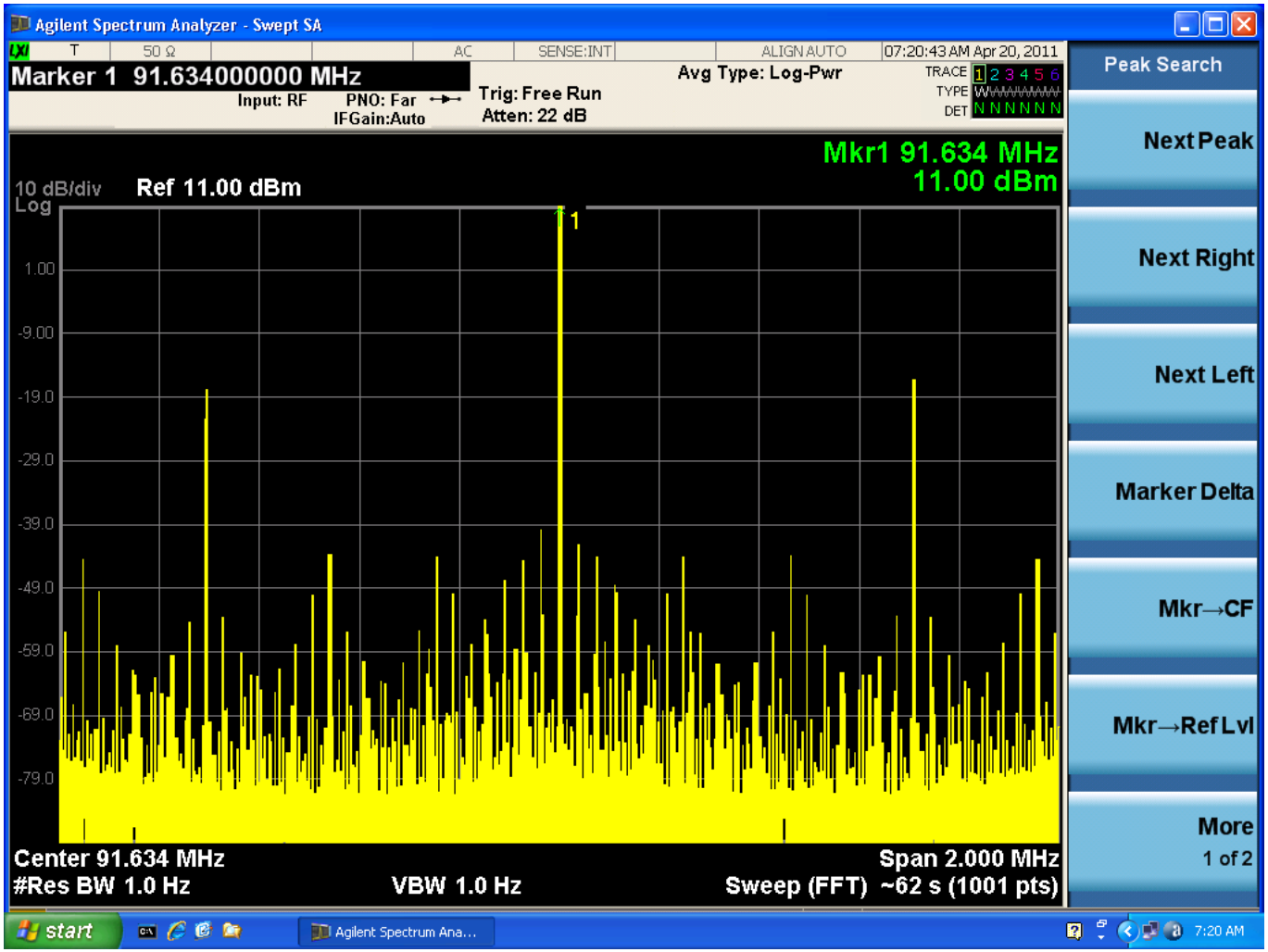
Output spectrum (simulation with a 16Mhz clk)



Spectrum is now clear of spurs but has elevated noise floor.

Implementation Measurements

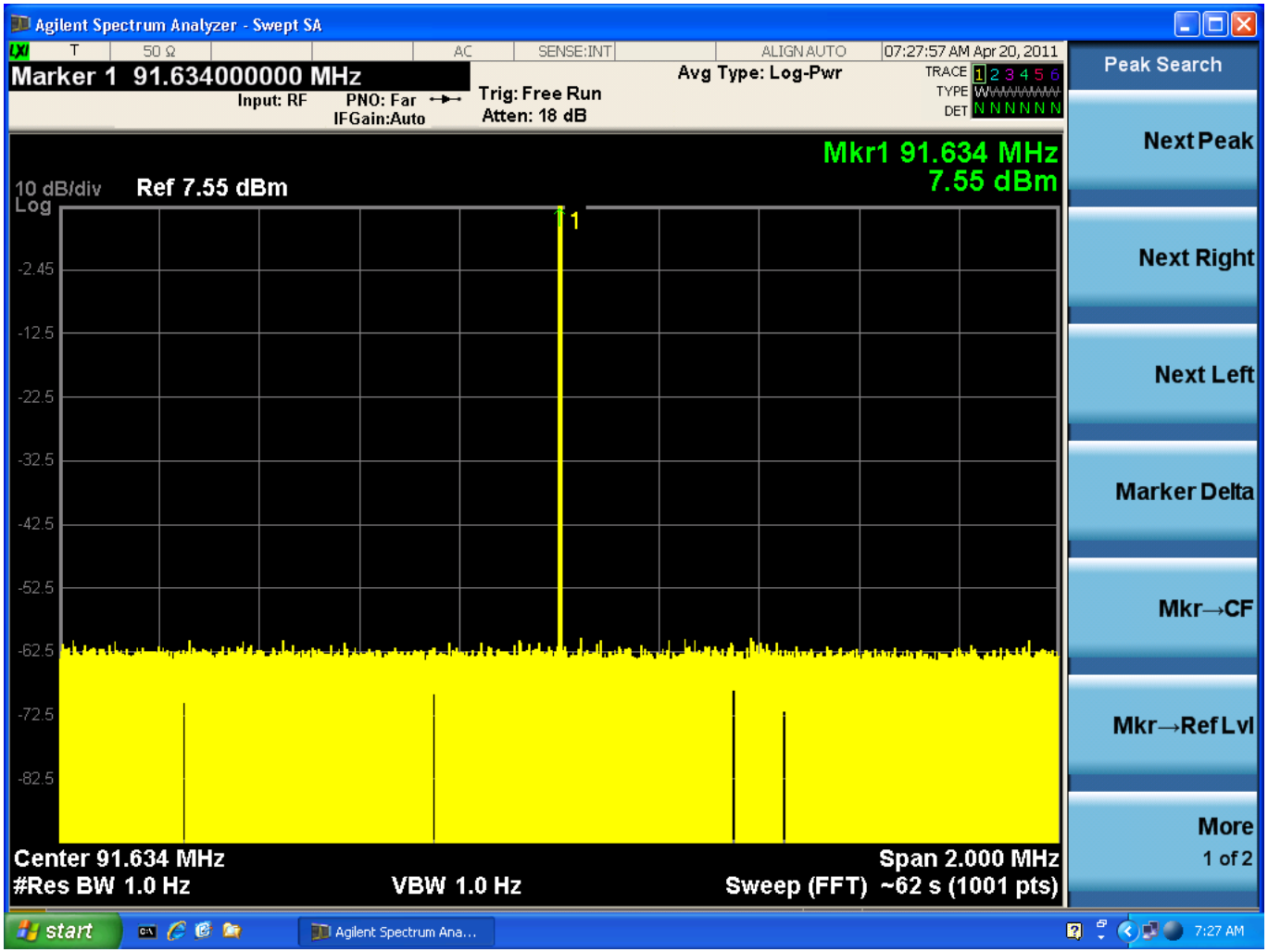
Undithered PDDS output



In Xilinx Spartan 3e (Clk = 200Mhz)

Implementation Measurements

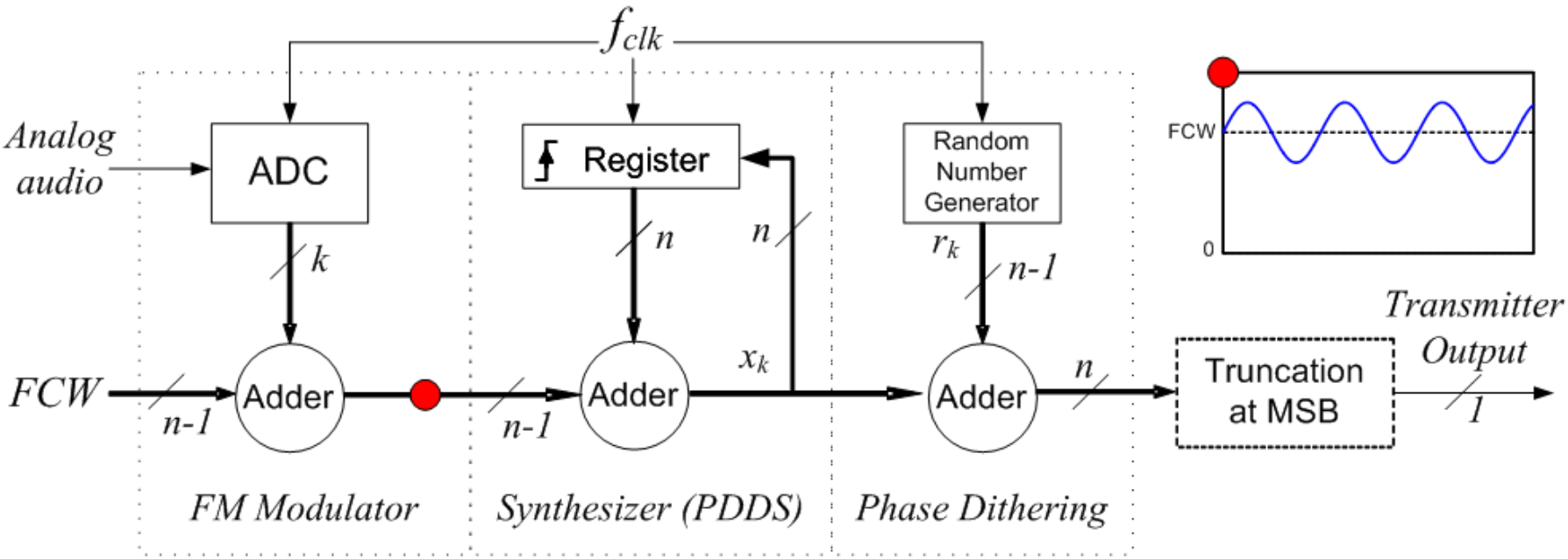
Dithered PDDS output



The implementation achieves a ~70dBc/Hz noise floor.

FM Transmitter Demo

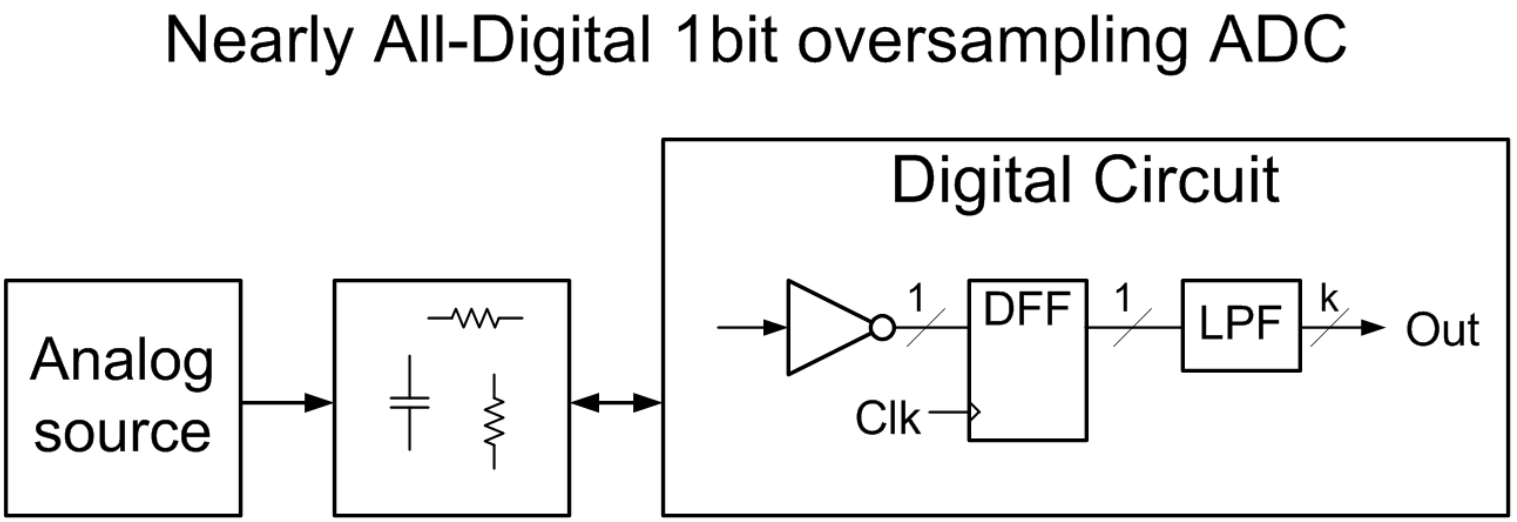
Block diagram



- Phase (rather than frequency) dithering is used in the PDDS.
- FM modulation is done by adding signed data to the FCW.
- A supporting ADC is used for Analog audio acquisition.

Audio Data Acquisition

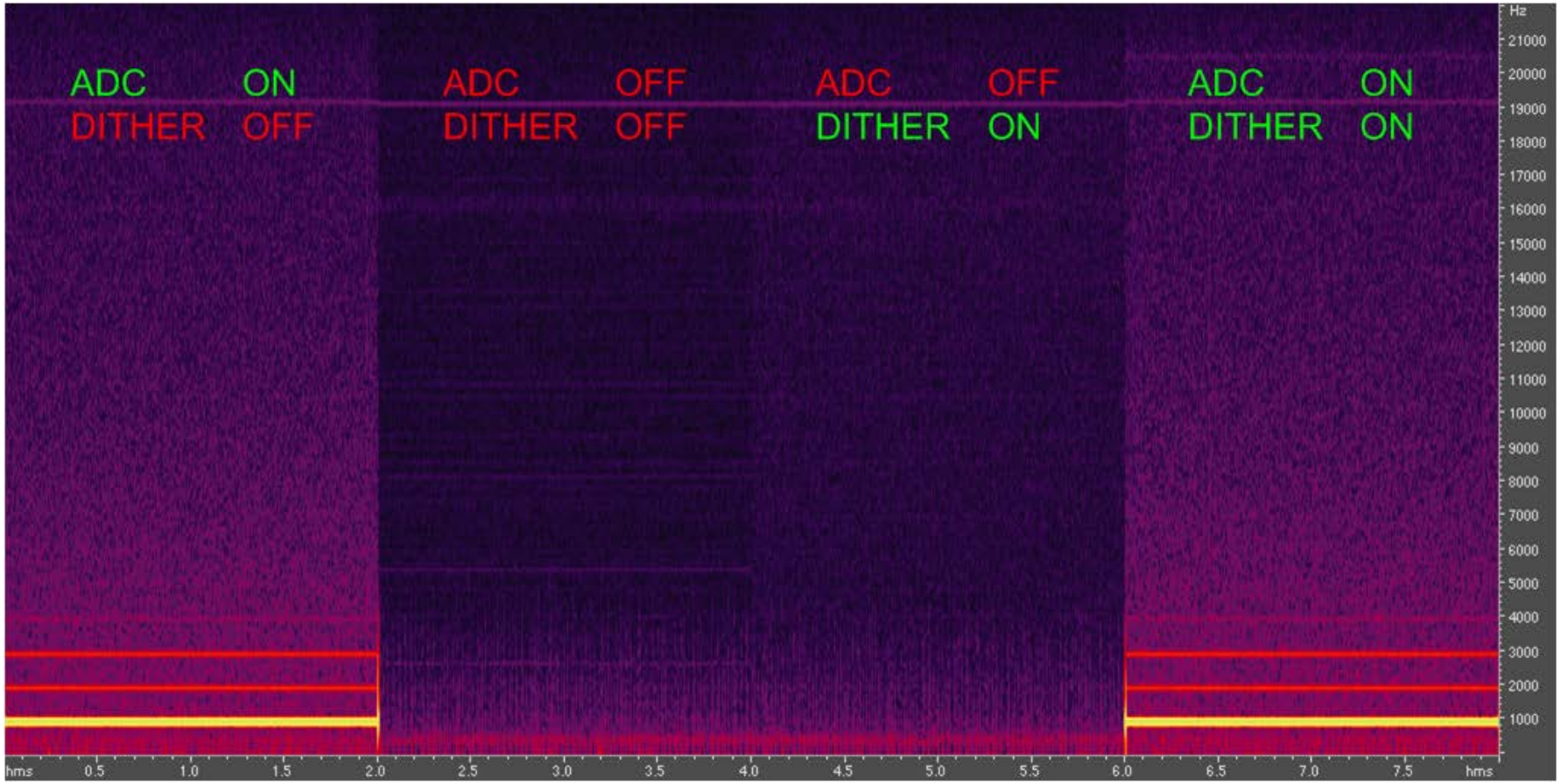
Any ADC could be used, but we preferred a…



- It is <u>supplementary</u>; Ideally (only) a Digital Data steam should be used.
- 1-bit Oversampling ADC better fits to this “All-Digital application”.
- Only a couple of external Rs & Cs analog components are used.

FM Transmitter Demo

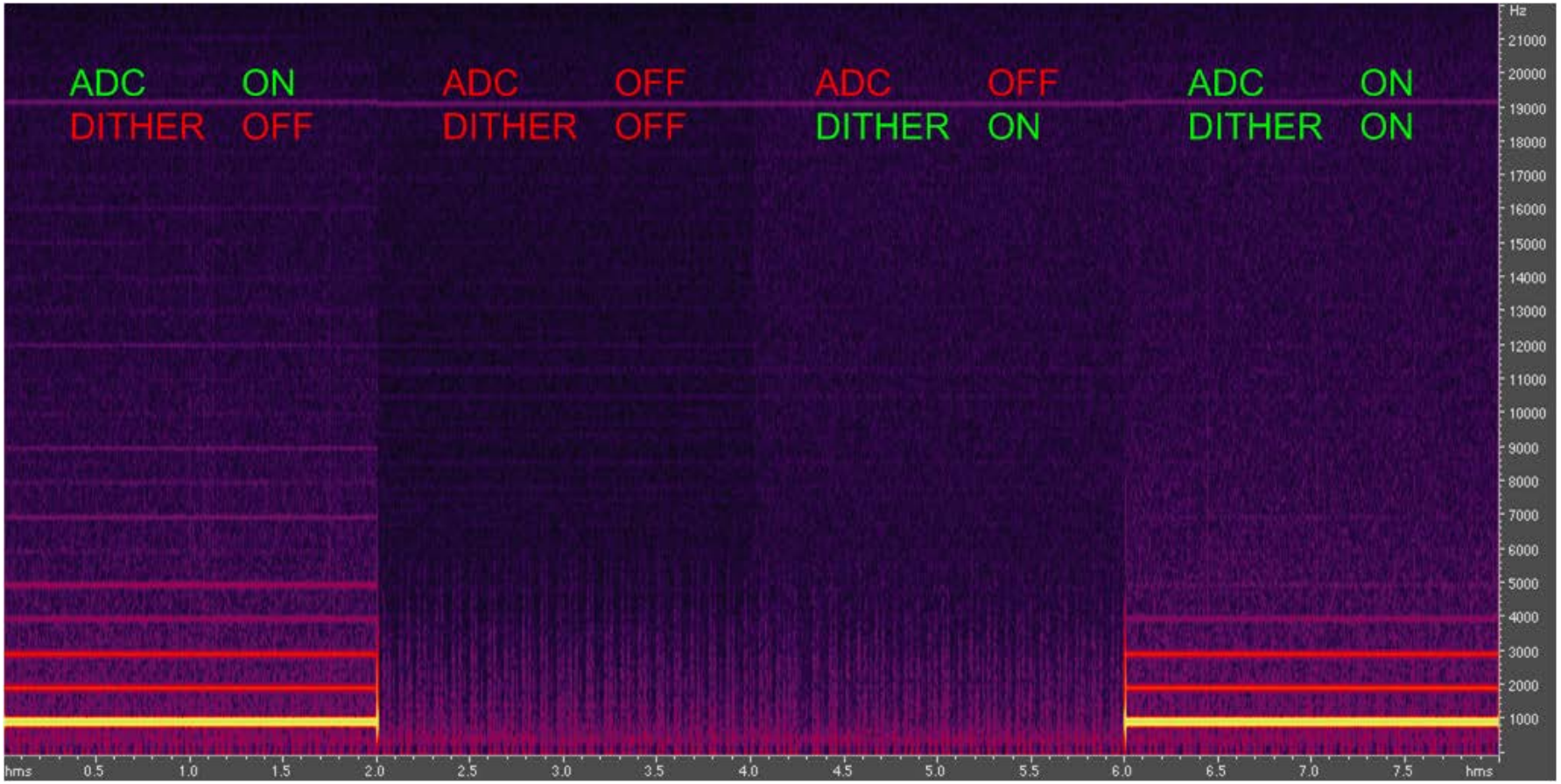
System performance using a 12bit ADC



Dithering slightly effects the noise performance of the system.

FM Transmitter Demo

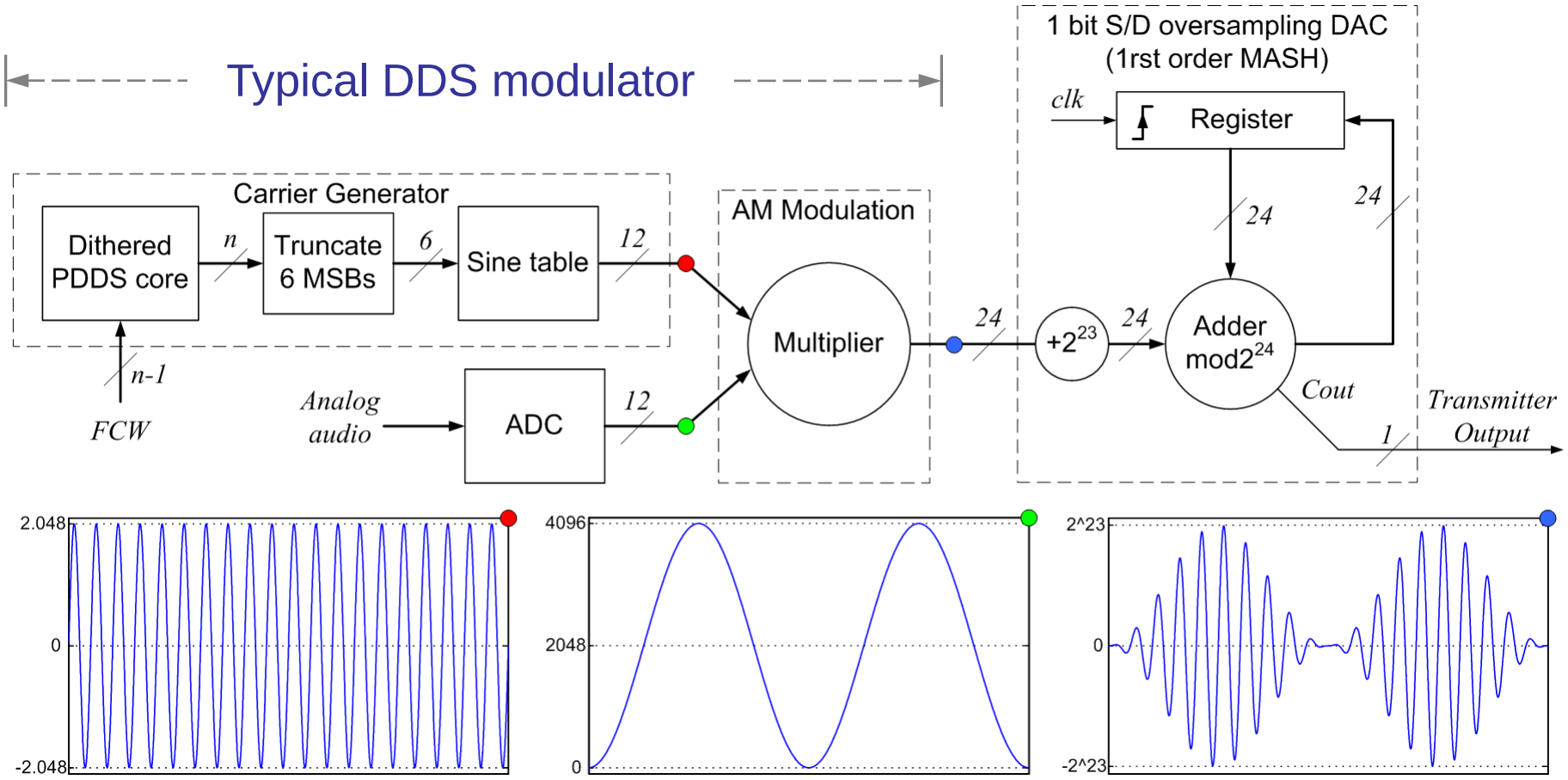
System performance using the implemented 1bit oversampling ADC



Similar performance but with lower ADC quantization noise.

AM Transmitter Demo

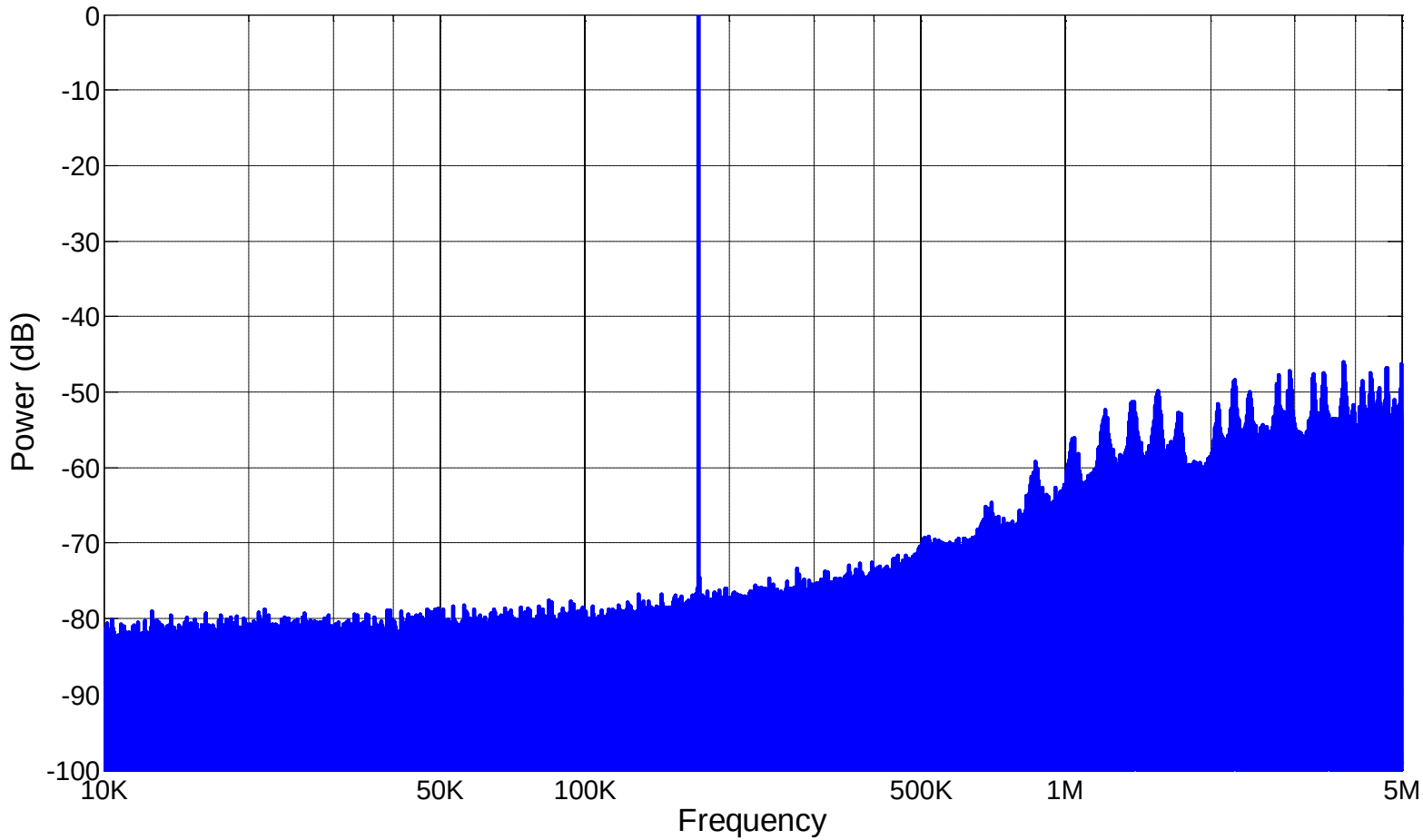
Block diagram



- The carrier is generated using the 6 MSB of the dithered PDDS and a sine table.
- AM modulation is done by multiplying the Carrier with the unsigned audio data.
- The Transmitter output is generated by an All-digital 1bit oversampling DAC.

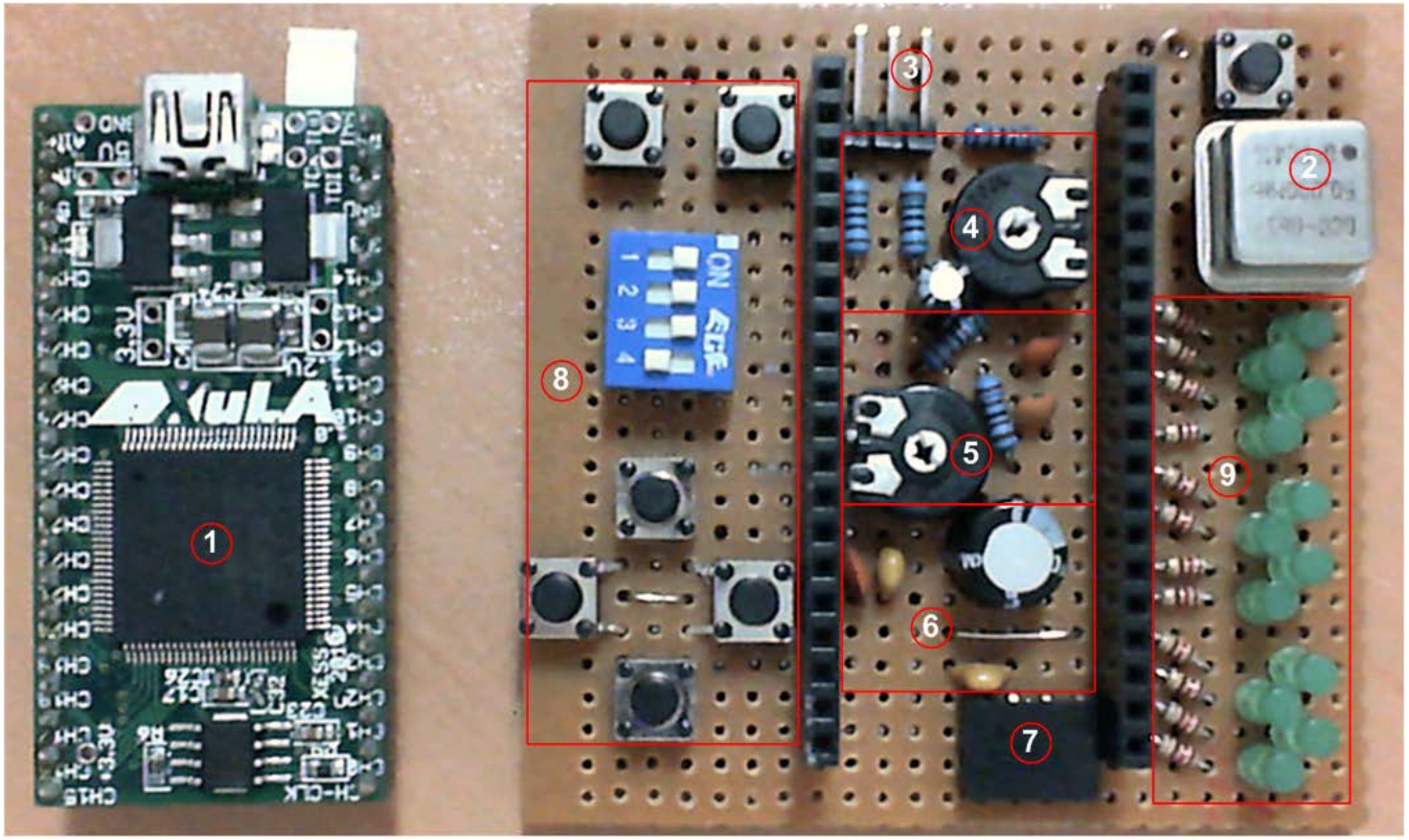
AM Transmitter Demo

Output spectrum (carrier only passing through the 1bit oversampling DAC)



- Useful only for lower frequencies but offers better noise performance.
- Actual implementation achieves a noise floor of ~90dbc/Hz for generated frequencies up to 5Mhz using a 200Mhz input clock.

The Demo Board



1) Xula-50 mini FPGA Board
2) System clock generator
3) Analog audio input
4) Analog audio handling
5) ADC external analog parts
6) Power decoupling
7) Antenna plug
8) Configuration controls
9) Led Display

The Demo Board

FPGA Utilization

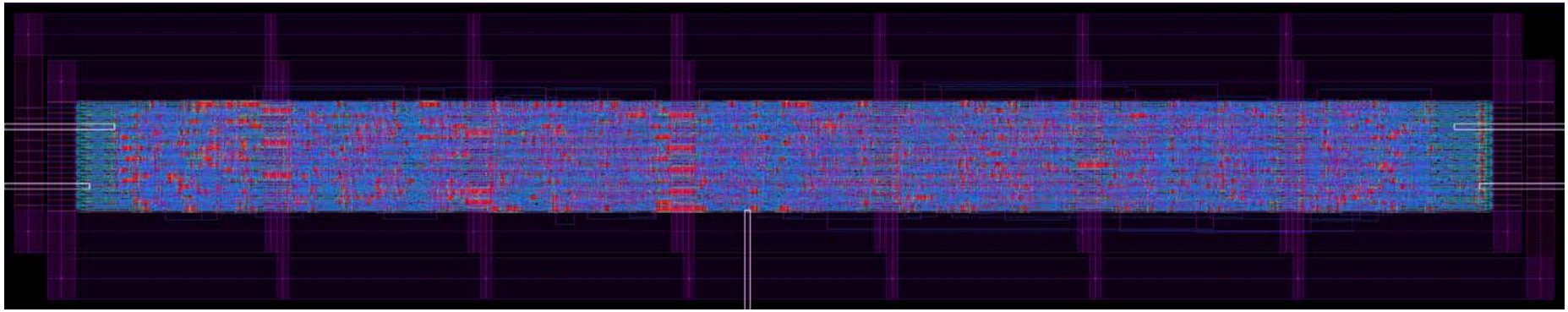
Target Device:	xc3s50a-4vq100
Product Version:	ISE 12.3
Design Goal:	Timing Performance

FM Radio Demo (with ADC and controls)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	336	1,408	23%
Number of 4 input LUTs	349	1,408	24%
Number of occupied Slices	258	704	36%

AM Radio Demo (with ADC and controls)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	404	1,408	28%
Number of 4 input LUTs	379	1,408	26%
Number of occupied Slices	304	704	43%

ASIC Version

An All-Digital transmitter (FM / FSK / PM / PSK) with digital data input has been implemented in a 90nm CMOS technology.



- Dimensions: 560um x 110um (with power ring).
- Generates GHz - range carrier frequency.

Conclusions and Future Work

- A versatile All-Digital transmitter architecture for low power, small area and low cost implementations has been presented.
- At this point we mainly focus on low power, short range applications.
- Algorithms are available for licensing.

Our team works on new architectures to:

- Further reduce the noise floor of the output.
- Increase the maximum operating frequency.
- Implement all popular modulation schemes (QAM, BPSK, FSK, QPSK, etc).
- Implement an All-digital receiver in order to offer a complete all-digital transceiver solution.

Thank you for attending

Questions and related communication are very welcome!

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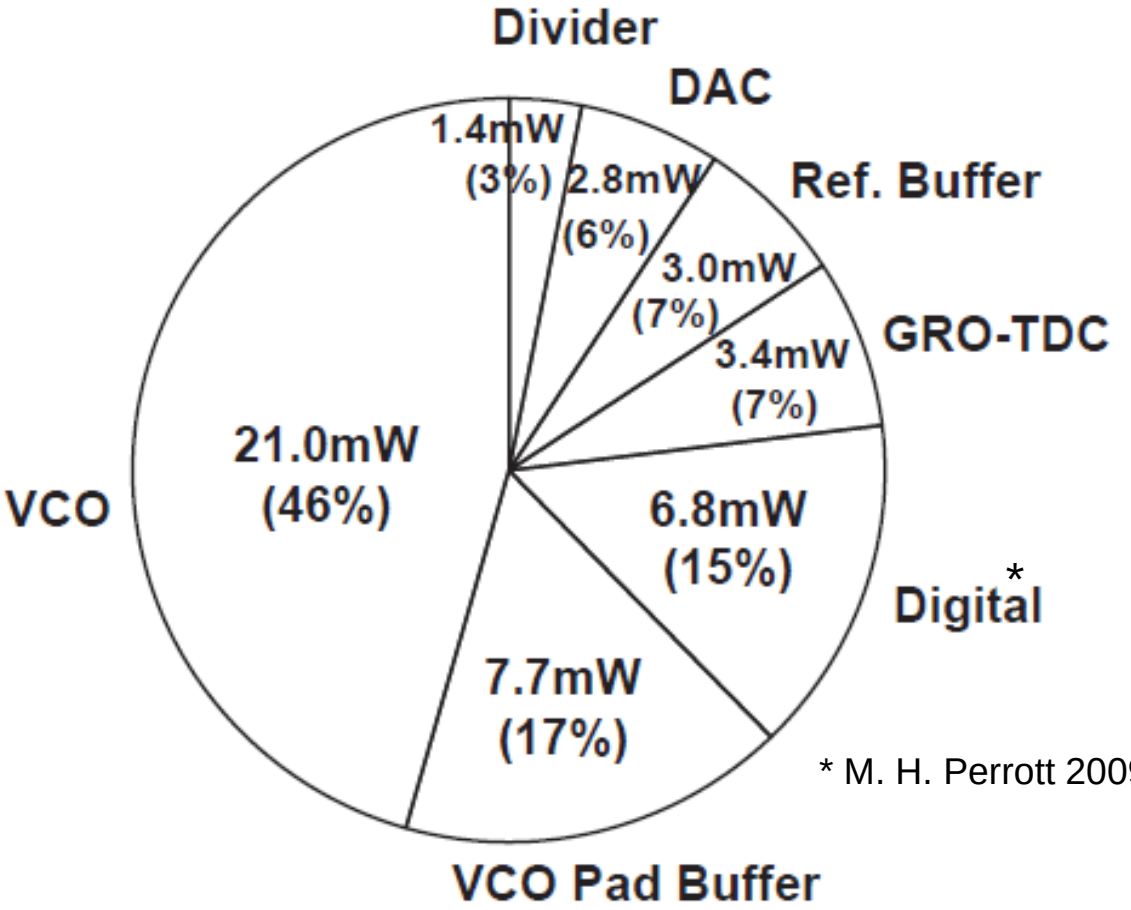
Direct All-Digital Synthesizer

In comparison to an All-Digital PLL



* M. H. Perrott 2009

DADS when used as part of an ADPLL consume less that 20% of the total consumption