Physical Verification Challenges and Solution for 45nm and Beyond

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Nanometer Design Era

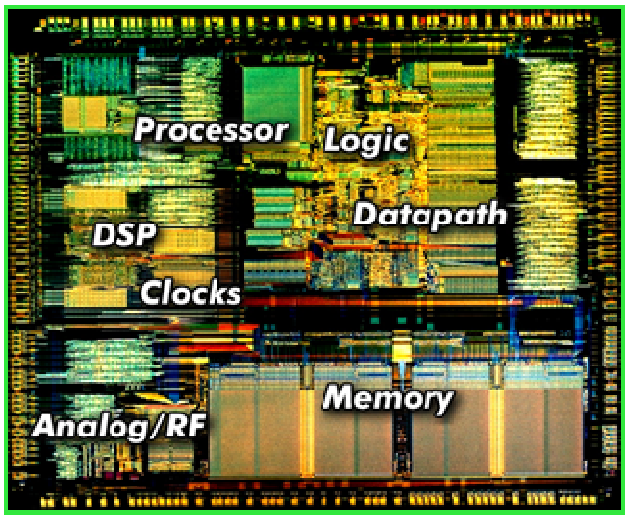
- Semiconductor feature size has been shrunk 500x in 40 years
  - Space for one transistor in 1971 holds a quarter million transistors now
- The feature size approaching silicon atomic size (the diameter is ~0.22nm)
  - Complexity of design rules increase explosively

Source: SemiconductorManufacturing@wikipedia

10 µm	1971
3 µm	1975
1.5 µm	1982
1 µm	1985
800 nm	1989
600 nm	1994
350 nm	1995
250 nm	1998
180 nm	1999
130 nm	2000
90 nm	2002
65 nm	2006
45 nm	2008
32 nm	2010
22 nm	2011
16 nm	~ 2013
11 nm	~ 2015

Layout Structure is Complicated …

- Deep hierarchy level
  - how many?
- Different design modules
  - Logic, memory, analog, …
- Module boundary is not just a rectangle
  - could be a rectilinear
- Modules are heavily overlapped each other



… Layout Structure is Complicated

- Bigger and bigger routing block
  - Which is flatten
- More and more library cells
- More and more metal layers
  - Up to 12 metals or more
- Huge dummy metals
  - Usually are very flatten
- …

Data Amount

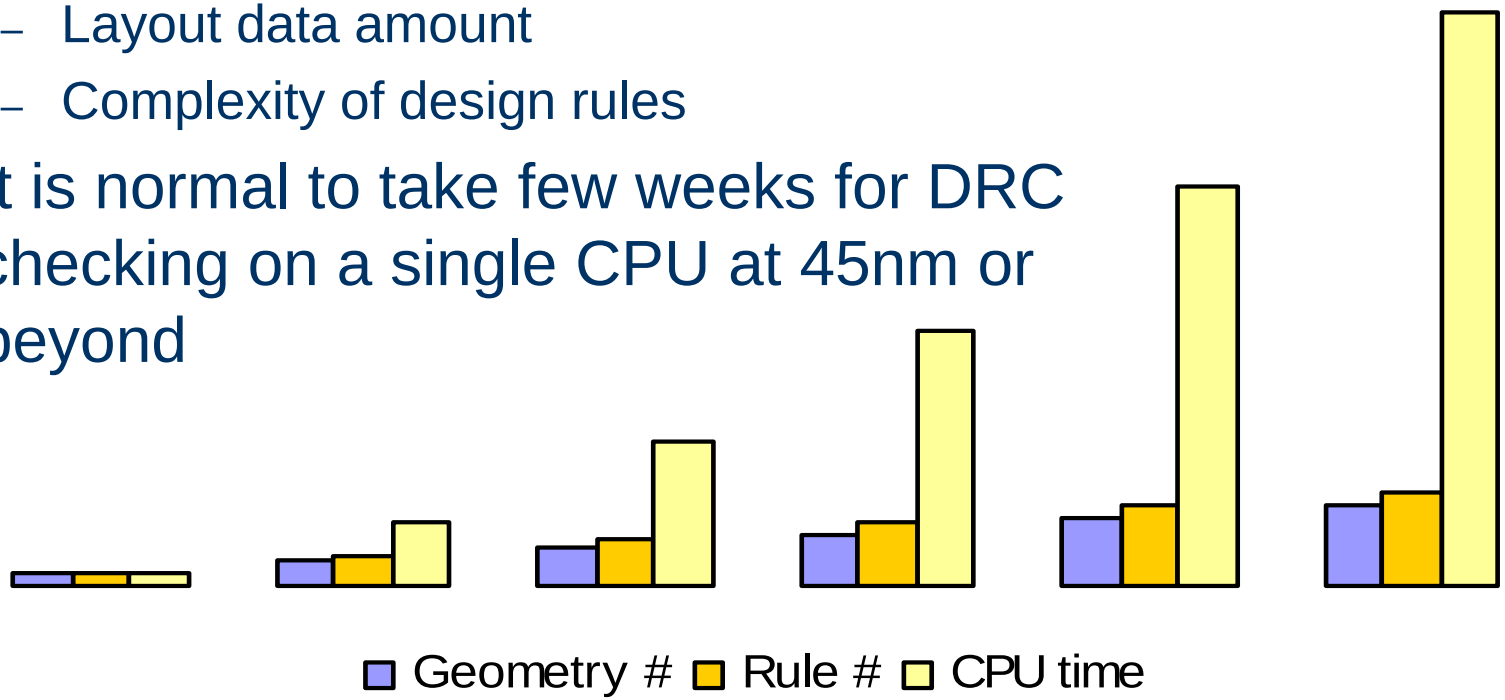
- Billions of transistors on a SOC chip
- Tape-out data for manufacture reaches terabyte magnitude in GDSII
  - What if the data is flatten?

Explosion on Design Rules

- Number of design rules are exploded, because of
  - The feature size approaching silicon atomic size
  - Sub-wavelength process technology
- Operation count has increased to over 20k
  - Total 6 hours CPU time for 1 second per operation

DRC Running Time Exploding

- Due to
  - Layout data amount
  - Complexity of design rules
- It is normal to take few weeks for DRC checking on a single CPU at 45nm or beyond



Parallel Processing

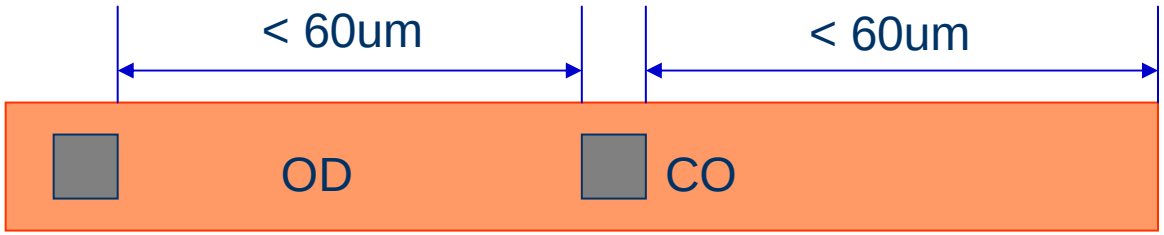
- Parallel processing is the solution
- But how, and what are the issues then?
  - How to partition data?
    - What if a device is partitioned?
    - What if an instance is partitioned, or hierarchy is broken?
    - Any data is duplicated?
  - How to balance jobs between processors?
  - How to synchronize them?
  - How to communicate between them?
  - How to merge data back?

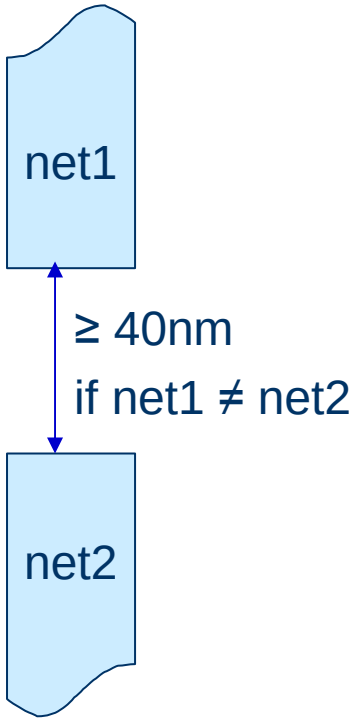
More Issues on Parallel Processing

- Memory
  - Will the memory be overflowed?
- Disk
  - Will the disk be overwhelmed?
- Network
  - Will the network be jammed?
- Seamless
  - Will the results be different from that on single CPU run?
- Overhead
  - How much overhead for that?
  - What is the scalability?

Is DRC a Local Issue?

- What is halo for dimension checking?
  - E.g.: Distance between two CO on layer OD should be less than 60um
- What if the polygon based operations?
  - E.g.: A metal must enclose at least two vias
- What if the net related checkings?
  - E.g.: Check space only if they are not the same net

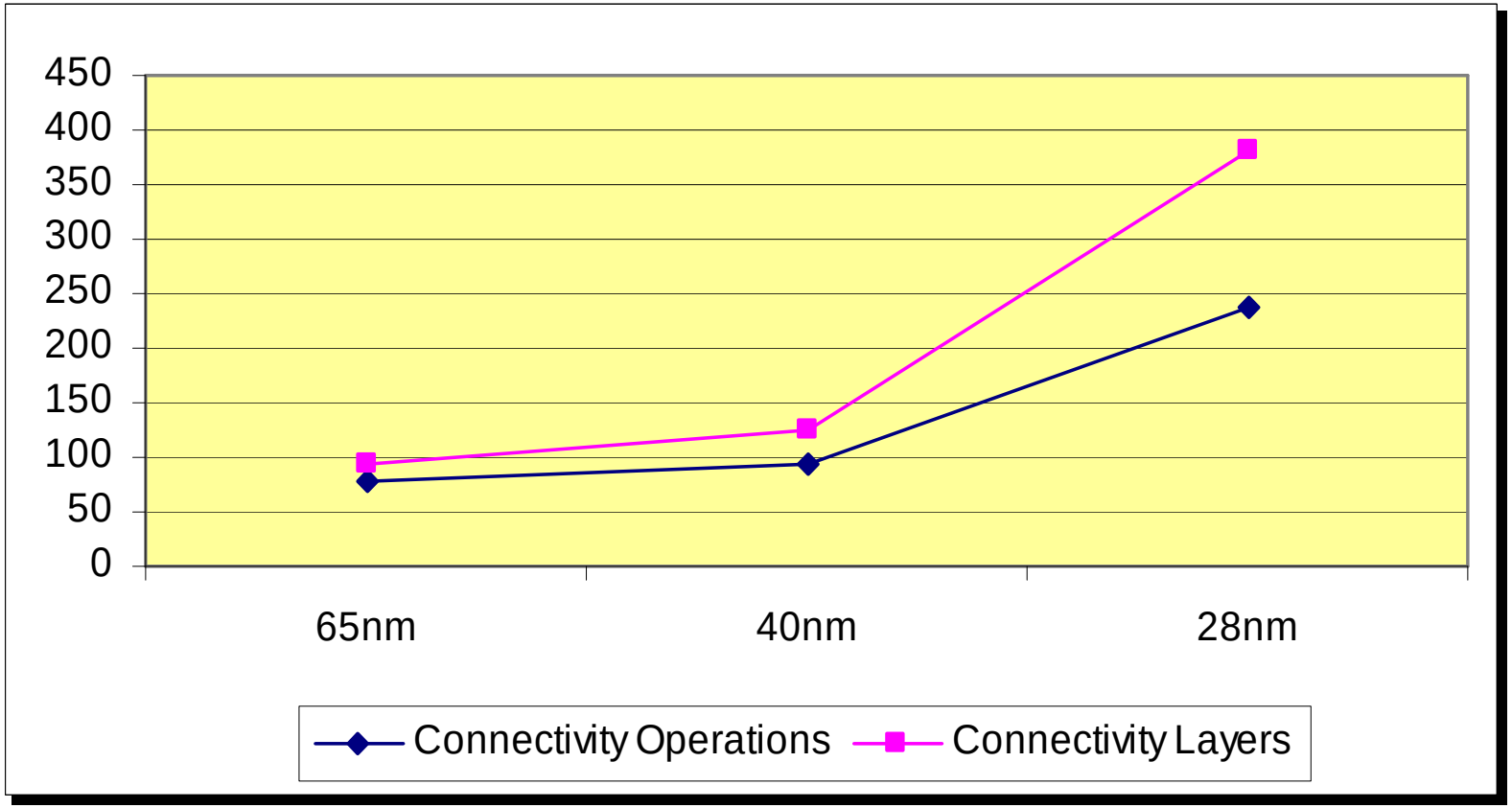




Rules, Operations and Layers

- Rules are more and more complicated
- More and more operations are needed to implement a rule checking
- More layers are involving for complicated rule checking, e.g.:
  - More and more rule checking needs connectivity information, and
  - More and more layers are involved in connectivity operations

Connectivity Operations and Layers



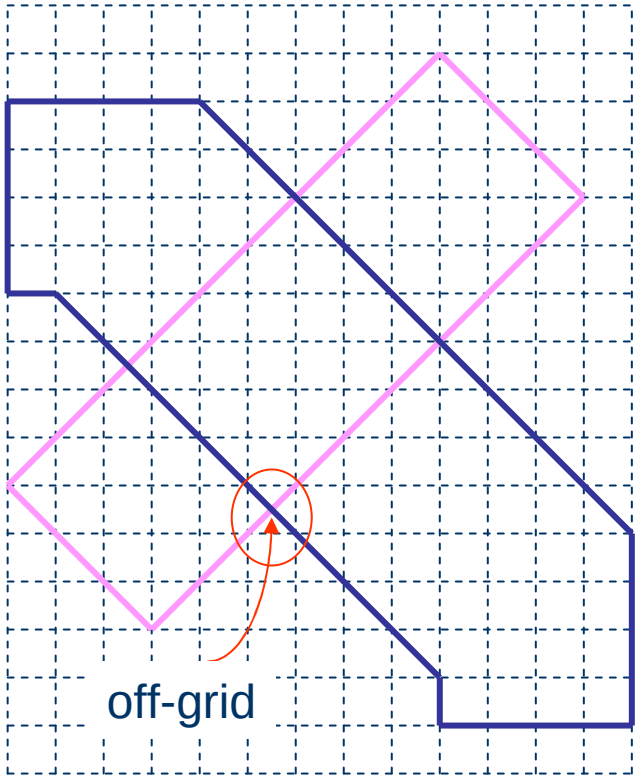
Is DRC just for Geometry Dimension Checking?

- Netlist extraction
- Device parameter calculation
- Antenna checking
- Electrical rule checking
- Net selection
- Overall, objects in DRC:
  - Polygons, edges, points, layers, nets, devices, device parameters, geometry properties, text labels, error marks, …

Is DRC just for Verification?

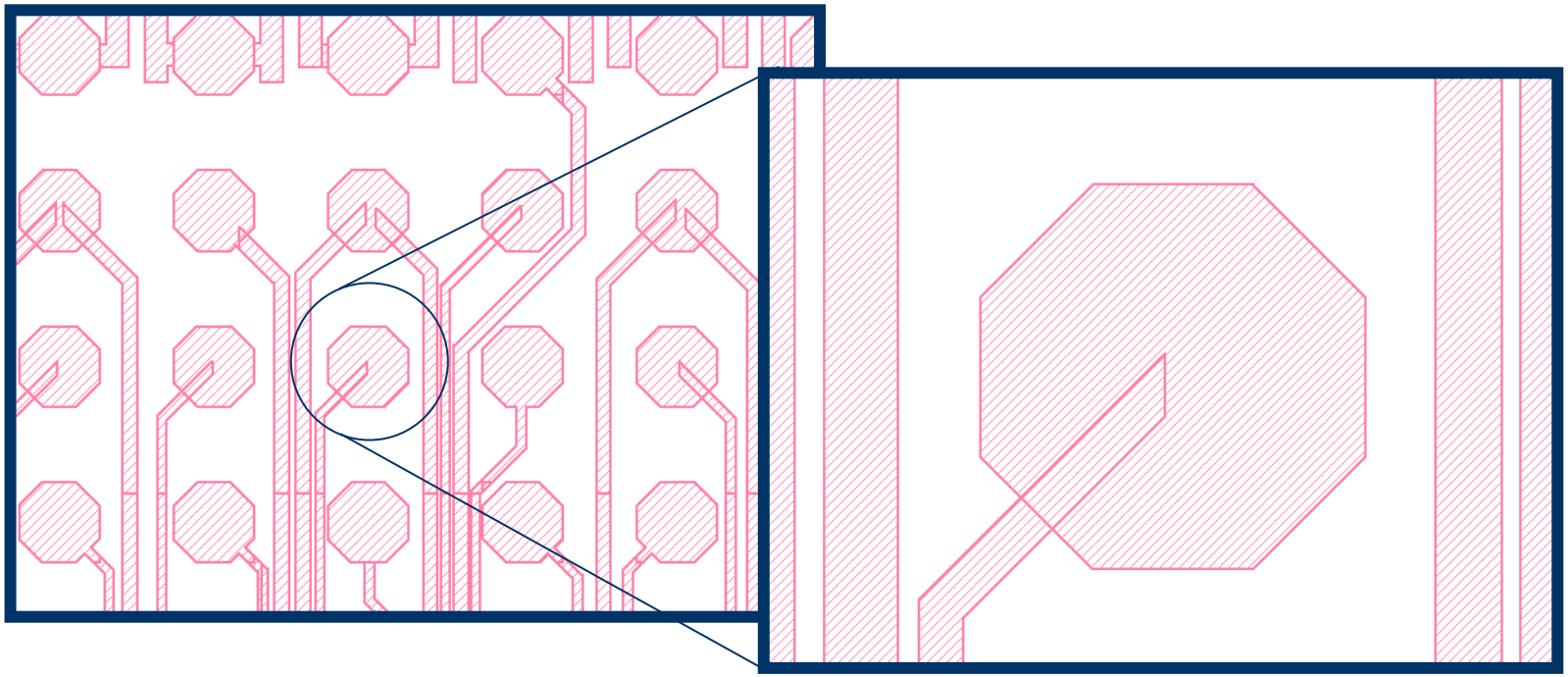
- Metal filling
- Layout modification
  - Double via insertion, for example
- Geometry correction
  - DFM optimization, such as OPC
- Mask generation
- …

Accuracy and Capacity



- Snapping the intersection point to a grid
  - Some edges are shifted
  - The angle is not 90 degree any more
  - False/Missing errors might happen
- Scaling up the design might limit the design size

Accuracy Example



- False errors might be created

DRC for Small/Block-level Designs

- **Custom Design Platform**
  - Small designs
  - These features are NOT critical

- **P&R flow**
  - Block-level designs, no hierarchy
  - These features are NOT critical
  - These features are NOT necessary
  - Rule deck is much simpler

Performance
Memory Usage
Hierarchy
Parallel Processing

Device Extraction
Device Parameter
Connectivity Extraction

Evaluating a DRC tool

- Layout patterns
  - To check error mark accuracy
  - To check robustness
  - To check feature coverage
- Full chip designs with **completed rule decks**
  - To check accuracy with large designs
  - To check accuracy with all advanced rules
  - To check memory usage
  - To check disk usage
  - To check performance
  - To check performance/accuracy on parallel processing
  - …

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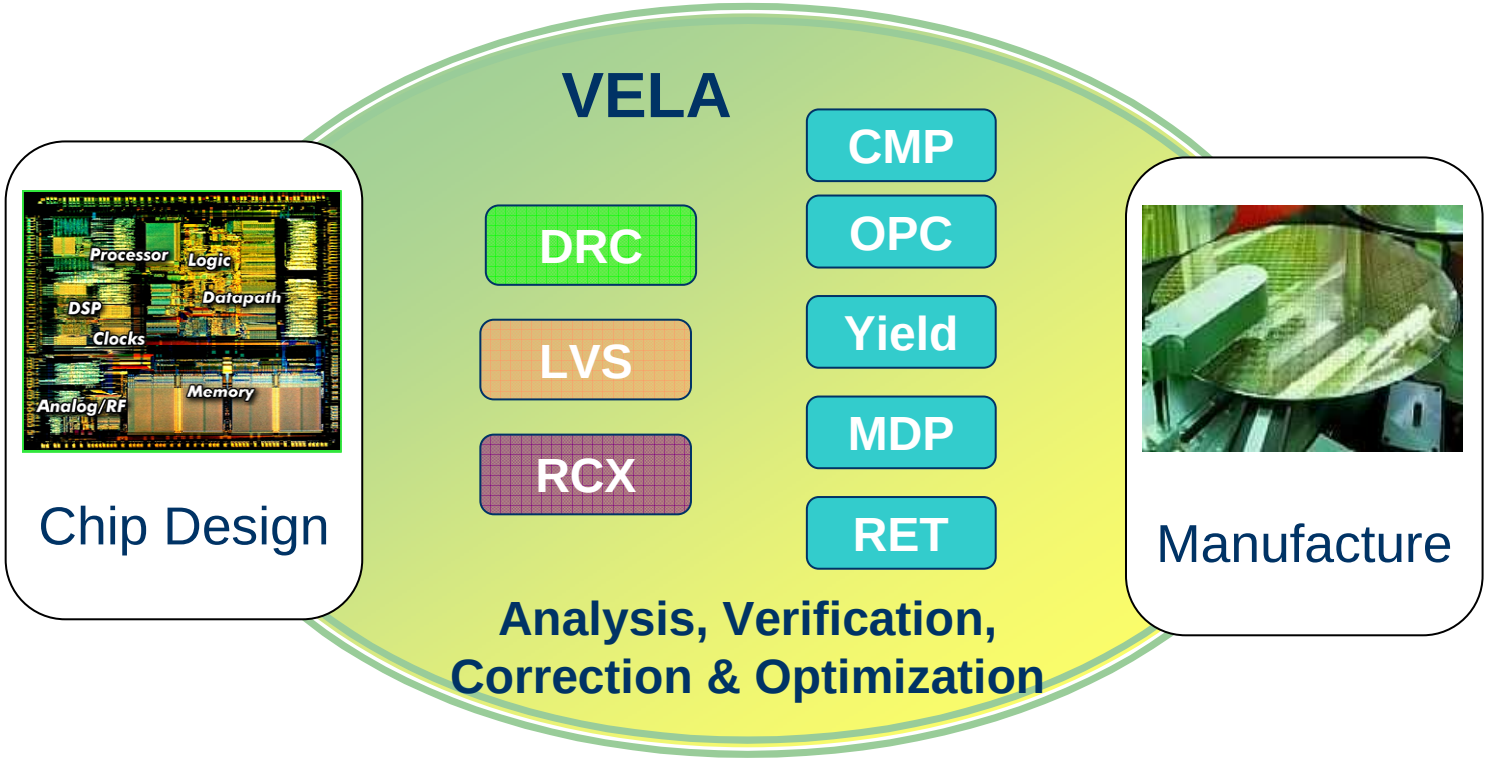
VELA Platform



Celesda Technologies

- Proprietary geometry processing algorithms to achieve performance boost
  - 2-4X faster than the leading competitor
  - Preserve verification accuracy
- Proprietary Multi-Level Intercrossing Data Management for Parallel Processing
  - Achieve linear scalability on multiple CPUs
- Less memory usage based on customer evaluation results

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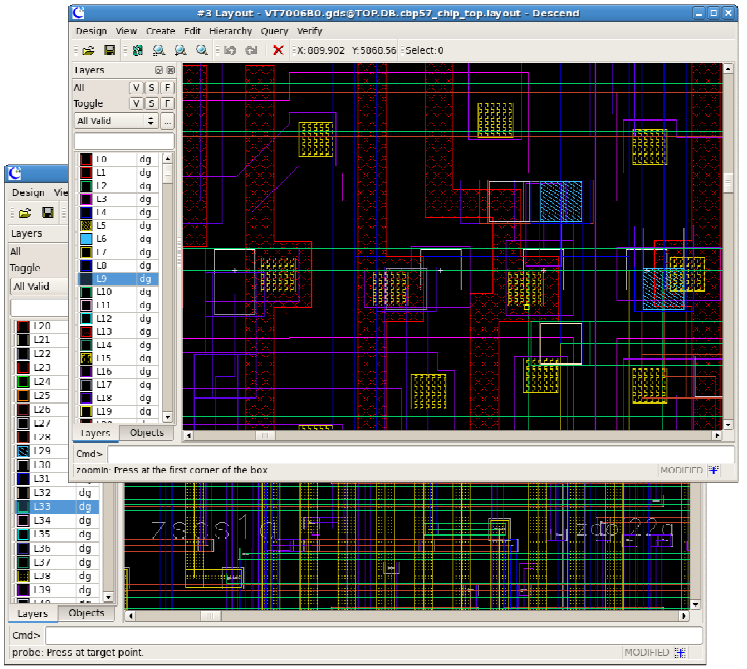
Plug-and-Run

- No impact on customers' existing flow
- Support iDRC for advanced technology nodes



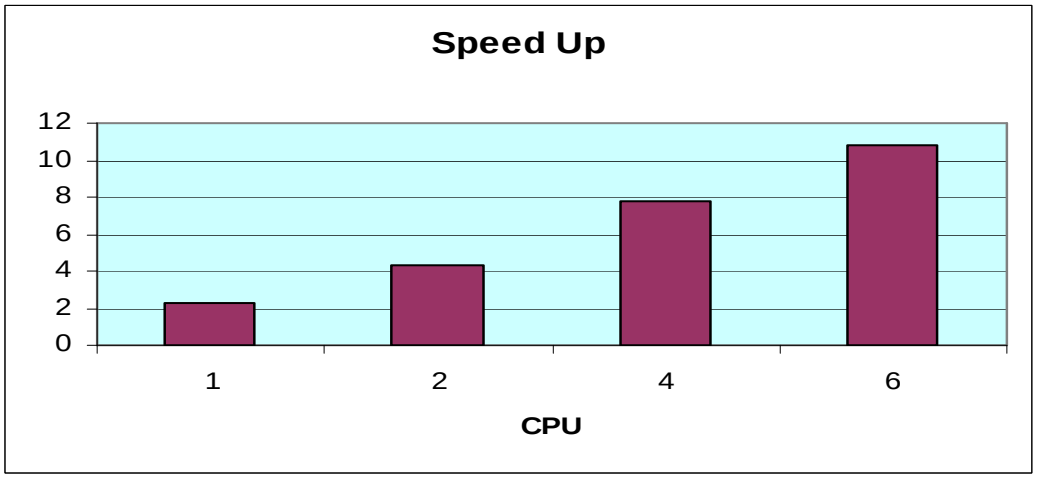
Product Status

- Verified Technology nodes
  - TSMC 180, 130, 110, 65/55, 45/40, 28nm
  - SMIC 180, 130, 110, 65nm
  - Jazz/Tower 180nm
- Supported Features
  - DRC
  - Antenna checking
  - Density
  - Metal Fill
  - Netlist extraction
- Business
  - Has taped out over 30 designs on few companies

Testing Data

Case	GDSII	Vela			
		1 cpu (s)	2 cpu (s)	4 cpu (s)	6 cpu (s)
V82	9.2GB	35,505	18,382	10,156	7,296

- A SoC Design
- Data communication, 40nm technology



Thanks