Future Directions in Mixed-Signal IC Design

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Outline

- A (superficial) snapshot of the semiconductor industry
- The need for analog/mixed-signal interfaces
- Research examples
  - High-performance A/D converters
  - Medical ultrasound systems
  - Structural health monitoring
  - Neural prosthetics
  - Large area electronics
The Beginning of an Industry

Transistor
Bardeen, Brattain, Shockley, 1948

Integrated Circuit
Kilby, 1958
Moore’s Law

- In 1965, Gordon Moore predicted exponential growth in the number of transistors per integrated circuit.
... And He was Right

[ITRS 2007]
A Gigantic (Economic) Feedback Loop
State-of-the-Art Semiconductor Fab

- E.g. Intel’s “Fab 32” (Chandler, Arizona) ~ $3 Billion
State-of-the-Art Silicon Chips

Intel “Tukwila”
>2 Billion Transistors

Single-Chip GSM Radio
[Staszewski, ISSCC 2008]
45nm Technology (Intel)

More than 2 million 45nm transistors can fit on the period at the end of this sentence.

If that period were enlarged to about 6 feet in diameter, as shown at left, a one-inch section would bear 500 transistors, shown in the cut-away below.

A slice from a chip
Intel's new chip holds 2.2 billion transistors. Below is a cut-away of a portion of the chip enlarged over 1 million times showing just 500 of these transistors. We've peeled back the nine layers of copper wires that bring electrical current to the transistors on the bottom layer. Each layer of copper must be thicker than the layer below until the top layer is large enough to connect to other parts of the computer.

Steve Cowden
THE OREGONIAN
July 2007
Transistors Will Continue to Shrink

The graph illustrates the evolution of transistor technology with shrinking gate lengths (L_GATE) over time. The x-axis represents the years (2000, 2010, and 2020), and the y-axis represents the gate length in microns and nanometers.

- Evolutionary CMOS
  - 2003, M.Bohr
  - Reasonably Familiar
  - Nanotubes
  - Nanowires

- Revolutionary CMOS
  - 11 nm

- Exotic
  - 8 nm

The graph shows the transition from evolutionary to revolutionary technology with a focus on the advancements in gate lengths, indicating the progression of semiconductor technology.
Increasingly Complex Applications


[Walden Rhines]
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The Age of “Digital” Stuff

Basic Features

- All Digital Phone
- Speakerphone included
- Hearing Aid Compatibility = M3
  For details on Hearing Aid Compatibility, select this link
- Insurance Available
- 4 Parent Programmable Numbers
- Dedicated Emergency Key (Programmable Number)
- Super Simplified Keypad and Interface
- Meets FCC SAR limit. Manufacturer’s highest FCC reported 1.24 at ear, 0.84 on body. Actual SAR may vary.
The Reality of Modern Electronic Systems

Sensors, Transducers, Antennas, etc.

- Signal Conditioning
- A/D
- CLK
- Signal Conditioning
- D/A
- Signal Processing

Analog

Digital
Analog Interfaces are Everywhere
Digitally Assisted A/D Converters

Analog Media and Transducers

Signal Conditioning

A/D

Signal Conditioning

D/A

CLK

Signal Processing

Additional digital processing for performance enhancement

Analog

Digital
ADC for a “Digital” Link

- No analog error accumulation
- Better scalability
- Need efficient digital processing hardware
- Need efficient high-speed ADC, typically > 10GS/s
Time-Interleaving

- Popular way to increase ADC throughput
Imperfections

- Mismatches result in signal distortion
  - Gain
  - Offset
  - Timing Skew

Mismatches result in signal distortion:
- Gain
- Offset
- Timing Skew
Our Focus: Timing Skew

(2-channel example)
Skew Calibration Using Extra ADC

- Statistics-based skew measurement in digital backend
- Correction through analog adjustments

Digitally adjustable delay cells
Timing of Auxiliary ADC Phase

\[ \phi_1, \phi_2, \phi_N, \phi_{Cal} \]

Digital Backend

ADC_1 \arrow{\phi_1} \rightarrow \ADC_2 \arrow{\phi_2} \rightarrow \ADC_N \arrow{\phi_N} \rightarrow ADCCal \arrow{\phi_{Cal}} \rightarrow X(t) \rightarrow Y[n] \rightarrow Digital Backend \rightarrow Clock
Calibration Scheme

- For each channel, adjust delay cells until correlation between calibration ADC output and each slice are maximized.
- $\text{ADC}_{\text{Cal}}$ can be 1-bit, "slow"
Experimental results deleted....
Cell Phones vs. Medical Ultrasound

- **Today’s cell phones**
  - Leverage highly optimized, power & cost efficient integration

- **Today’s ultrasound machines**
  - Lots of progress in miniaturization
  - Insufficient progress in holistic system optimization, SoC integration and cost reduction
Today’s System Architecture

N = 16…512 Piezo Elements

Digitization path (~12b, 50MS/s) using discrete components replicated N times

1. This small-footprint PCB includes Simplify Systems’ 32-channel ultrasound analog front-end reference design. It includes a pair of 16-channel SAM1600 ADCs.
Working on the Next-Gen Front-End
Fly-by-Feel Aircraft

Fly-by-Feel Autonomous Vehicle

Intelligent, Self-Repairing Materials

Multi-Scale Fabrication and Integration

Bio-Inspired Sensor Network

Stretchable Network

[Fu-Kuo Chang]
Stretchable Network

[Fu-Kuo Chang]
Interface for Structural Health Monitoring
Neural Prosthetics

- Cortical motor prosthetics
  - Neurons in the motor cortical areas of the brain encode information about intended movement
Neural Signal Acquisition

- Electrode signals consist of multiple sources
  - DC Offset, about 15mV from electrode/tissue interface
  - Local field potential (LFP), ≤3mV peak, 10Hz to 100Hz
  - Spikes from nearby neurons, 35μV – 1mV peak, 500Hz to 5kHz

![Raw signal](image1)

![Filtered signal](image2)

Courtesy M. Sahani

Courtesy C.L. Klaver
## Specs

- Separate the fast and slow signal acquisition for DR
  - Custom front end design for each path

<table>
<thead>
<tr>
<th></th>
<th>Spikes</th>
<th>Local Field Potential</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gain</strong></td>
<td>600 V/V</td>
<td>200 V/V</td>
</tr>
<tr>
<td><strong>Lower Cutoff</strong></td>
<td>300Hz</td>
<td>1Hz</td>
</tr>
<tr>
<td><strong>Upper Cutoff</strong></td>
<td>10kHz</td>
<td>1kHz</td>
</tr>
<tr>
<td><strong>Input Referred Noise</strong> (total from sampling node)</td>
<td>2.0µVrms</td>
<td>1.0µVrms in 10-100Hz</td>
</tr>
<tr>
<td><strong>Total Power (96x Array)</strong></td>
<td>3mW</td>
<td>100µW</td>
</tr>
</tbody>
</table>
Spike Path Front-End

Input Stage

SC Bandpass Filter

Output Buffers

SAR ADC Input Cap
Sampling Phase

- Integrate signal current on $C_B$ and sample
  - High-pass for DC block using $C_{ac}$ and $R_{big}$ (off-resistance)
  - $A_1$ contains a pole that helps minimize noise folding
A1 Implementation Details

Flicker noise reduction

Anti-alias for thermal noise from $M_{1a,b}$
Processing Phase

- Process charge on $C_B$
  - SC biquadratic filter
  - Output buffers make a post-filtering pole and reduce A2’s load cap
Static Power

Power Pie Chart (including overhead)
Total Power (Single/Array) = 21.26uW / 2.04mW

- Overhead = 2.76uA
- A4 = 1.36uA
- A3 = 0.74uA
- A2 = 0.90uA

A1 = 11.96uA
Two-Channel Interface Pixel

SAR ADC

Frontend
Die Photo (96 channels, 5mm x 5mm)
The Future?
Organic Semiconductors

- Mechanically flexible
- Suitable for solution processing
  - Cover large areas at low cost
  - Make disposable devices

Jellyfish Autonomous Node

Cartesian Diver (Communication)
Control Surfaces
Constrictor Muscles
Piezoelectric – conductive polymer bundles, IPMC, shape memory, carbon nanotube, Elastomeric conducting polymers
Hydrophones
Flexible PVDF copolymer based NEMS / MEMS

Bell: Compass (nanocomposites)
Control Electronics (flexible, organic)
Supercapacitors (carbon nanotube)
Bio-Cell
Fuel storage and chemical reactors
Calibration / Positioning
Projector (Magnetoelectric GPS, PVDF)

Energy Harvesting (multi-modal)
Ferroelectric polymer
Magnetoelectric microtubes
Elastomeric conducting polymers
(actuators for locomotion)

http://muri.mse.vt.edu/
A bio-inspired shape memory alloy composite (BISMAC) actuator
A.A. Villanueva, et al., 2010 Smart Mater. Struct. 19 025013 (17pp)
Want to Make Plastic ADCs!
### 6-bit A/D Converter Prototype

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>Glass</td>
</tr>
<tr>
<td>Interconnect</td>
<td>Ti/Au evaporation, litho, wet etch</td>
</tr>
<tr>
<td>Gate electrodes</td>
<td>Al evaporation, shadow masking</td>
</tr>
<tr>
<td>Source/Drain</td>
<td>Au Evaporation, shadow masking</td>
</tr>
<tr>
<td>Dielectric</td>
<td>5.7nm AlO&lt;sub&gt;x&lt;/sub&gt;/SAM</td>
</tr>
<tr>
<td>PFET</td>
<td>DNTT, ~0.5 cm&lt;sup&gt;2&lt;/sup&gt;/Vs</td>
</tr>
<tr>
<td>NFET</td>
<td>F&lt;sub&gt;16&lt;/sub&gt;CuPc, ~0.02 cm&lt;sup&gt;2&lt;/sup&gt;/Vs</td>
</tr>
<tr>
<td>Area</td>
<td>28mm x 22mm</td>
</tr>
<tr>
<td>Component count</td>
<td>74</td>
</tr>
</tbody>
</table>

Calibration enables 6-bit precision despite poorly matched capacitors

C-2C structure possible due small stray caps (glass)
Comparator

Auto-zeroing cancels threshold voltage drift

Anti-parallel PFET/NFET layout minimizes variations if $C_F$ due to misalignment
Measured DNL/INL

Before calibration, 100 Hz clock rate
Measured DNL/INL

After calibration, 100 Hz clock rate
## ADC Summary

<table>
<thead>
<tr>
<th>Process</th>
<th>3 metal complementary organic thin-film</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum feature size</td>
<td>20 μm</td>
</tr>
<tr>
<td>Chip area</td>
<td>28 mm x 22 mm</td>
</tr>
<tr>
<td>Resolution</td>
<td>6 bits</td>
</tr>
<tr>
<td>Full-scale range</td>
<td>2 V</td>
</tr>
<tr>
<td>Max DNL / INL</td>
<td>-0.6 LSB / 0.6 LSB</td>
</tr>
<tr>
<td>Clock rate / Update rate</td>
<td>100 Hz / 16.7 Hz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>3.6 μW @ 3 V</td>
</tr>
</tbody>
</table>
Summary

- More than 50 years of R&D in integrated circuit technology & design have created an incredibly powerful platform for electronic information processing
  - We are only beginning to understand what we can do with the “billions” of transistors available today

- Virtually all of today’s systems rely on highly sophisticated analog-digital interfaces
  - This makes my job exciting

- No apparent “technological” end of innovation in sight
Murmann Mixed-Signal Group