Physical CAD Changes to Incorporate Design for Lithography and Manufacturability

Lou Scheffer, Cadence

What's the problem?

- Chip designers, and CAD tools, have traditionally worried about
  - Logical correctness
  - Design rule adherence
- But all legal designs are not equally easy to make
  - New lithography considerations must be followed
  - Design features can have a big impact on ease (and cost, and yield) of manufacturing
- Designing chips to be easy to make is "Design for Manufacturing"

Why now?

- DFM was always helpful, but at sub-100nm processes it's critical
- Sub-wavelength lithography
- New materials
- Other related issues not covered in this talk
  - Timing variation
  - Process variation, and yield prediction/analysis/improvement

Today's tutorial, part I and II

- Part I: What happens after tapeout?
  - Lithography problems
  - Manufacturing problems
- Part II: covers the changes to CAD tools to address these problems

What Happens after Tapeout, and why should you care?

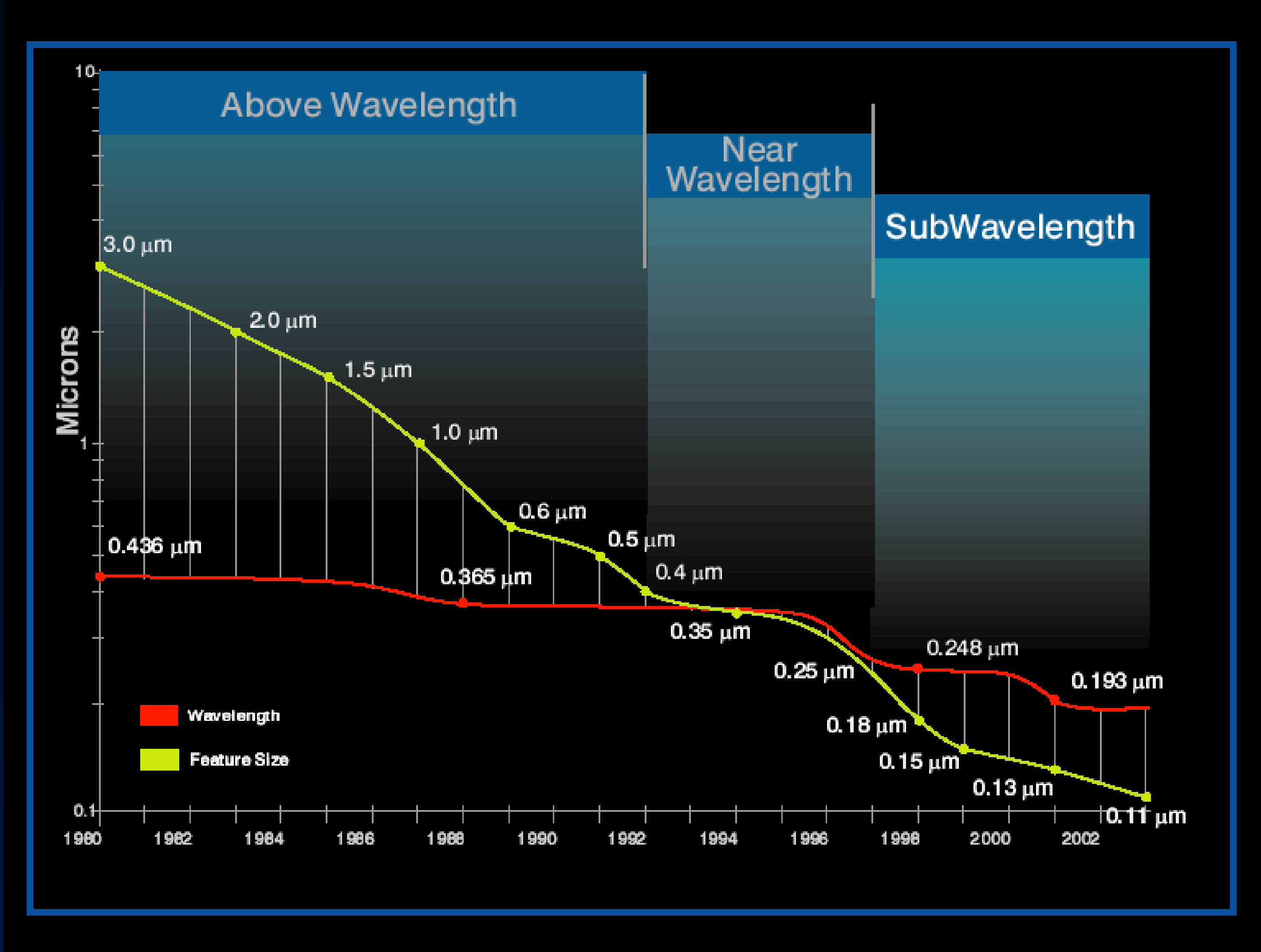
After tapeout, and before chips come back

- You need to make masks and exposures
  - Masks need optical modification
- The material must be etched
  - Leads to local density constraints
- The layers must be polished flat
  - Leads to more global density constraints
- This must be repeated for many layers
  - Leads to antenna problems
- How well you do these steps determine yield

Masks and Exposure

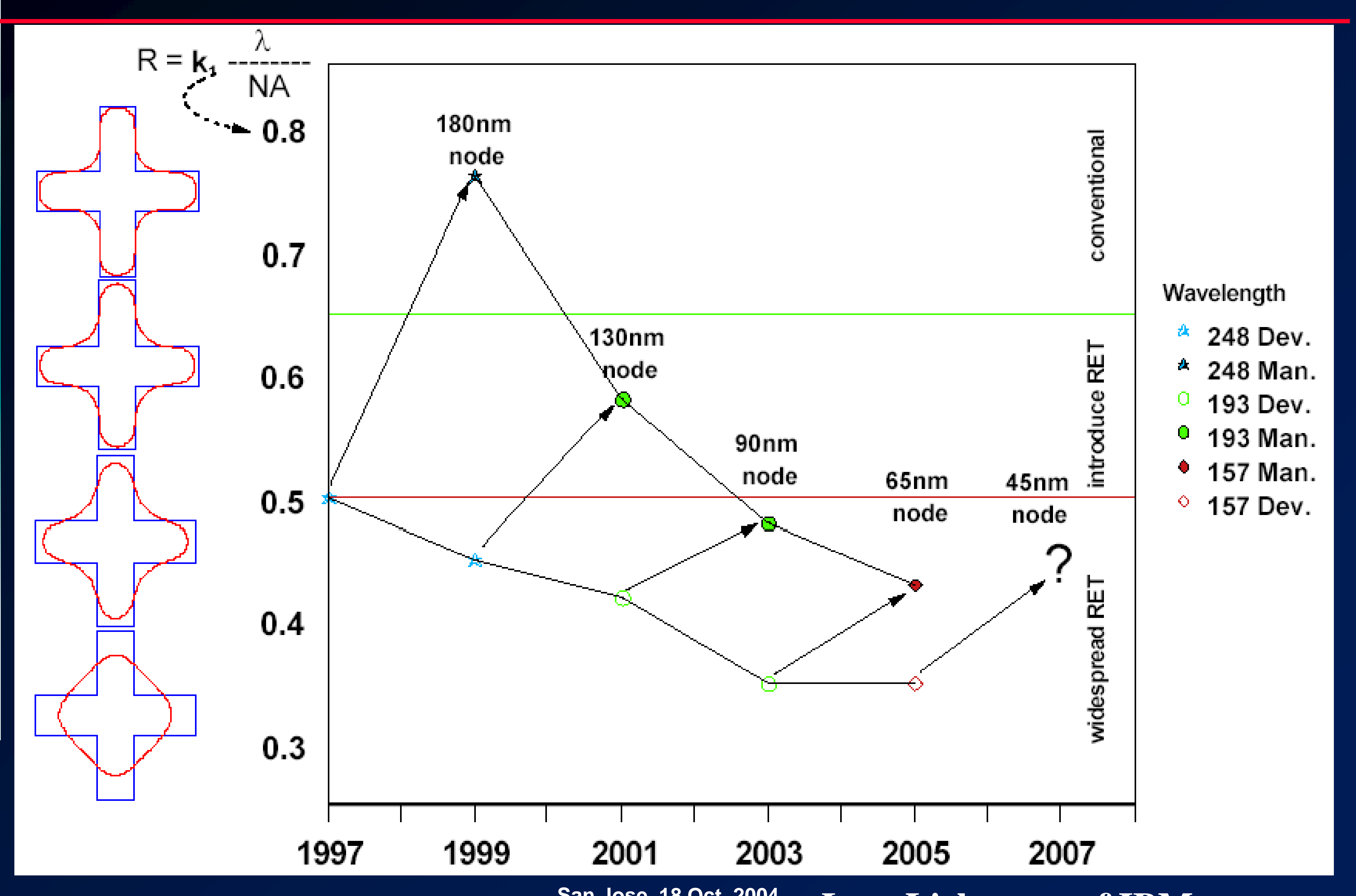
- Long ago, we exposed 1 micron (1000 nm) features with 300-400 nm light (relatively easy)
  - The mask looked the same as the polygons
- Now we are exposing 90 nm (and soon 65 nm) features with 193nm light
- Now, it looks very different
  - Lots of tricks are needed
  - Difference between a photo and a hologram

Wavelength used vs process generation

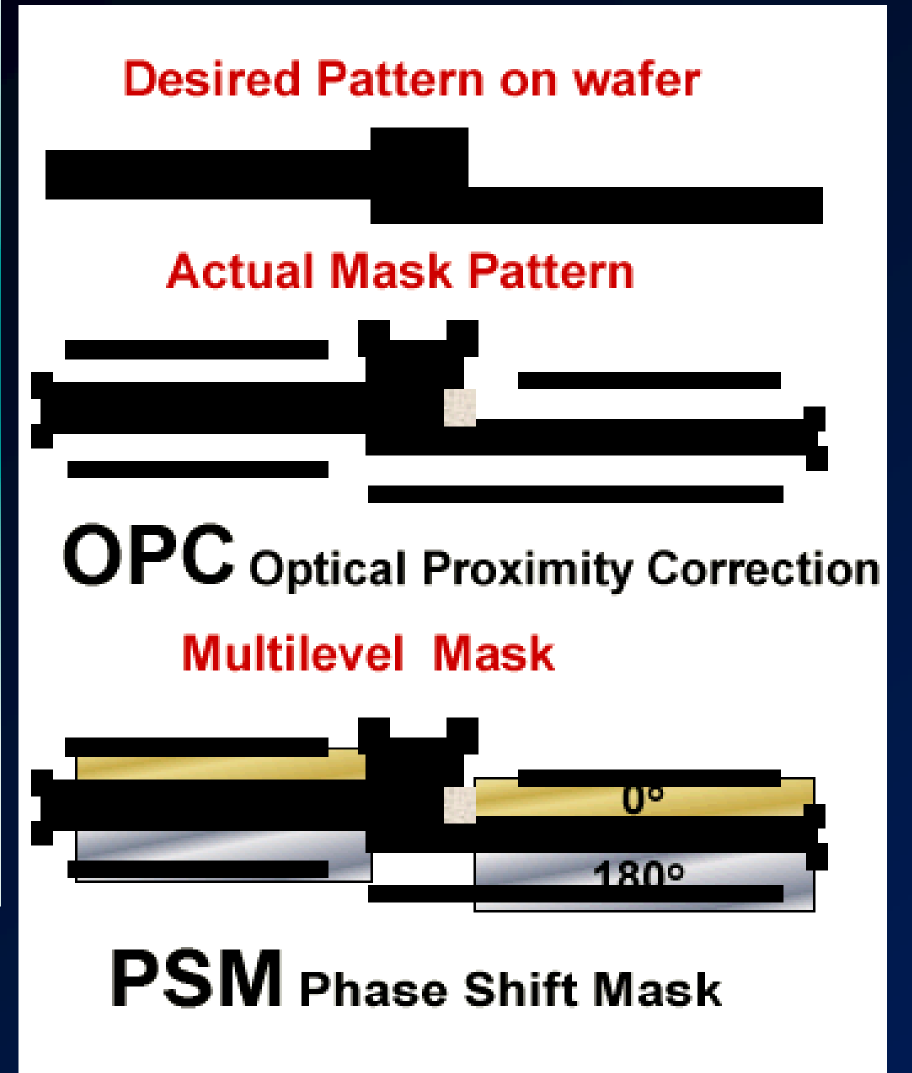


From Numerical Technologies

How a polygon comes out at differing K_1, and K_1 for different process variations



Example of OPC and PSM



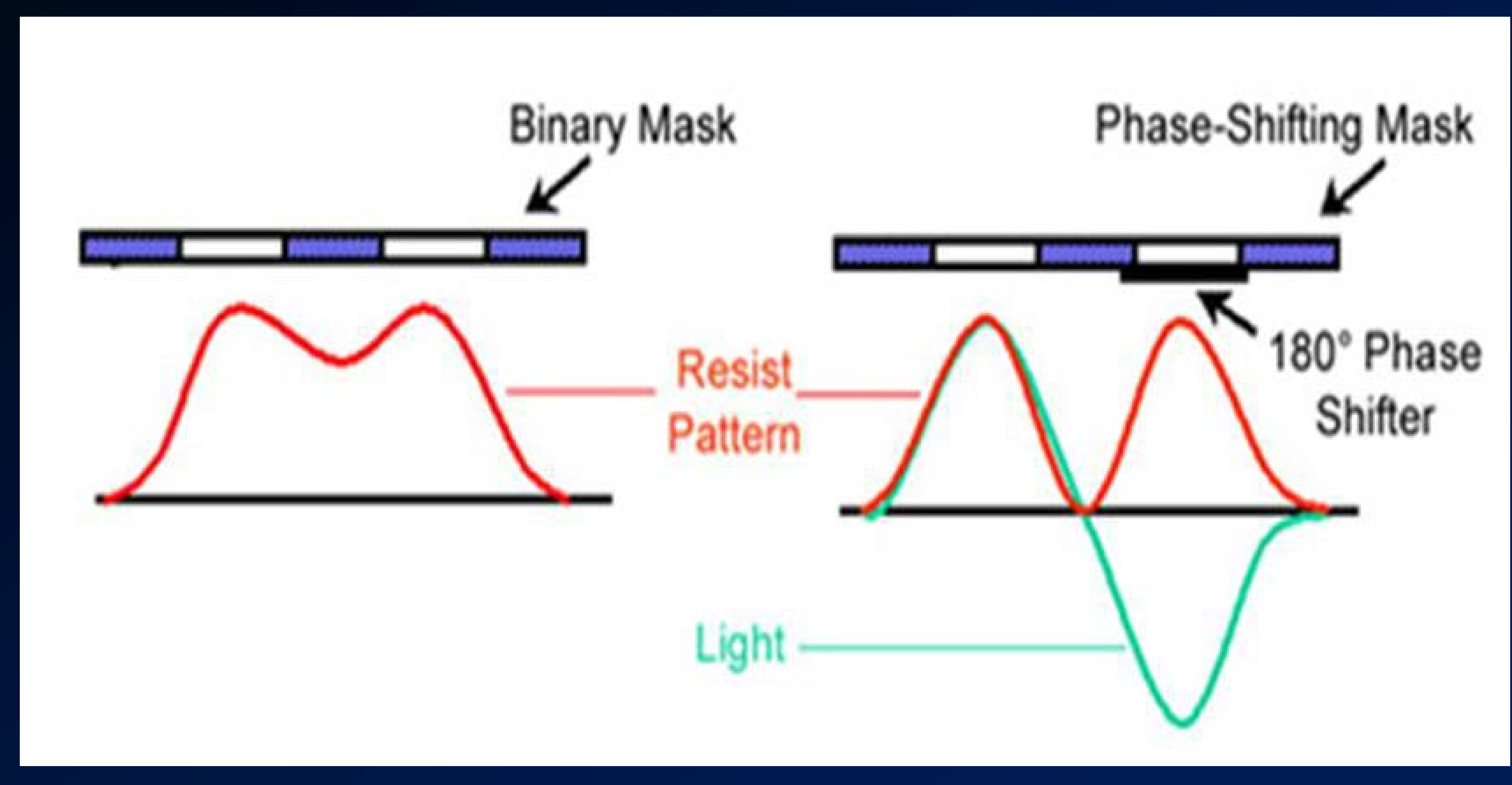
This is what the designer drew

Added 'scattering bars' and serifs to make the polygon print more exactly

Added additional phase features to allow printing smaller features at the same wavelength

From Andrew Khang

How Phase Shift Masks Work



Lots of lithography tricks is an understatement

- Entire conferences, journals and working groups devoted to this topic
  - And sessions at DAC, ICCAD, DATE, ISPD, ASP-DAC and so on
- SPIE has a MicroLithography symposium each year, comprised of 6 conferences
- One of these conferences, Design and Process Integration, specializes in the subjects of this tutorial
- See the SPIE web site: http://www.spie.org

New techniques are being developed

- Dual mask techniques
  - One prints big features and one sharp edges, or
  - One prints horizontal and one vertical edges.
- Lots of new techniques under investigation
  - Attenuated PSM
  - DDI – Double Dipole illumination
  - CPM – Chromeless Phase Mask
- Each new technique has different limitations

Can the process developers bail us out?

- Shorter wavelength (157 nm)?
  - This is turning out to be harder than was thought
    - Calcium Fluoride shortages, birefringence problems, etc.
- Immersion lithography?
  - Fill the space between the lens and wafer with water
  - Light goes slower in water so wavelength is less
  - Physics well understood, but lots of practical problems
    - Bubbles
    - Lens moves over wafer in scanning
    - Temperature control

RET – Resolution Enhancement Techniques

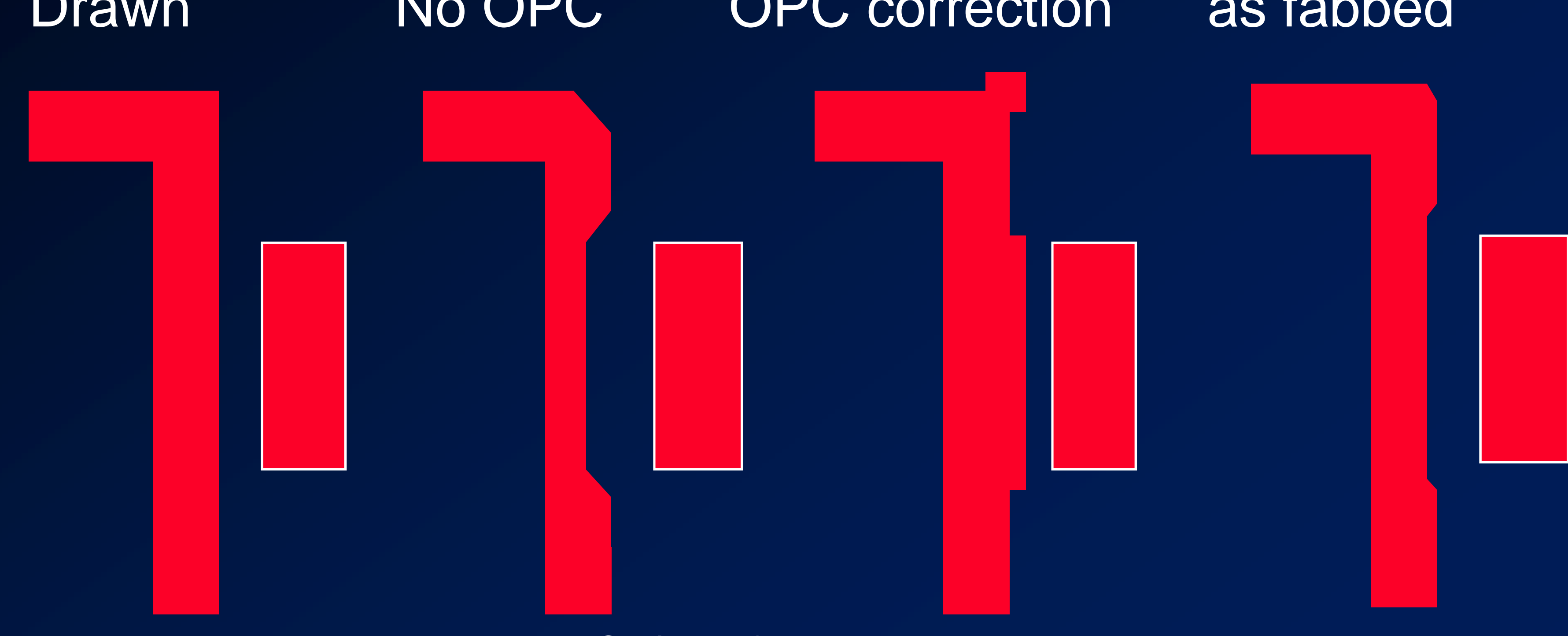
- If we can't use a shorter wavelength of light, then we must use RET (Resolution Enhancement Technology)
- This is a generic term for modifying the mask so that it prints better
- Specific cases we have seen are
  - OPC – Optical Proximity Correction
  - PSM – Phase Shift Mask
- Many other techniques are possible

OK, so the mask guys are really tricky

- But why do I (as a designer) care?
- Three reasons:
  - Corrections are not complete
  - Some designs cannot be built at all with certain RET technologies
  - Of those that CAN be built, some are more manufacturable after RET than others

Corrections are not complete

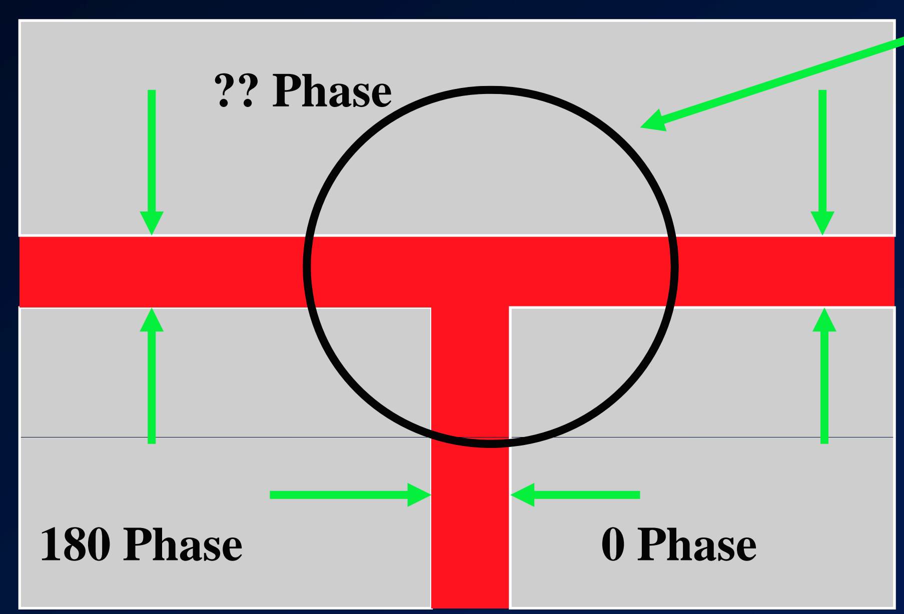
- If RET worked perfectly, designers could ignore it
- But as we scale down in R, corrections are not complete



Some features cannot be corrected

Odd Phase cycles – Classic example, T junction

To get minimum width, phases must be opposite

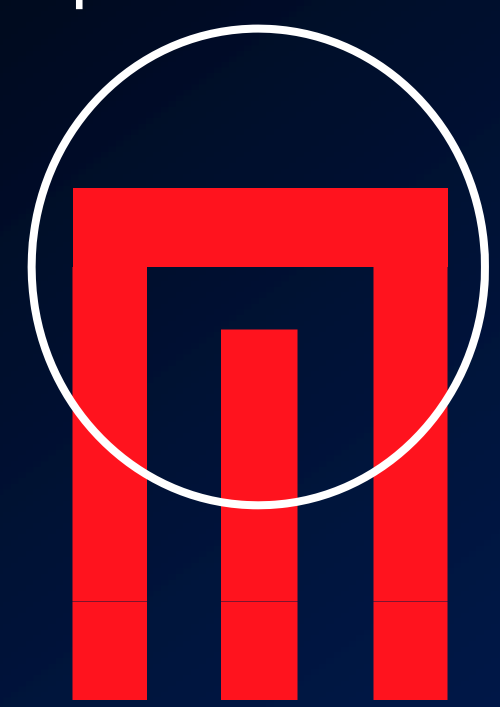


As you go around this circle, you encounter an odd number of regions which require a phase assignment

All three lines cannot be minimum width

Features that cannot be corrected

- Just eliminating T junctions does not solve the problem

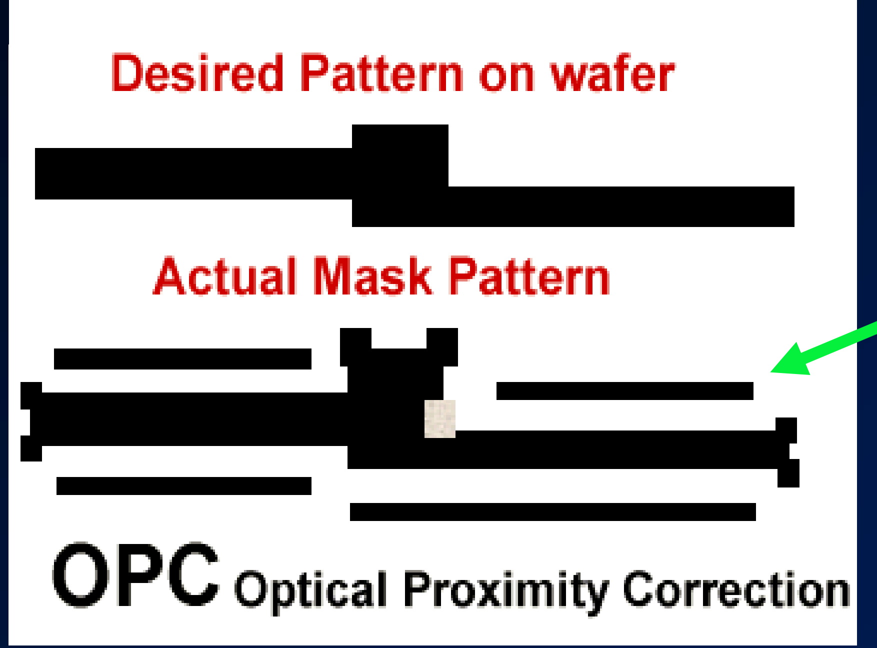


•Errors can be hard to localize, much less correct

•What does the designer do if the OPC tool warns of a cycle of length 47?

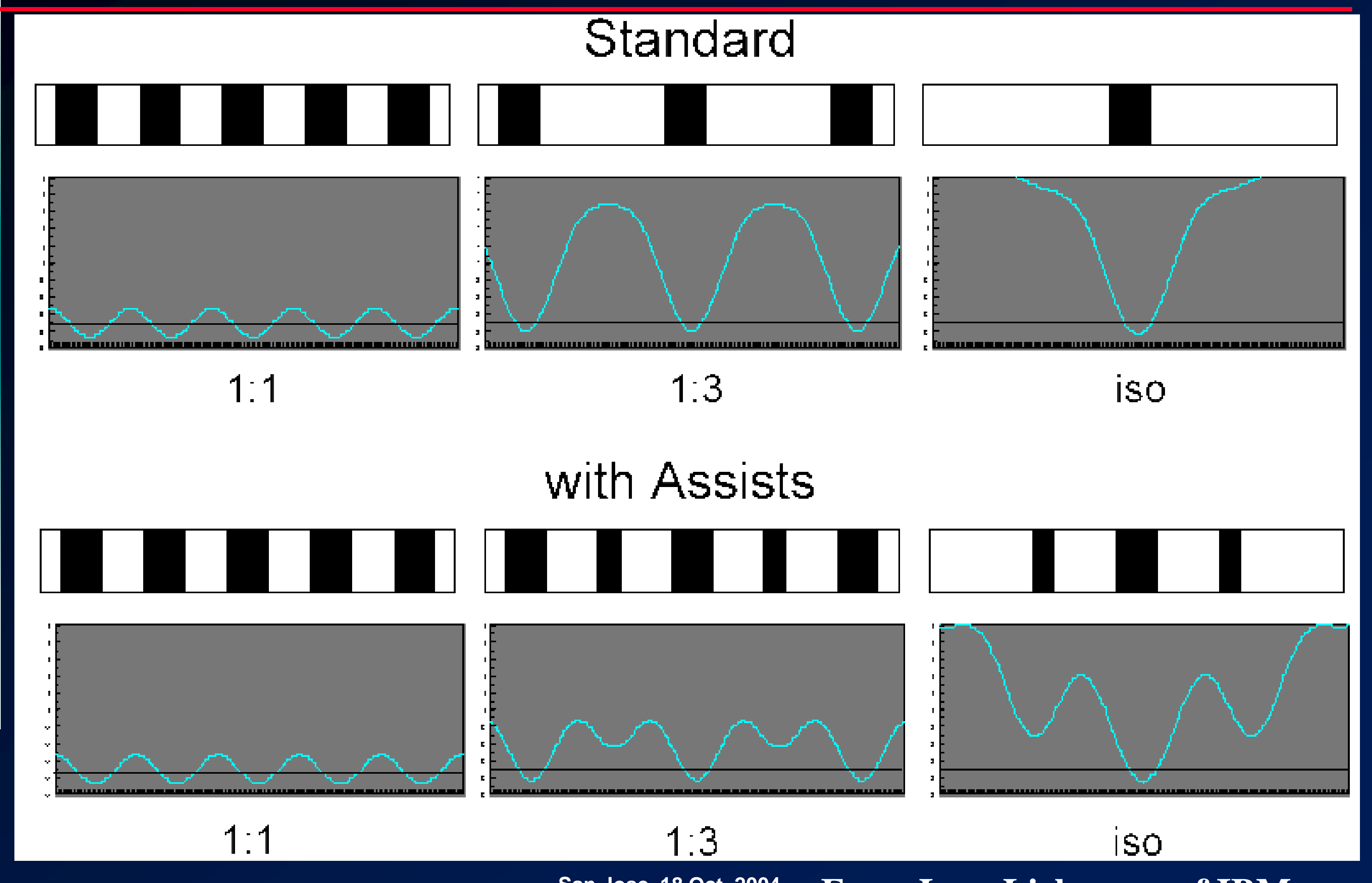
Features that work, but hurt manufacturability

- Example – scattering bars



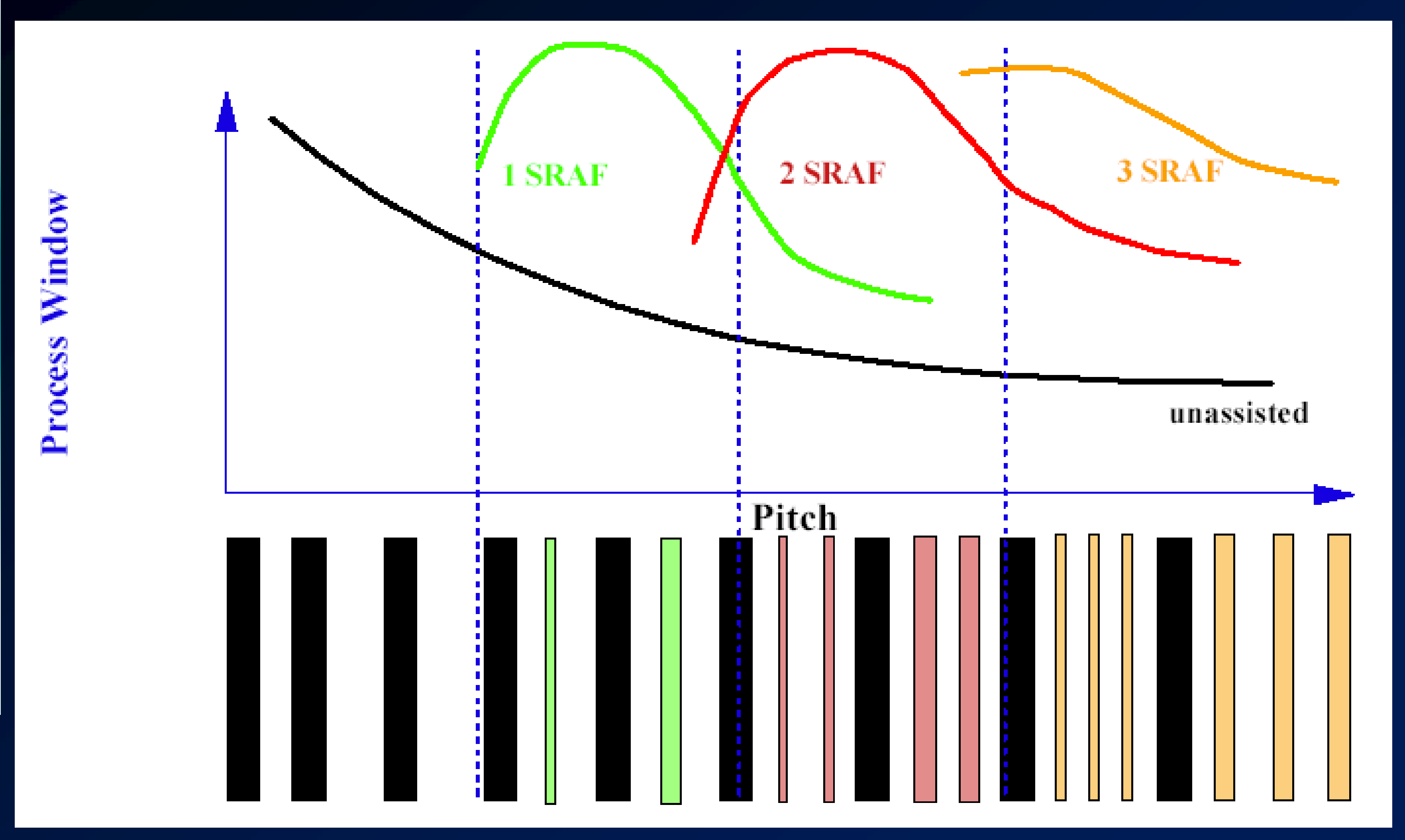
Scattering bars are these extra lines. They do not print themselves but help the other features print with larger process latitude

Here is how scattering bars work



From Lars Liebmann of IBM

This leads to ‘forbidden’ pitches



From Lars Liebmann of IBM

Features that work, but hurt yield

- Forbidden pitches are not really forbidden, unlike odd cycles.
- They will work, but force sub-optimal scattering bar insertion
- This leads to a smaller process window and hence more difficult manufacturing, and lower yield

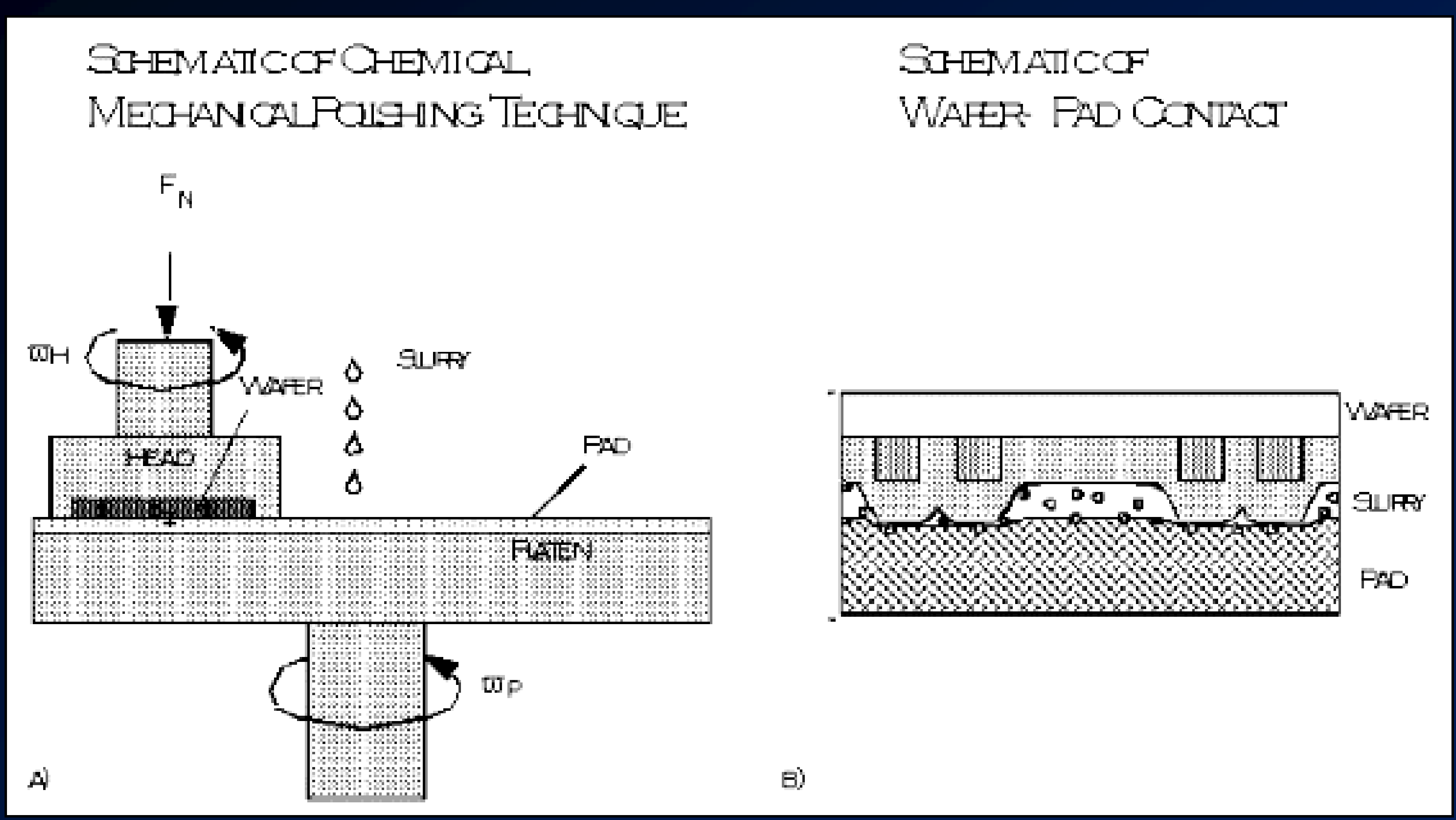
Two basic approaches to dealing with RET

- Basically, knowledge or methodology
- Knowledge: Designers and/or CAD tools aware of RET, design around it
  - Analog, SRAM, and DRAM folks will do this
  - Standard Cells may do this
  - For full custom, it's a lot to expect of designers, few will do this
  - Digital designers will never do this
- Methodology: Very strict design rules
  - All critical dimensions uniform spacing and one orientation
  - Mask must be a subset of a uniform grating

Etching and polishing

- Even if we can expose the wafer with the right shape, we are not done yet
- Still need to build and etch the metal, then polish it flat so we can build the next layer
- Etching – local loading effects
- Polishing – more global effects
  - CMP – Chemical Mechanical Polishing

CMP – Chemical Mechanical Processing

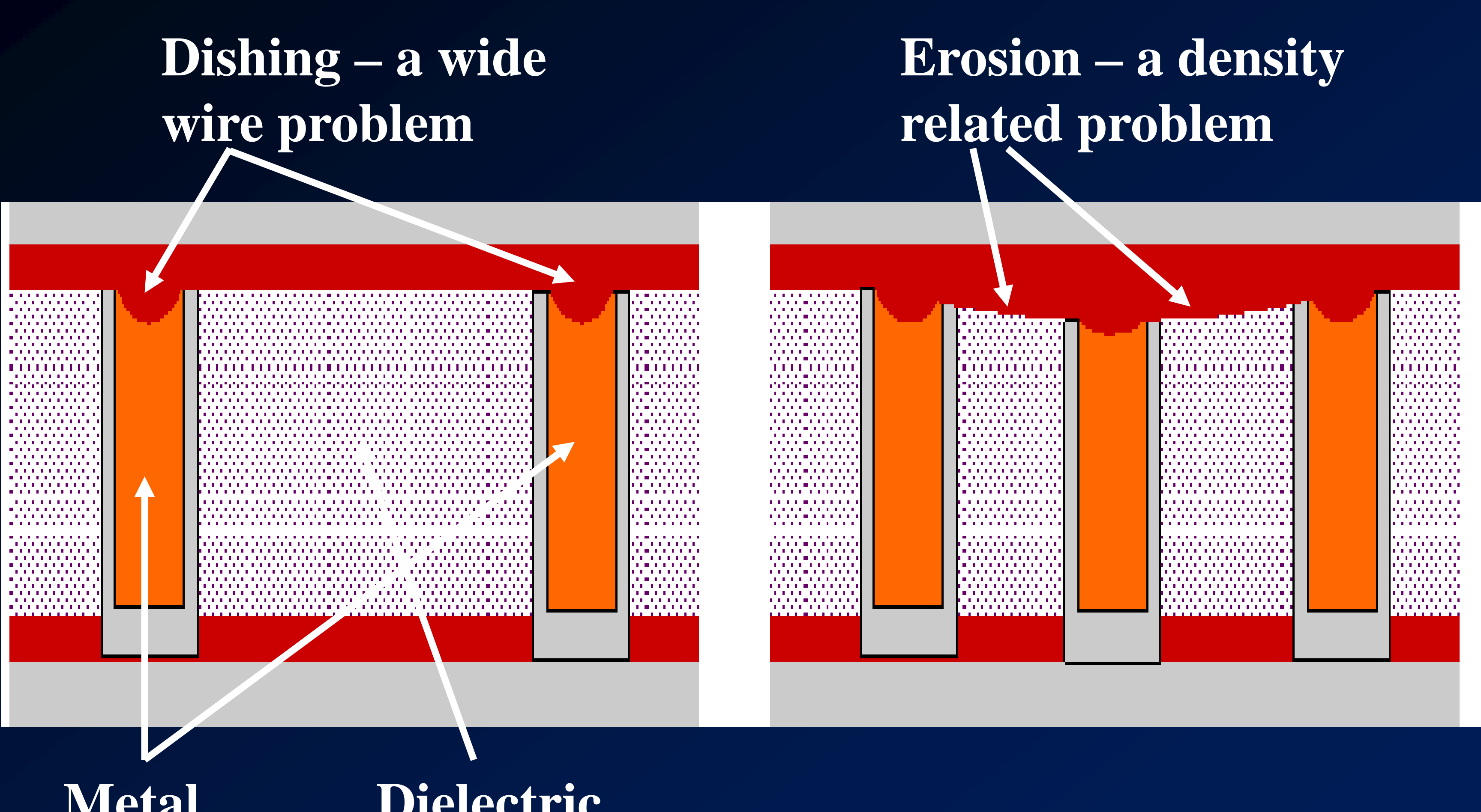


From Fraunhofer Institute web site

Etching and CMP

- Etching Problems
  - Plasma becomes more heavily loaded in regions of high density
  - This is a relatively short range effect (a few microns)
- Polishing Problems
  - Oxide and metal are different hardnesses
  - Therefore they etch at different rates
  - This occurs over hundreds of microns
- Solution: Try to keep density constant over all scales

Problems with CMP: Erosion and dishing



Solution – keep density uniform

- Keep density from getting too high by adding 'wide wire' rules
- Keep density from getting too low by adding 'metal fill'
- But these clearly impact
  - Coupling
  - Critical area
  - Yield

Metal Spacing and Density (cont)

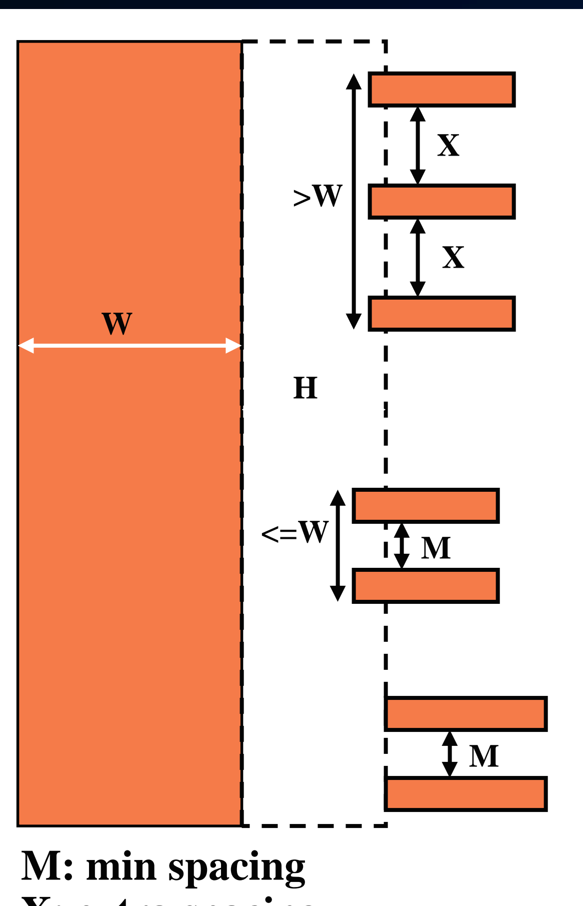
Maximum density rules "helped" by wide-wire spacing rules

- Implicitly enforces a local density rule
- Helps global density, but no guarantee
- Also helps with etch loading

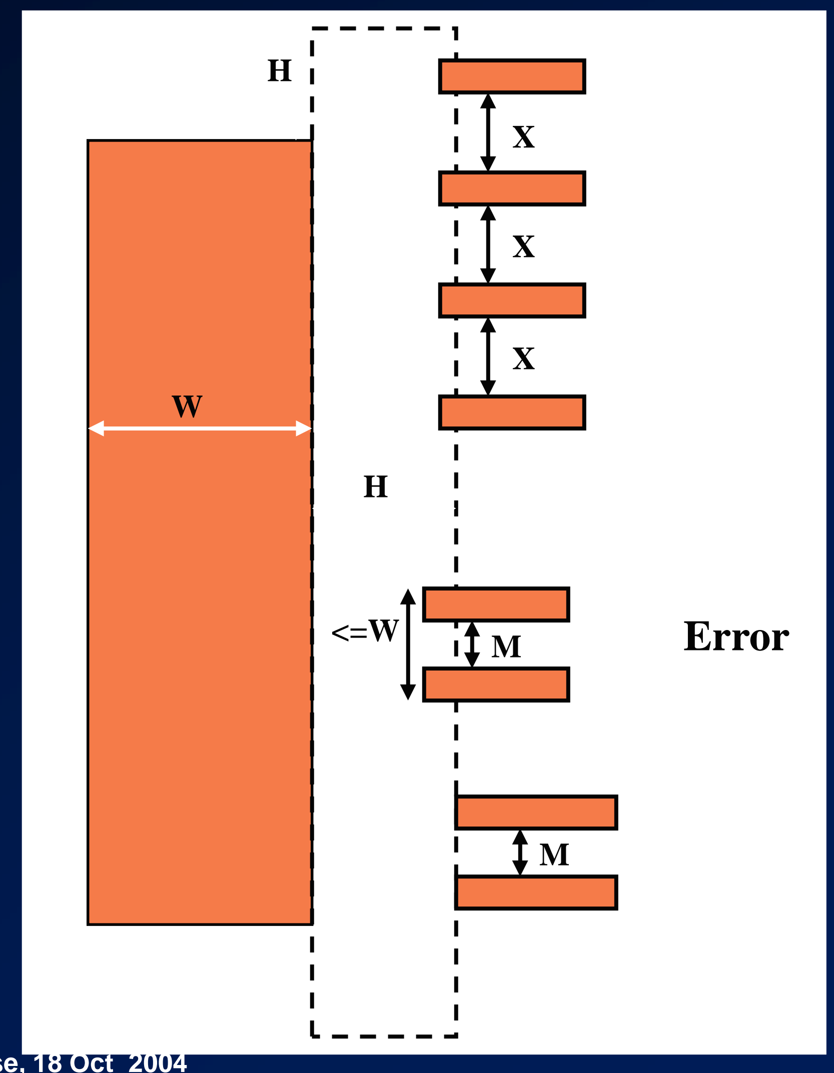
Width	Spacing	Max Density
0.15um	0.15um	50-60%
0.22um	0.20um	52-88%
1.50um	0.50um	75-90%
4.50um	1.5um	75-83%
7.50um	2.5um	75-83%

Metal Spacing and Density (cont)

New Vicinity/Influence rule (two versions)



M: min spacing
X: extra spacing
H: halo size
W: wide-wire width



Metal Spacing and Density (cont)

Local density rules enforced by wide-wire vicinity rules

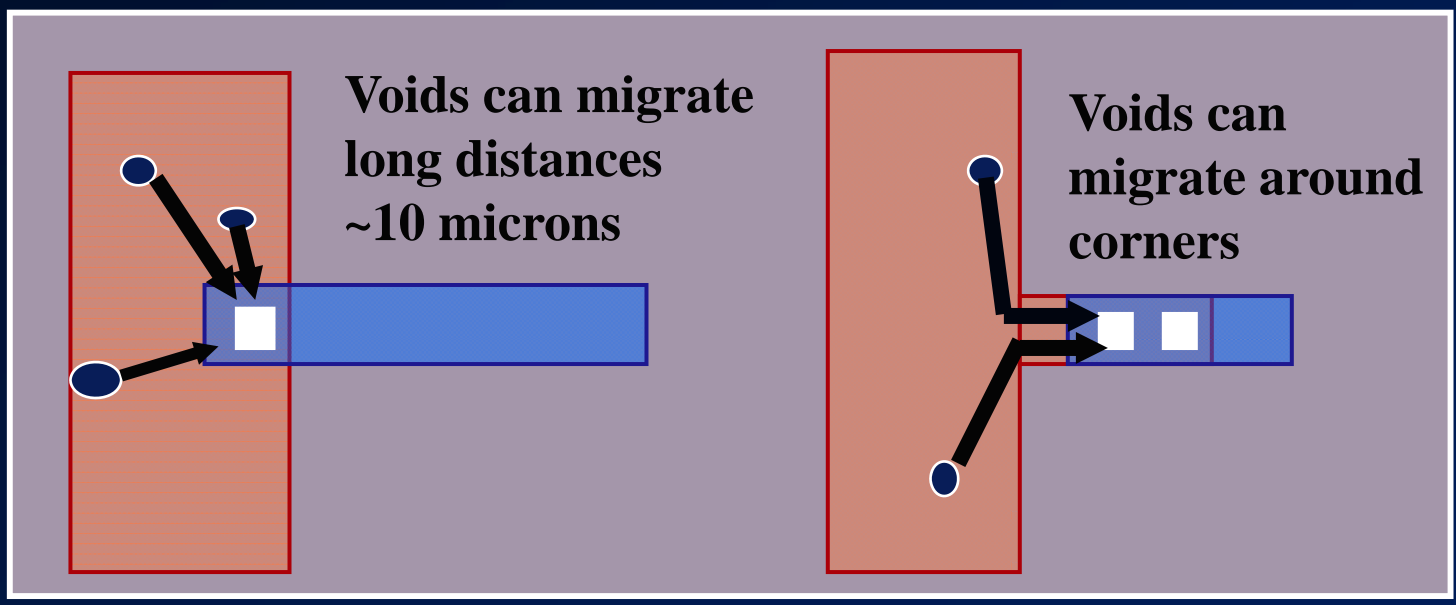
- values vary even inside same consortium
- helps global density, but no guarantee

Width	Halo	Spacing
0.15um	NA	NA
0.22um	0.20*	0.20*
1.50um	0.50um	0.50um
4.50um	1.5um	1.50um
7.50um	2.5um	2.50um

*may be removed

Via Void Problems

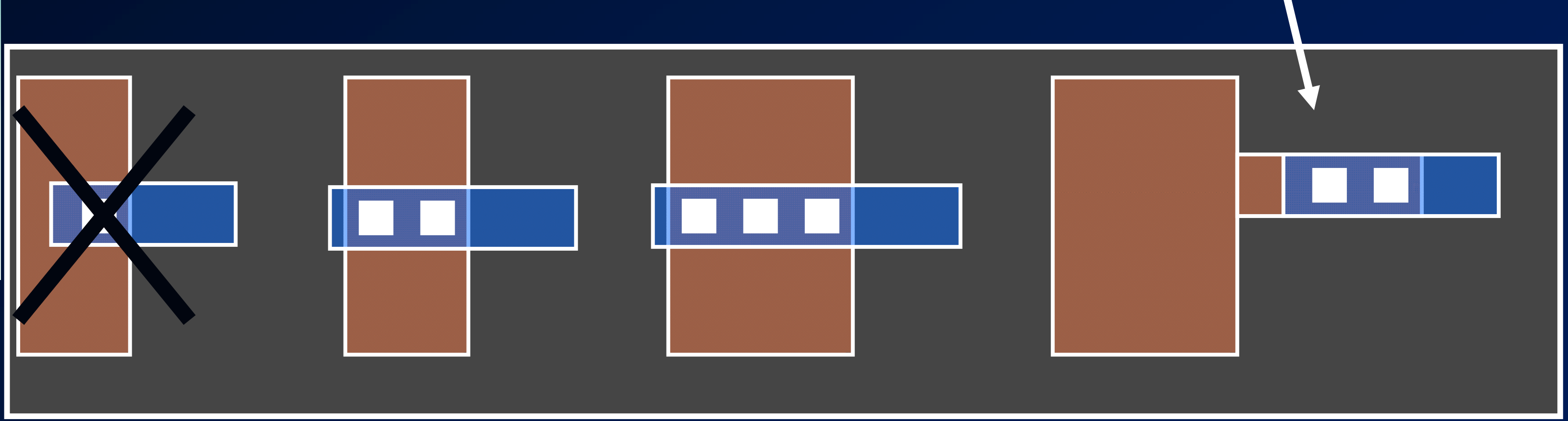
- Copper processing causes new problems for vias
  - Voids in Cu migrate under thermal stress towards vias
  - If enough voids migrate to a via it can cause failure
  - worse at 90/65nm due to increased stress of smaller via



Via Void rules

- To keep reliability acceptable, need more vias
  - Need 2, 3 or 4-cut vias when connect to wide-metal
  - Does not depend on the current carried

applies to "close connections" of wire-wires also



Antenna rules

- Antenna rules have nothing to do with traditional definition of antenna
  - Really a collector of static charge, not electromagnetic radiation
- Only happens during manufacturing
- Problem introduced with plasma etching, many process generations ago
- Not a new problem, but sub-100nm materials may make it a lot worse

Antenna Rules – a Review

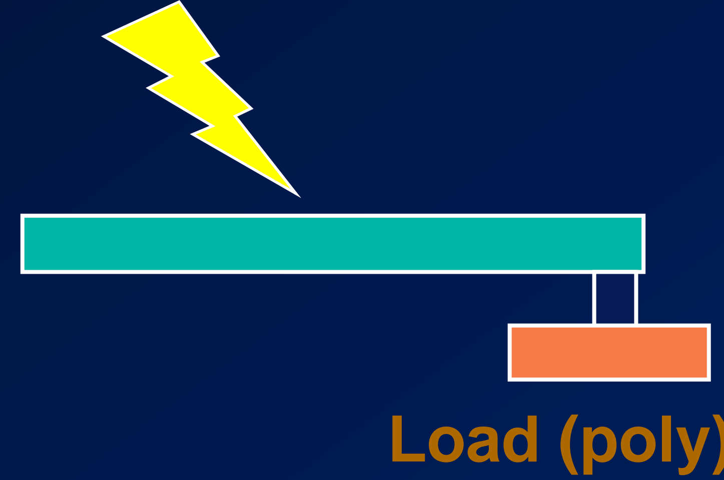
- A long line connected to gate only can cause failure
- Not a problem after chip is complete since every net has at least one driver

Antenna Rules

- But, we can have a problem during manufacturing
- Here is the same net after M1 is built, but not yet M2
- Error!

M1

Driver (diffusion)

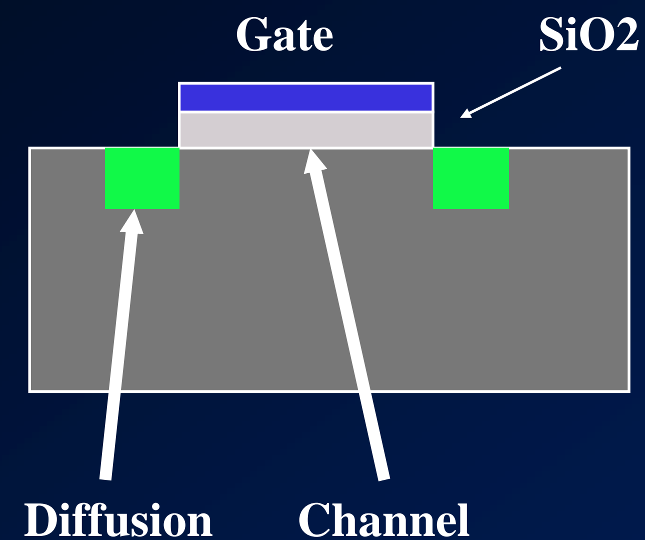


Gate leakage and materials

- Gate leakage is <u>helpful</u> for antenna problems
  - Leakage does not hurt the oxide
  - Keeps voltages from getting to dangerous levels
  - Thin oxide has higher area ratios allowable
- But gate leakage is creating horrible standby power problems
- Process engineers are trying to switch to high-K materials to help the standby leakage problem
- But this will (probably) make the antenna problem much worse!

Why high K for gates?

- High K allows thicker gate oxide
- Here's the cross section of a transistor
- High K material replaces the SiO_2 of conventional gates



Transistor with high K gate oxide

Why high K?

- Capacitance is the same
  - No additional loading on prior gates
- Field at the edge of the dielectric is the same
  - Transistors have the same performance
- Dielectric is much thicker
  - Leakage is reduced exponentially (to negligible levels)
- Great in theory, but a hard material problem
  - Must be easy to make and reliable

Conclusions

- A lot happens between tapeout and working chips coming back
  - Mask making
  - Etching
  - Polishing
  - Stacking layers
  - New materials cause new problems
- Designs can help or hinder these efforts

CAD Tool Changes for sub 100nm Lithography and Manufacturability

Outlined a number of mfg problems

- OPC rules
- Metal density
  - Local and global
- Antenna rules
- In general, three approaches to new rules:
  - Design tools (and designers) know about these problems
  - Post processing corrects these problems
  - Methodology changes to avoid these problems

Rules in general are more complex

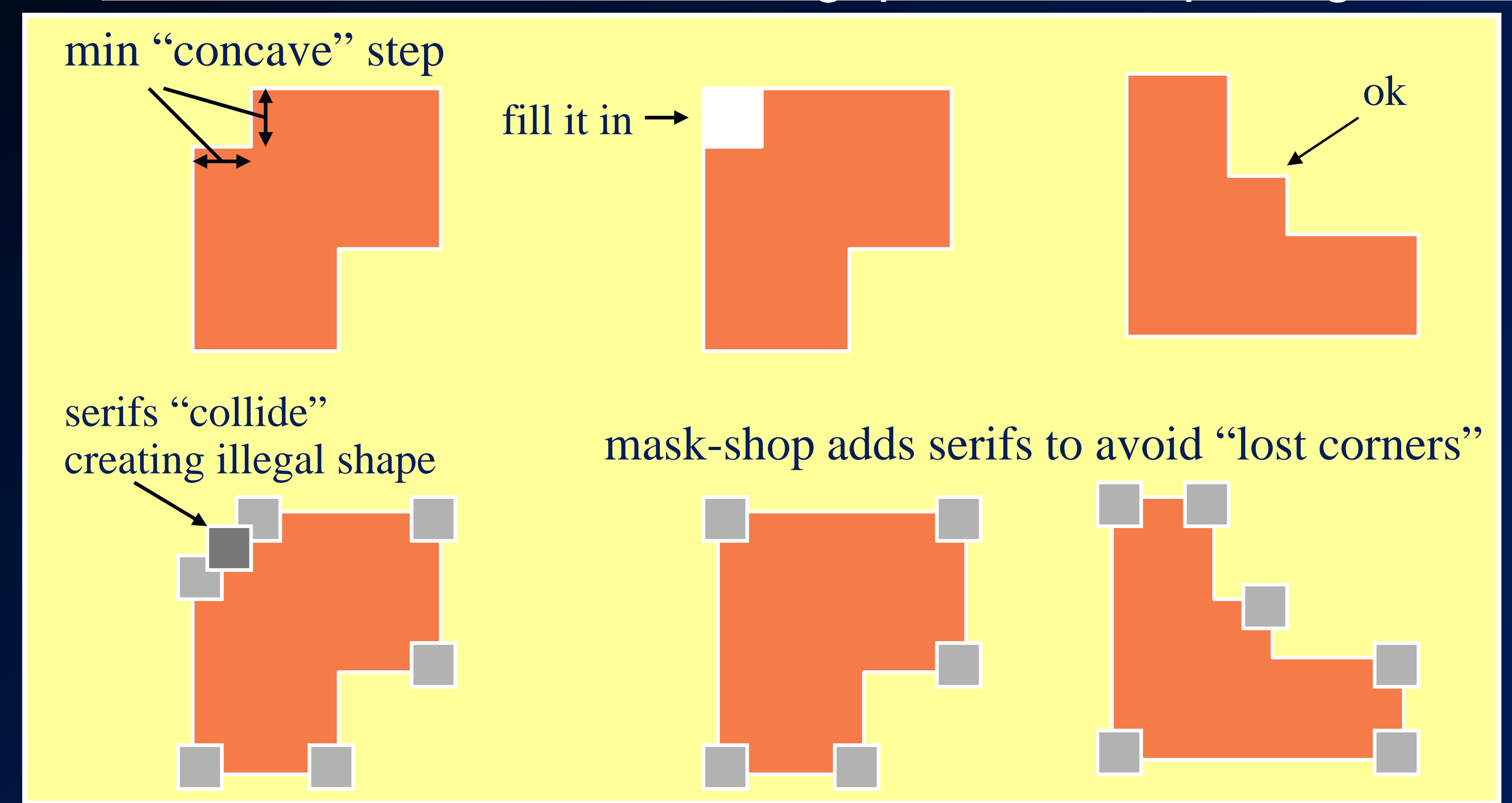
- There are roughly 600 design rules for a typical 90 nm process
- Example: Wide wire spacing rules
  - These must be understood by the router
  - Cannot be fixed by post-processing
- In addition, many ‘recommended rules’ that affect manufacturability
  - Extra spacing if room available
  - Redundant vias if possible
  - Extra enclosure around contacts if possible

OPC driven changes

- Downstream OPC usually requires limitations on geometries
- Exact limitation depends on OPC chosen
  - OPC for 90nm is already decided and factored into design rules. Mainly impacts the poly mask.
- OPC, and mask technology, for 65 nm node is still unclear

Metal OPC Rules

- Small steps cannot be "fixed" by OPC rules
  - add commands to fill in the gap, then do spacing check



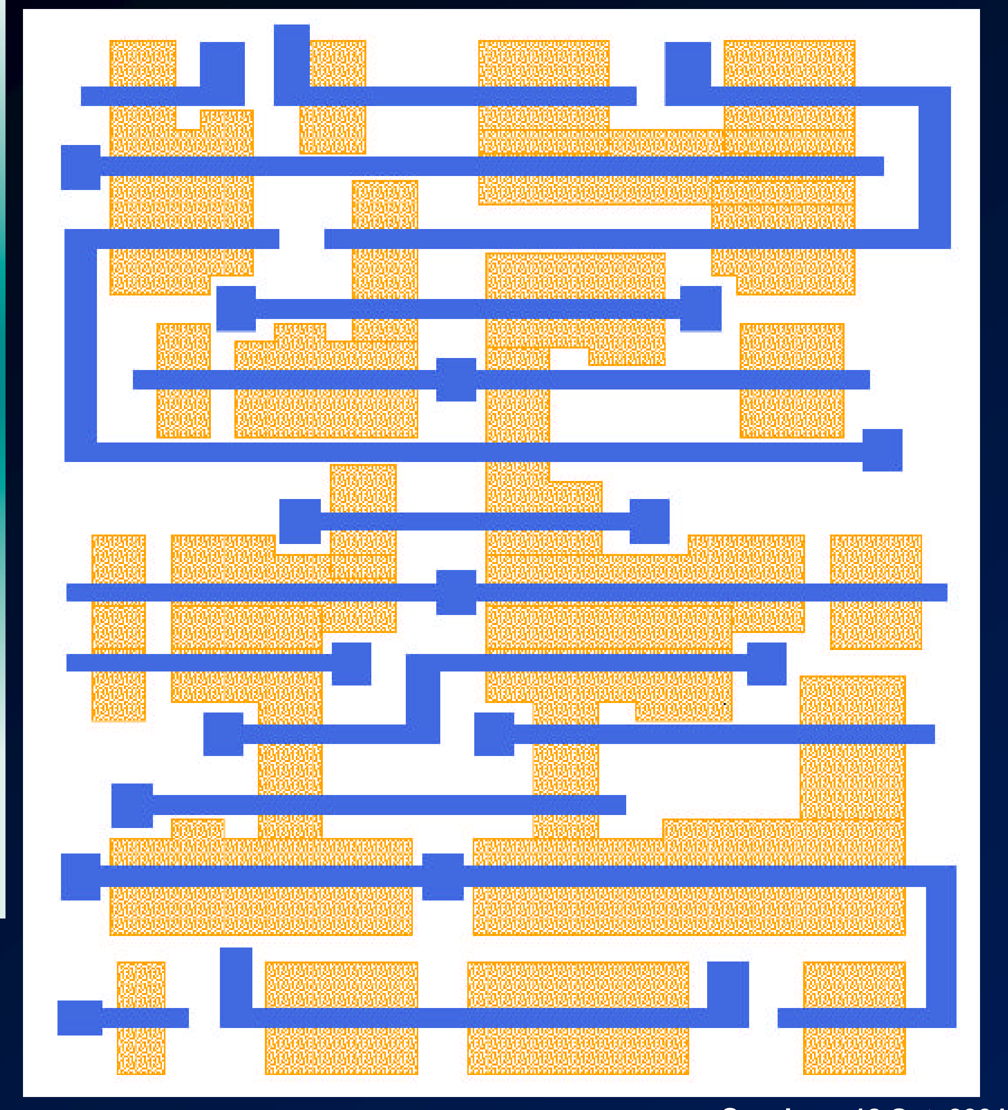
Phase shift rules

- Depends on whether you have dark field or light field exposures
  - Assign phases to the gaps or the polygons
- Where you cannot get good phase assignment, need to use larger rules
- In general, cannot fix violations (at least well) by post processing
- Therefore, routers (and designers) must understand these constraints
- New tool – “Phase compliance checker” to see if phase assignment is possible

An Alternative: Methodology fixes

- Lars Liebman of IBM is the champion of the school that proposes very strict methodology
- We don’t know what lithography will win at 65 and 45 nm
  - Immersion, PSM, double dipole, etc.
- Each lithography method has different limitations
- But all proposed techniques are good at equally spaced lines and spaces (a grating)
- Therefore, build your layout (at least the critical masks) to look as much like a grating as possible
  - All critical dimensions in one direction and equally spaced.

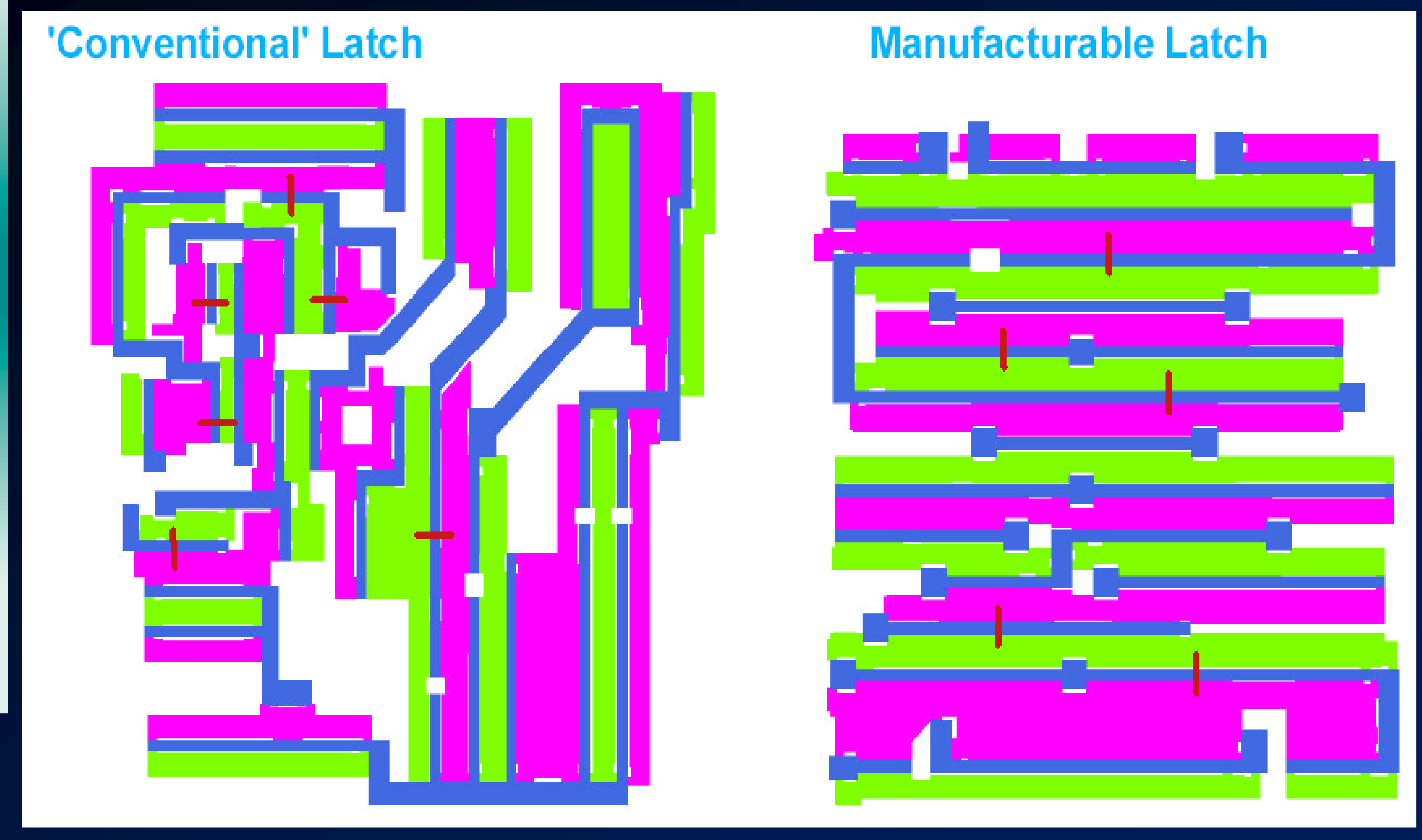
Example of a 'strict' methodology design



- All transistors are horizontal
- All gates on a common pitch
- All wrong way routing uses wider (non-critical) dimensions
- Easy to assign phases
- But won't this cost area?

Source: Lars Liebmann of IBM

Not clear if this costs any area!



Source: Lars Liebmann of IBM

Metal Spacing and Density

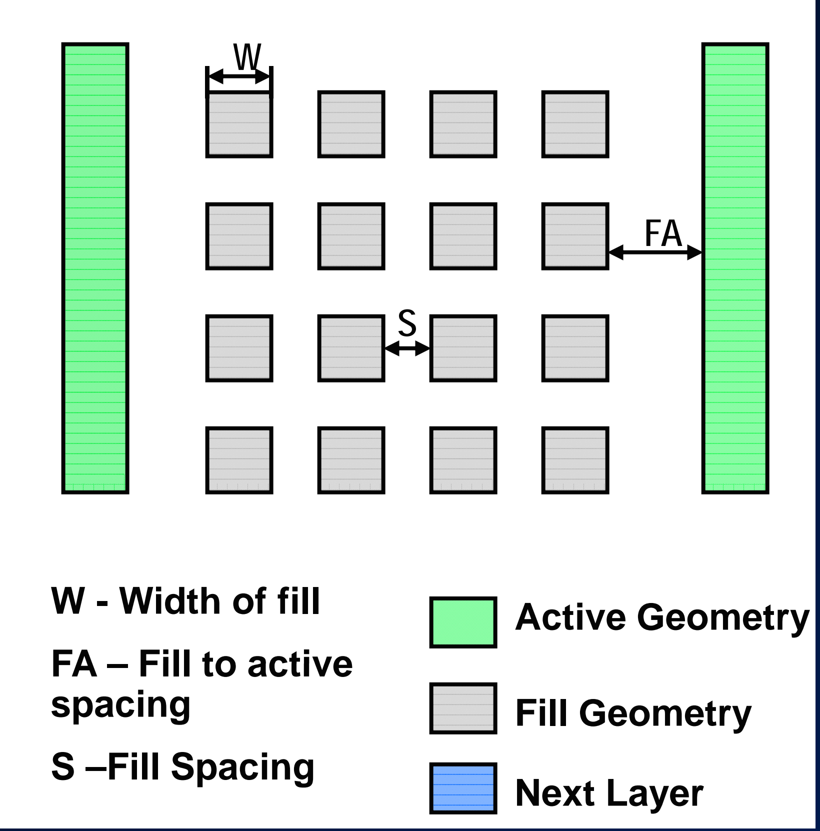
- Caused by CMP (Chemical Mechanical Polishing)
  - metal and dielectric thickness varies due to metal density (thickness varies by +/- 30% without rules)
- Multiple density rules for different window sizes
  - 20% to 70% for 100x100um windows
  - 20% to 65% for 500x500um windows
  - minimum met by adding dummy metal (metal fill)
  - maximum "helped" by wide-wire spacing rules
  - local maximum density enforced by spacing rules
  - Need new verification commands check/fix densities
  - rules keep thickness variation to ~ +/- 10%

Several different methods for density control

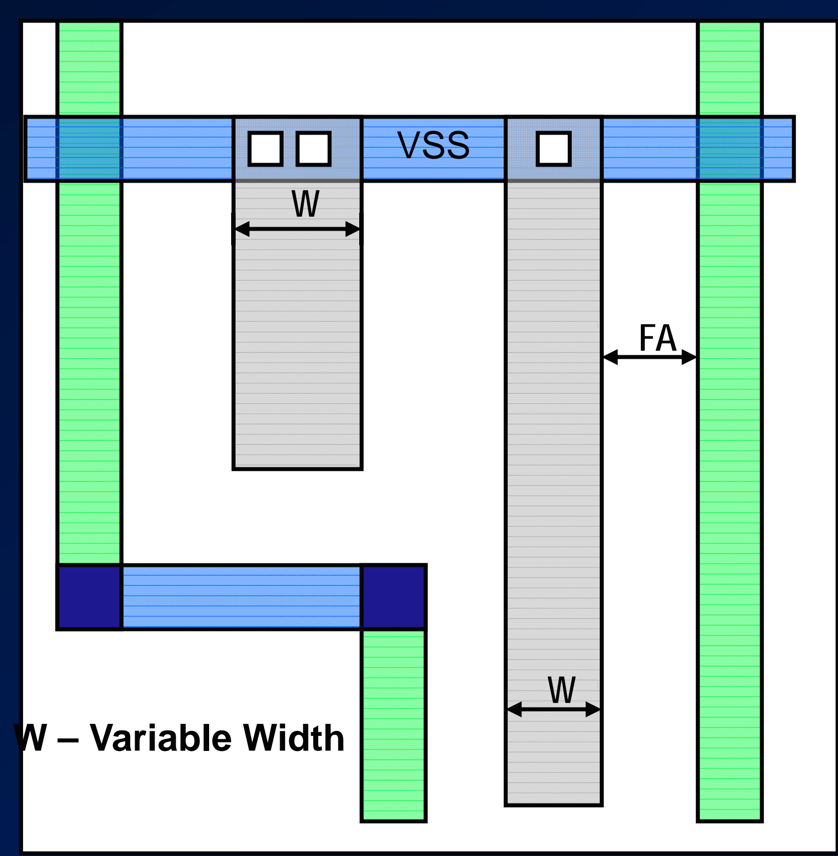
- Who does the fill?
  - The router?
  - A post-processor?
- How do we do the fill?
  - Add patterns of rectangles
  - Add wires
- Handling maximum width rules
- What do you do if the density is too high?
- Target a density versus meeting the rules
  - Rectangle count (and mask cost) versus yield

Metal fill to fix low densities

Traditional Metal Fill Method – Done by Post-Processing



Alternative Metal Fill Method – Done by the Router



Conflict between vendors and designers

Pros and cons of post-processing for fill

- Traditional (post-processing) fill requires no help from the router
  - Works on arbitrary designs
- However, it introduces uncertainty in timing
  - Minimized by keeping the fill far from nets
- And uncertainty in coupling
  - Since the inserted metal is floating

Pros and Cons of router-created fill

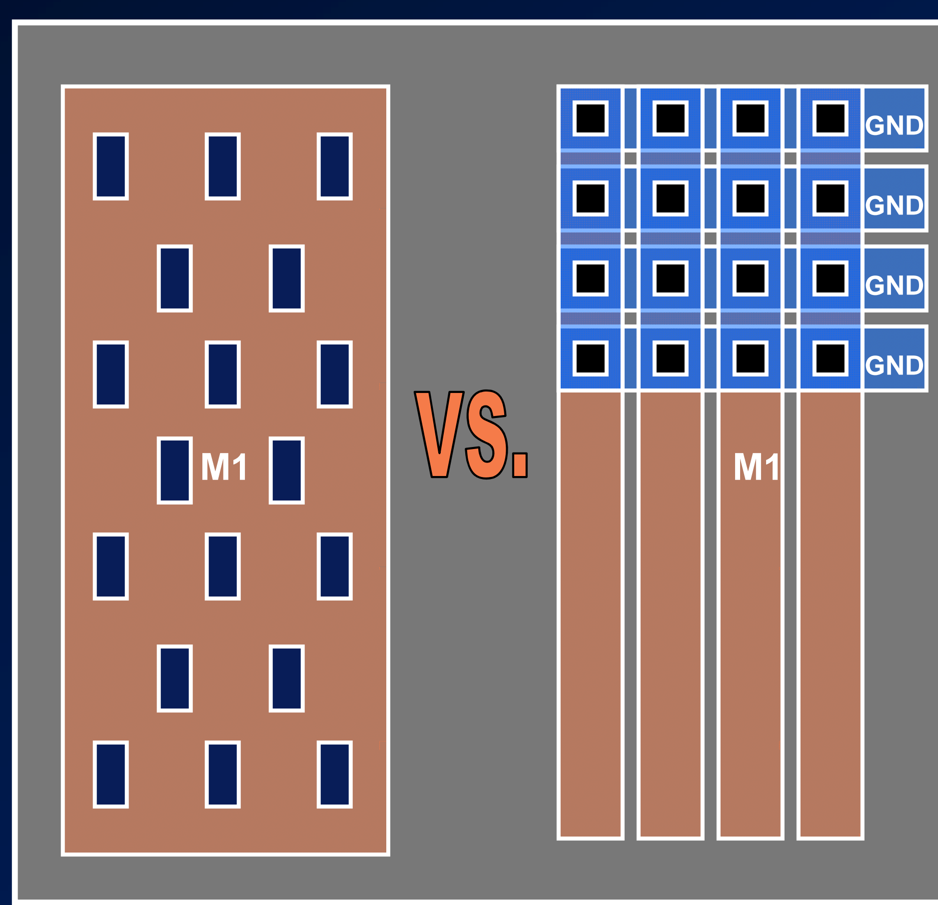
- Fewer polygons
- Most inserted polygons are grounded
  - Helps crosstalk rather than hurts it
- Fill geometry and effects are known when the designer does extraction
  - This is crucial, since that's when they can be corrected
- But the router must be smarter
  - Insert fill, grounded fill, remove fill for ECO, etc.

Smarter extraction

- Even after fill, density will not be completely uniform
  - IP blocks, RAMS, etc. often cannot be adjusted.
- Metal thickness in general depends on density
- Wide wires suffer dishing
  - R per square depends on the width
- Need extractor technology that handles CMP effects

Maximum Width rules

- Due to thermal stress and local density rules
- Maximum wire width can be quite small
  - > 2.5um needs slots in some 90 nm processes
- Post-layout slotting versus “bus” of thin wires



Pros and cons of slotting as a post process

- Advantages of adding slots as a post-process
  - Easy on the designer
  - Power routing tools do not need to worry about maximum width rules
  - Manual editing of routes is easy – they are simply a very wide wire at this stage
- Disadvantages:
  - Slots may not be aligned with current flow
  - Via arrays are very hard to correct
  - True IR drop not known until after slotting

Pros and Cons of Slotting by the Power Router

- More difficult for power router
  - Needs to understand maximum width rules
- Needs special understanding for manual editing
  - Must understand a bundle of small wires is a single construct
- However, IR drop is becoming more critical
  - Lower VDD
  - Higher power
- Slots are aligned with the current flow
- Via arrays are handled very naturally
- Router driven slots lets designers fix problems

Dealing with Maximum Density rules

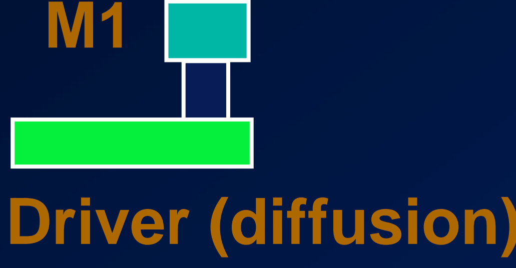
- What if your maximum density is too high?
- This can happen if you (for example) have a bus of wide wires.
- No plausible post-processing can fix this
- Tools must be aware of this limitation

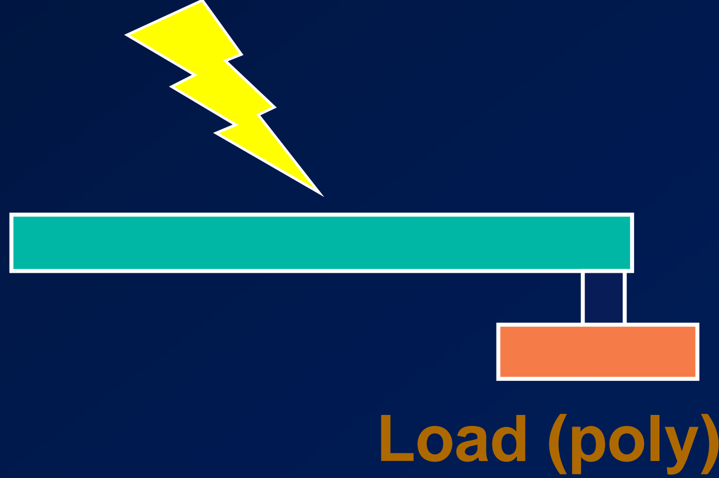
Antenna rule driven changes

- Antenna rules very difficult to check by geometrical operations alone
- Need connectivity understanding
- Necessity will depend on when high K gates are introduced
  - Situation will get better (thinner oxides) until it suddenly gets much worse (high K materials).

Antenna Rules – a review

- A problem during manufacturing
- Here is a net after M1 is built, but not yet M2
- Error!



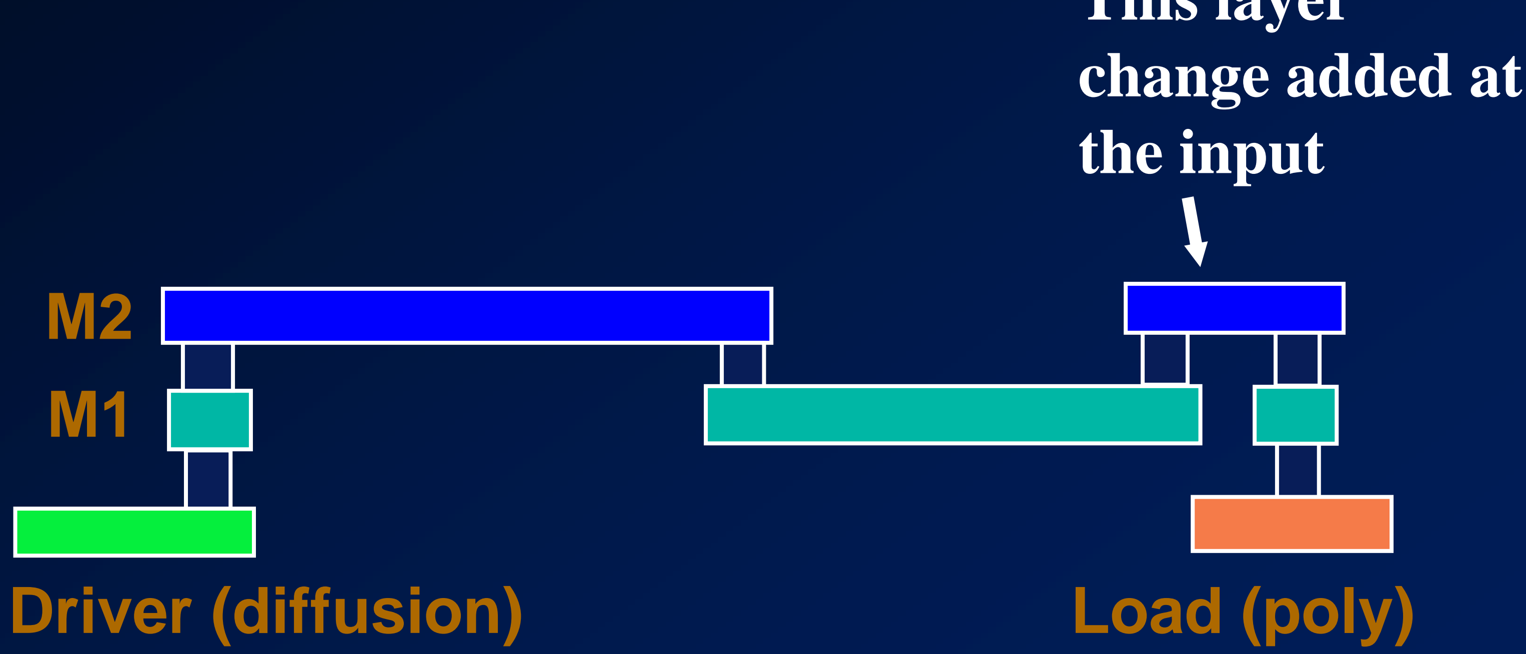


Antenna Rules – what can tools do?

- Possible solution – reverse order of layer assignments
- Changes local layer utilization

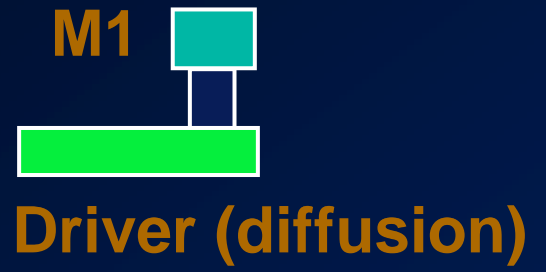
Antenna Rules – what can tools do?

- Another possible solution
- Little change of routing, but adds vias



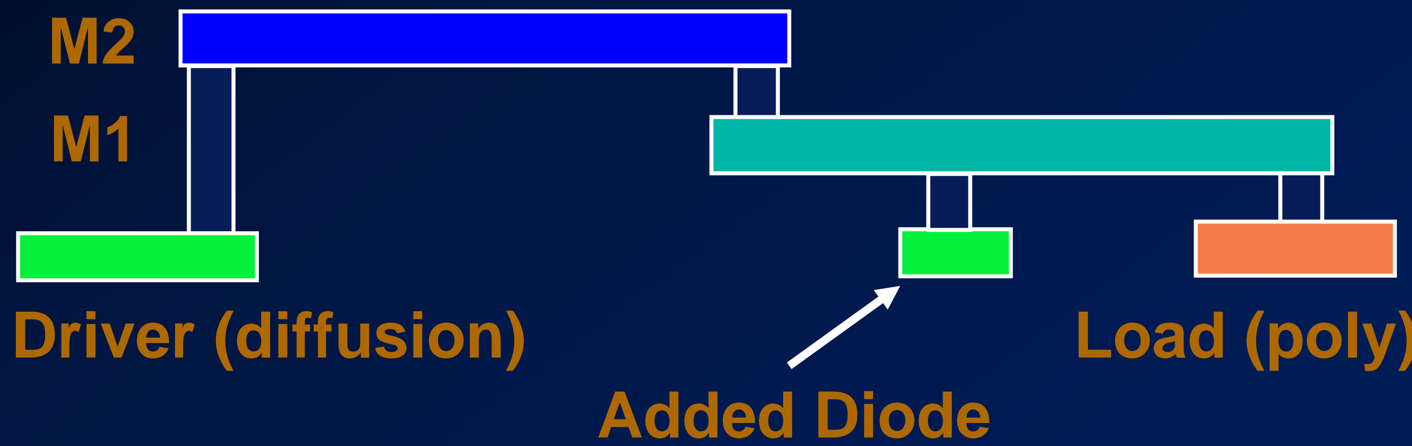
Antenna Rules

- After M1 we have floating nodes, but that's OK



Antenna Rules – what can tools do?

- A third possible solution – add diodes
- Will probably be required by high K rules
- But introduces more via blockage (and performance penalty)



Avoiding antenna problems

- Fix antenna problems with the router
  - Highest performance, but can't always be done
  - Requires the router understand the antenna rules
- Add diode cells after routing for those nets that cannot be fixed
  - Still requires some router smarts
- Add diodes to each input
  - This is a "methodology" fix
  - Requires no tool smarts
  - Lowest performance option – extra C and extra area

Antenna rules

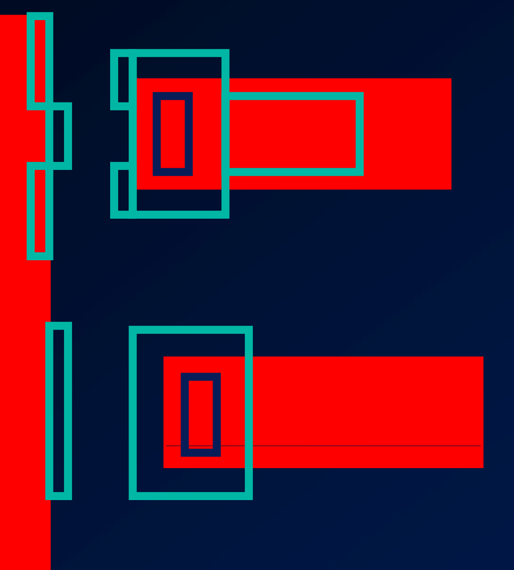
- The routing corrections cannot be added by post-processing.
  - The router must understand these rules
- Adding diodes as separate cells requires some cooperation from the router
- Adding a diode to each input avoids the problem
  - Lowest performance
  - But no tool changes required

Recommended rules and optimizations

- Foundries have additional ‘recommendations’
  - Double vias where possible
  - Add extra spacing where possible
  - Add more extension around vias where possible
  - Help from foundries is needed to make this quantitative
- Some of this can be done by post-processing
- But much better results possible if tools do it
  - Example – What percentage of vias can be doubled?
  - 30-40% as a post-process, more than 90% if router tries hard.

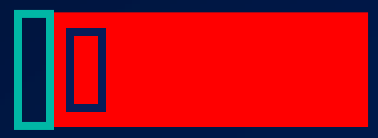
Router can help make RET easier

- Can choose correction based on need (SPIE)



Line end at minimum spacing perhaps 5-10 extra rectangles required

Slightly greater spacing – 2 rectangles required



Still greater spacing – extension only required

Simulation based OPC will correct all to the highest (most expensive) standard

Conclusions

- Post processing is the most convenient fix
  - But it works in fewer and fewer cases
- Tools (and designers) need understanding of downstream effects for best results
  - OPC
  - Metal density
  - Antenna
- A new generation of tools will handle these effects
- Methodology changes may be required as well