

# Applying equation based synthesis to produce optimal pipeline A/D converters

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Time: Refreshments and networking at 6:30 p.m., lecture at 7:00  
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Analog Design continues to be the bottleneck in the design of Mixed Signal Integrated Circuits that are used in popular consumer electronics devices, and the communications and industrial electronics devices that enhance the productivity of today's businesses. Unlike digital circuits that can be automatically synthesized from a relatively simple description, analog circuits continue to require hand design, optimization and layout.

However, there are a number of CAD startups that have been working to remove this bottleneck. One area in which this works, is the application of optimization to adjust device parameters of a given circuit to meet a new set of performance targets. The target circuit for this application is a Pipeline A/D Converter.

Optimal device sizing and operational amplifier gain setting in a pipeline A/D converter is essential to meet the requirements of lower power consumption, reduced supply voltage and large SNR for many wireless and portable devices. Equation 1 defines the SNR limit of the pipeline A/D converter, where  $n_Q$  is the quantization noise,  $n_{stage}$  is the stage noise, and  $G$  is the gain of the stage. The right hand

side of the equation is constant for a given pipeline specification in terms of dynamic range,  $V_{max}$  being the analog range and  $SNR_{max}$  expressed in dB, the effective noise voltage. The lower supply voltage requirement presents the challenge of reduced dynamic range and SNR. Additionally, thermal noise limits the maximum SNR, the magnitude of the thermal noise being a function of the size of the sampling capacitor defined by  $\sigma_{thermal}^2 = kT/C$ . Note, this does not include the noise contribution from the operational amplifier.

Eq 1

$$n_Q + \sum_{i=1}^M \frac{n_{stage_i}}{G^{2(i-1)}} < \frac{(V_{max} / 2)^2 / 2}{10^{\frac{SNR_{max}}{10}}}$$

The sequence of setting the optimal gain, noise, and power, therefore, is the following:

- Earlier stages of the pipeline have lower gain and therefore noise contribution can be smaller
- Large proportion of noise is proportional to  $KT/C$ , to reduce noise  $C$  has to increase
- The earlier stages need larger capacitors which means more power is required

The effective resolution can be improved by increasing the sizes of the sampling capacitors (being determined by the noise floor) in the first few stages of the pipeline. The requirement on resolution is less at these stages in the pipeline, the sampling capacitors in the final stages can be made smaller, also parasitic capacitances begin to dominate and settling time requirements need to be taken into consideration. However capacitor sizing from the first stage of the pipeline to the last stage is a complex optimization

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task as the later stages contribute to both power dissipation and noise depending on their capacitor sizes.

Therefore in order to meet the requirements for lower power and higher performance, the designer is faced with making **complex design trade-offs** for the optimal capacitor sizes and also the optimal gain for switched capacitor blocks and minimum power consumption of the operational amplifiers and these determine the size of each stage.

This presentation will: introduce the equation based synthesis method as applied to the optimization of pipeline A/D converters; highlight the benefits of a synthesizable approach over traditional hand design; describe the pipeline architecture including the high gain operational amplifier and conclude with silicon results from the prototype.

The architecture chosen for the synthesis is a traditional 9-stage design including a sample and hold stage in front for better dynamic linearity for high-frequency input signals. Each stage of the pipeline resolves a number of bits, and is implemented using a switched capacitor technique. In this architecture, accuracy relies only on capacitor matching, and it is possible to achieve up to 12-bit resolution without trimming. The circuit is differential, which ensures optimum immunity to interference from the power supply or the substrate. Digital error correction is added to generate the final digital code.

The synthesis method computes the sizes of the different components (transmission gates, capacitors and operational amplifier gain-bandwidth product) for each stage in the pipeline, so that the design specifications are

met in the desired process technology. Therefore the designer does not need to need find the optimal resolution of each stage or

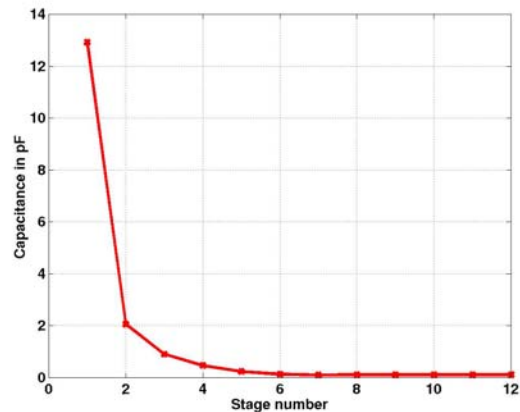


Fig 1 Capacitor scaling through pipeline

the optimal capacitor sizes through the pipeline. Figure 1 shows that using equation based synthesis the capacitors sizes are optimally sized through the pipeline.

The method is based on formulating the A/D design constraints in special convex form in terms of the component sizes of the A/D and intermediate design variables.

The resulting GDSII layout includes a sample and hold amplifier, voltage reference and 2-phase clock generator from a single ended or differential single-phase clock input. The topology is compatible with standard CMOS processes. By using this topology and the synthesis approach a very wide specification range can be covered suitable for portable communication devices and wireless LAN.

To verify the effectiveness of the technique, a prototype 10bit 100 MS/s pipeline A/D converter was designed

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and fabricated in a 0.13  $\mu\text{m}$  CMOS technology.

About the author:

Navraj Nandra joined Barcelona Design in June 2001 as Director of Applications from Austria Mikro Systeme International, where he was U.S. Design Center Manager supporting ASIC and COT designs in high voltage CMOS, SiGe and BiCMOS technologies.

Mr. Nandra has worked in the semiconductor industry since the mid 80's as an analog IC designer for Philips Semiconductors, EM-Marin (Neuchatel, Switzerland) and Thorn EMI Central Research Labs (UK). He has authored papers in A/D converter design and RFID design. In 1996 he was awarded the best poster for "A Contact-less Read/Write Transponder using Low Power EEPROM technology" at ESSCIRC in Neuchatel.

Mr. Nandra holds a Master of Science degree in microelectronic systems design from Brunel University and a postgraduate diploma in process technology from Middlesex Polytechnic, both in the UK.