

Noise Constraint Driven Placement for Mixed Signal Designs

**William Kao and Wenkung Chu
October 20, 2003
CAS IEEE SCV Meeting**

OUTLINE

- **Introduction**
- **Substrate Noise: Some Background**
- **Substrate Noise Network Model**
- **Virtuoso Custom Placer (VCP)**
- **Substrate Noise Constrained Placement**
- **Integrated SEISMIC – VCP Flow**
- **Study Example**
- **Conclusion and Future Work**

Introduction

- Increasing larger number of SOCs where digital, analog and RF functions are all integrated on a single chip substrate.
- In the deep submicron regime SIGNAL INTEGRITY issues are increasingly becoming more critical.
- One of the significant 'signal integrity' problems in mixed signal designs today is the handling of noise coupled through the common substrate and power supplies which is caused by signal switching inside the digital section and affecting sensitive analog circuitry.
- In this paper, we propose a solution to constrain noise coupling through the substrate based on an analysis-optimization loop between:
 - the substrate analysis capabilities of SeismIC [5] and
 - the placement capabilities of Virtuoso Custom Placer [6].

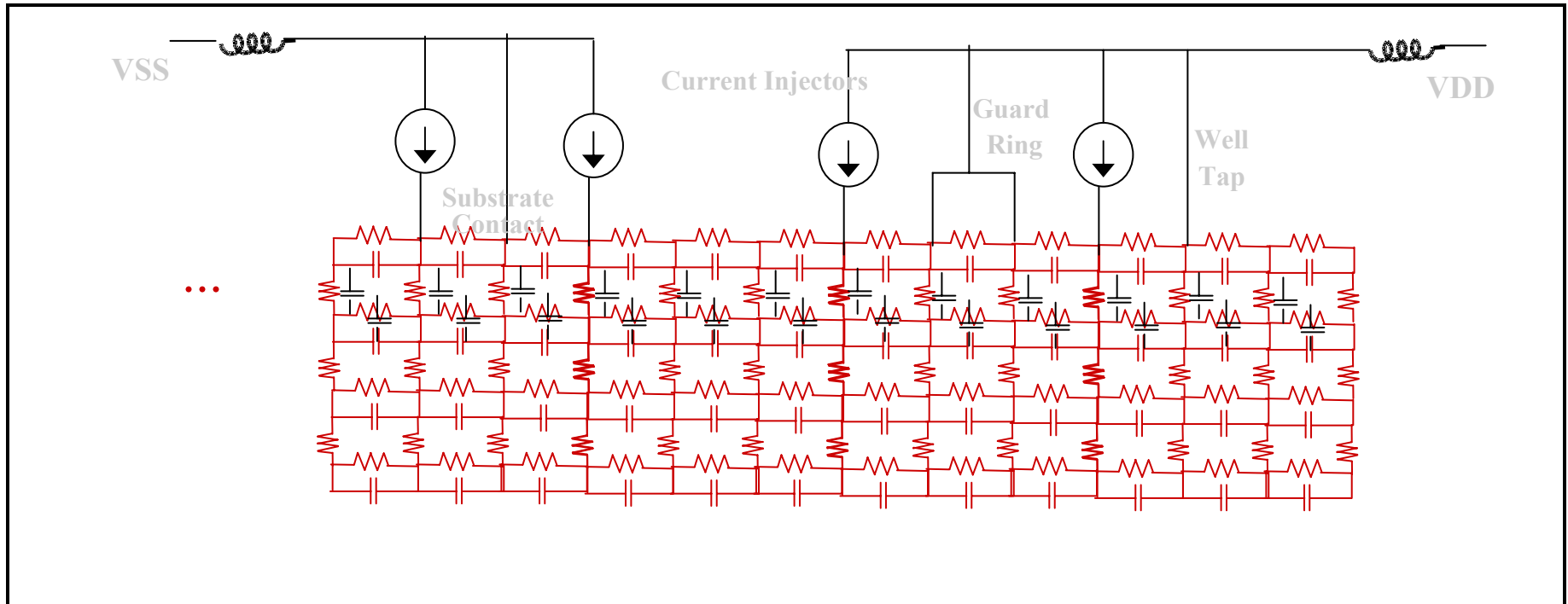
What is Substrate Noise?

- **Substrate noise modulates device threshold voltage, shifts operating point.**
- **Noise coupling of digital switching currents to sensitive analog devices.**
- **Substrate noise manifests itself in signal path and affects performance.**

Why are Substrate Noise problems getting worse?

- **SOC requirements of getting digital, analog and RF on the same chip.**
- **Design scaling: noisy and quiet nets getting packed closer together.**
- **Lower supply voltages.**
- **Lower noise margins on analog components.**
- **Faster clock frequencies and slew rates.**

Substrate RC Mesh Network



- Model substrate as a distributed medium.
- Add switching current macromodels at noise source locations.
- Perform analytical simulation including all injected currents.
- Voltage response at bulk node of interest is desired:

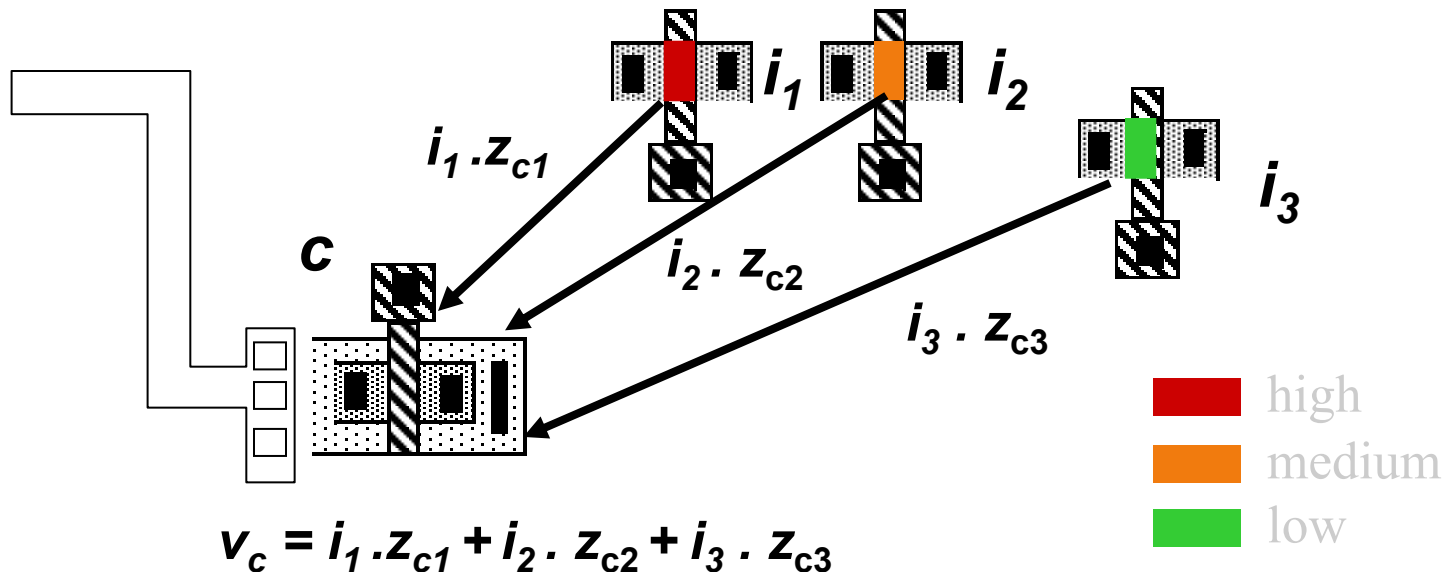
$$V_b(s) = \sum_k z_k(s) i_k(s)$$

Identifying Noise Contributors

$$v_c(s) = z_{c1}(s) \cdot i_1(s) + z_{c2}(s) \cdot i_2(s) + z_{c3}(s) \cdot i_3(s) + \dots$$

$$\Rightarrow v_c(t) = z_{c1}(t) * i_1(t) + z_{c2}(t) * i_2(t) + z_{c3}(t) * i_3(t) + \dots$$

Given critical device, c and noise source, j ,
noise contribution at c from source j , $v_{cj} = z_{cj} \cdot i_j$



Substrate Noise Network Model

- Current sources (a in Fig. 1) are used to model charge injected into substrate via device drain/source diffusions.
- The contacts and guard rings are modeled by r_c , r_g and packaging inductors (b in Fig. 1). So the packaging induced noise at the substrate ties can be calculated by the simulation engine.
- Ideal voltmeters V_n (c in Fig. 1) are used to detect voltages at relevant substrate nodes and are used to calculate the substrate noise related penalty terms in the form $\min(0, V_n - V_{\text{target}})$.
- The substrate itself can generally be represented as a network grid (d in Fig.1) composed of impedances Z_s .

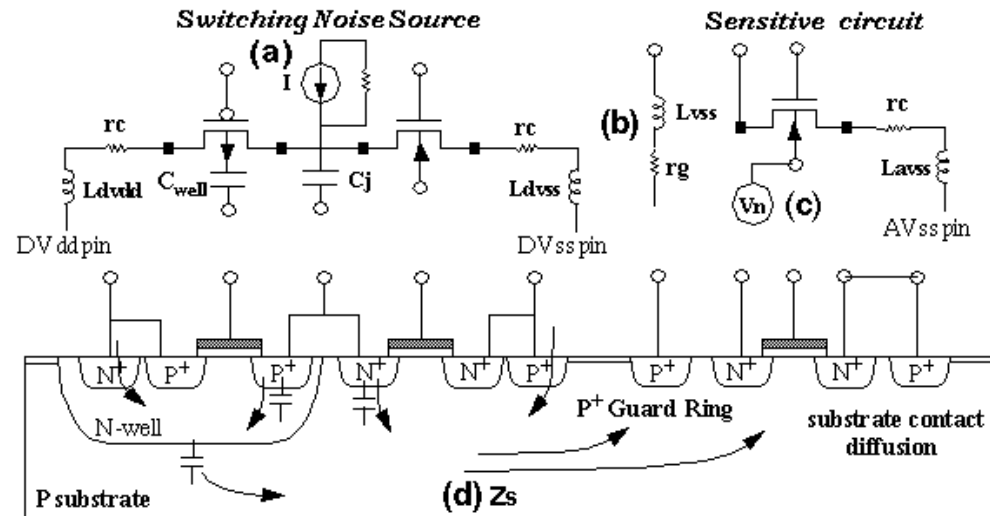


Figure 1

Virtuoso Custom Placer

- Automatic placement of custom analog, mixed signal and high performance digital circuits is a challenging task.
- It is also impossible to rely solely on manual custom layout design to remain performance competitive.
- The Virtuoso Custom Placer (VCP) was developed by combining interactive and automated placement to enhance productivity without sacrificing custom performance.
- VCP's placement process consists of 4 basic steps:
 1. **Data Preparation** where the netlist and constraints are read in from the database and constraint manager.
 2. **Global Placement.** It starts by using iterative quadratic/mincut methods to recursively bipartition components into different regions. The goal is to find an overall violation-free placement and spread all components into the defined placeable area.
 3. **Detail Placement.** Using annealing based methods it refines the initial placement to obtain a better placement based on the costs defined by the user.
 4. **Congestion Estimation and Spacing Adjustment:** To make the placement routable and reduce the overall wire length, there is a need to identify where the congested spots are and make room for routing.

Substrate Noise Constrained Placement

- Minimize Total Area and Wirelength constrained by

$$[F_{\min}] < [F(P)] < [F_{\max}] \quad (3)$$

where P is the placement instance and $F(P)$ represents the noise constraint which is affected by the placement instance P .

- The constrained multi-objective optimization problem above is converted to the unconstrained single objective problem:

Mimimize:

w_1 Area + w_2 Wire Length + w_3 Constraint Violations,

where w_1 , w_2 and w_3 are weighting functions.

Integrated SEISMIC –VCP Flow

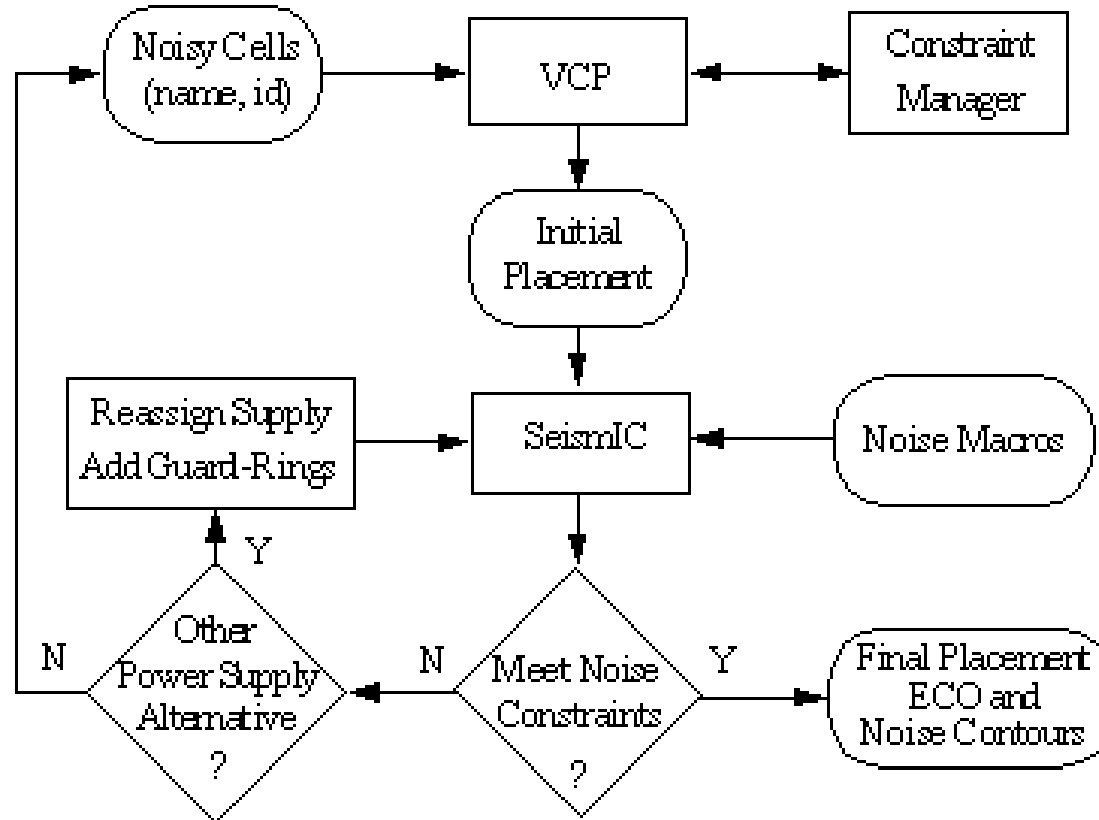
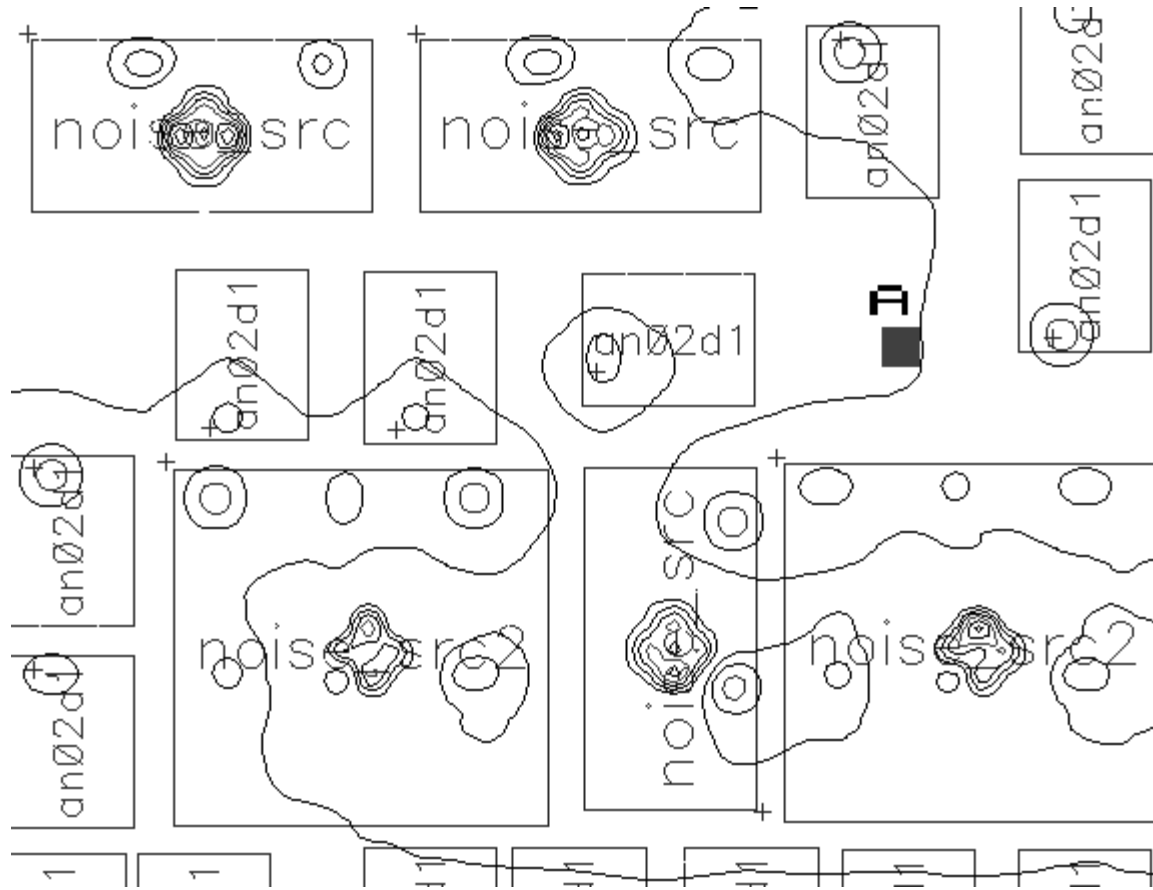


Figure 3

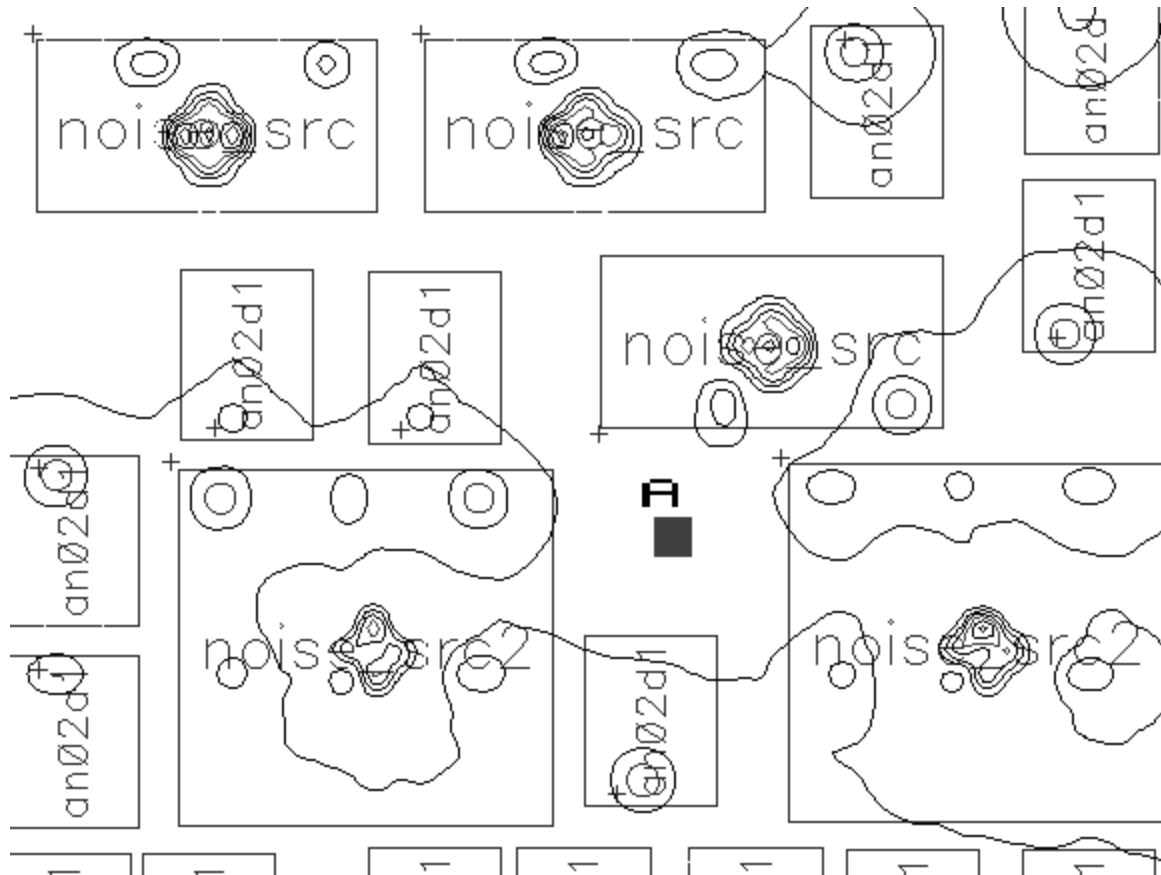
Study Example:

Fig 4. Initial placement (V_n at Cell A = 22mV)



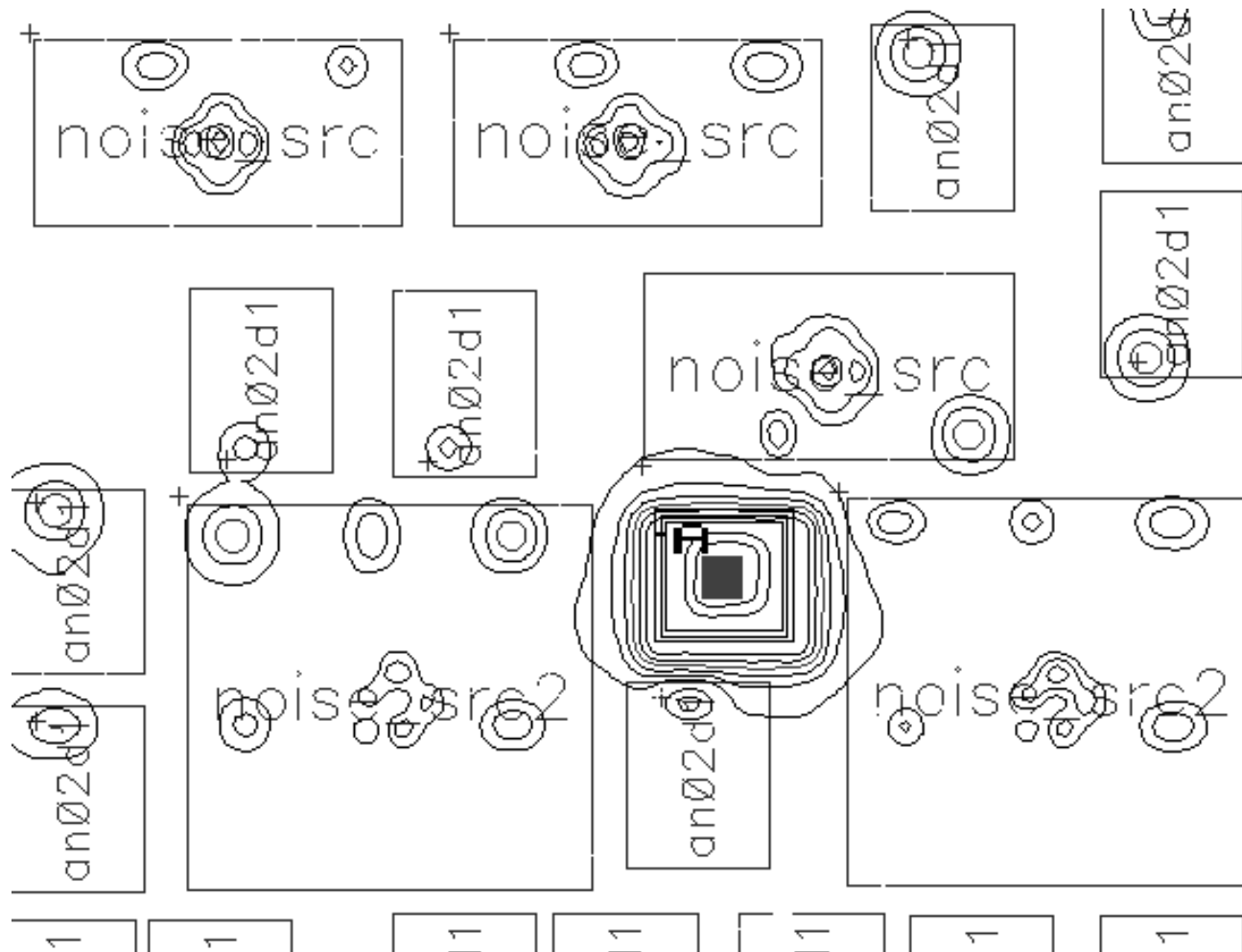
Study Example:

Fig 5. Placement after few Iterations ($V_n = 19\text{mV}$)



Study Example:

Fig 6. Final solution with Guard-ring added ($V_n = 6.2\text{mV}$).



Conclusion and Future Work

- **We have presented a ‘constraint driven placement flow’ which addresses the problem of substrate coupled switching noise in Mixed Signal designs.**
- **It is accomplished by utilizing:**
 - **the substrate noise modelling and analysis capabilities in SeismlC and**
 - **coupling it to the Virtuoso Custom Placer in an analysis and optimization loop.**
- **Further work would be to extend this flow to include other signal integrity issues such as crosstalk, EM, IR and thermal effects.**