EMI Issues for Power Electronic Systems

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Outline

- EMI overview
  - Qualitative Discussion: Maxwell's Equations
- Path of Lowest Impedance
  - Video Demonstration
- Decoupling Capacitors
  - Proper Layout, Minimize Circuit Problems
- Strategy for DC Bus Decoupling
  - Beware of Resonances
- Filtering Performance & Degradation
  - What is Mutual Inductance
  - Self- and Mutual-Parasitics

Definition

Electromagnetic Interference (EMI) is an unintended transfer of electrical energy from one circuit or system to another. This energy has the ability to interfere, corrupt, or damage the operation of the receiving circuit.

EMI is broadly classified into two categories: Emissions is the electromagnetic energy that a system (unintentionally) emits.

Susceptibility specifies the ability of a system to continue to operate properly in the presence of an EMI disturbance.

Important Electromagnetic Laws

Gauss' Law (1)

$$\nabla \bullet D = \rho$$

Electric flux begins and terminates (diverges) on electric charges.

Gauss' Law (2)

$$\nabla \bullet B = 0$$

Magnetic flux always closes on itself (no divergence).

Faraday's Law

$$\nabla x E = -\frac{\partial B}{\partial t}$$

Time changing magnetic flux creates an electric field.

Ampere's Law

$$\nabla x H = J + \frac{\partial D}{\partial t}$$

Conduction and displacement currents (time changing electric flux) create a magnetic field.

Charge Continuity

$$\nabla \bullet J = -\frac{\partial \rho}{\partial t}$$

Charge is conserved.

Circuit Theory Equivalents

$$e = M \frac{di}{dt}$$ Time changing current induces a voltage.

$$i = C \frac{dv}{dt}$$ Time changing voltage induces a current.

Current ALWAYS closes on itself.

Current takes the path of lowest IMPEDANCE.

- Not the same as lowest resistance. For AC circuits lowest impedance usually means lowest inductance.

95% of EMI problems are simple R-L-C equivalent circuits.

This is (almost) everything you need to know about EMI.

Then why is EMI so difficult?

- Important M {L} and C values are parasitic
  - Never on the schematic, but they affect the system
  - Parasitic L, M, C values can be counterintuitive
- We usually ignore where currents flow
  - We use symbols like  for “current return”
- Often there are multiple EMI problems
  - Difficult to decouple multiple problems
  - EMI symptoms can be misleading
- “Noise” implies we cannot control it
  - EMI often treated as complex, unknowable, or magic
- Most engineers don’t have EMI training
  - We don’t understand what EMI symptoms are telling us

Comments on EMI Troubleshooting

The theory of EMI & EMC is simple. In practical applications the problems become difficult. Most systems are asymmetrical, have complex geometrical shapes making closed-form solutions difficult or impossible. Multiple EMI events often occur simultaneously.

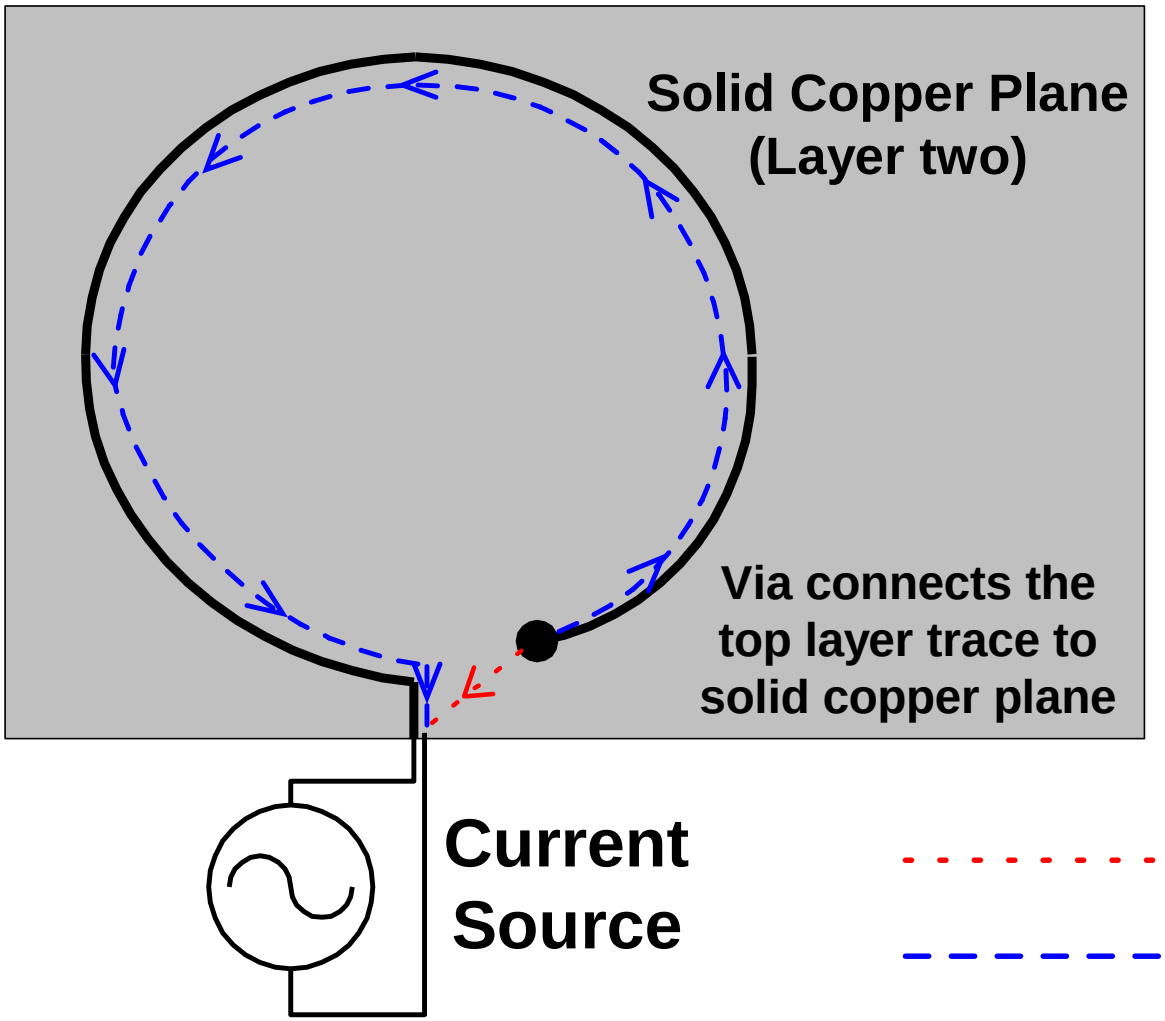
It is important to understand the physical mechanisms of energy transfer in an electronic system. Having this insight allows a practical understanding of EMI problems and solutions.

Path of Lowest Impedance

EMI is All About Current Paths

- **The golden rule: Return currents back to their source in a defined path and as compactly as possible.**
- **Most EMI problems arise because of an unknown or an uncontrolled current return path.**
- **A very important concept to understand for making a robust EMI board is "where are the currents flowing, and why are they flowing there." This is true for both EMI emissions and EMI susceptibility.**
- **High frequency currents will automatically flow in the best available path (minimum energy principle). It is your job to allow good sending and return paths to exist. Usually the return path is the problem.**

Example: Current Flow on a Two Sided Board



Current takes path of lowest impedance.

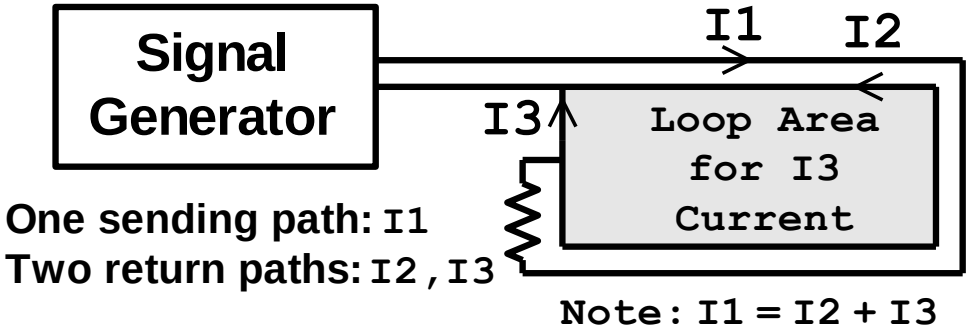
Lowest impedance path means lowest inductance (smallest current loop area) for >10 kHz currents.

Lowest impedance path is:

- - - - - - - - **Lowest R: Freq < 1 kHz**

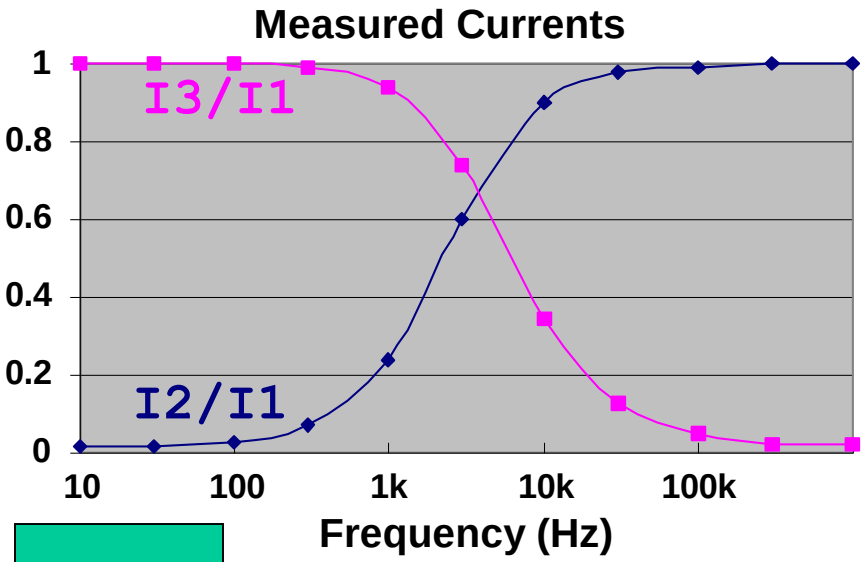
– – – – – – **Lowest L: Freq > 10 kHz**

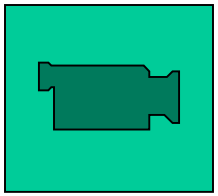
Demonstration # 1: Path of Lowest Impedance, and Frequency Decomposition

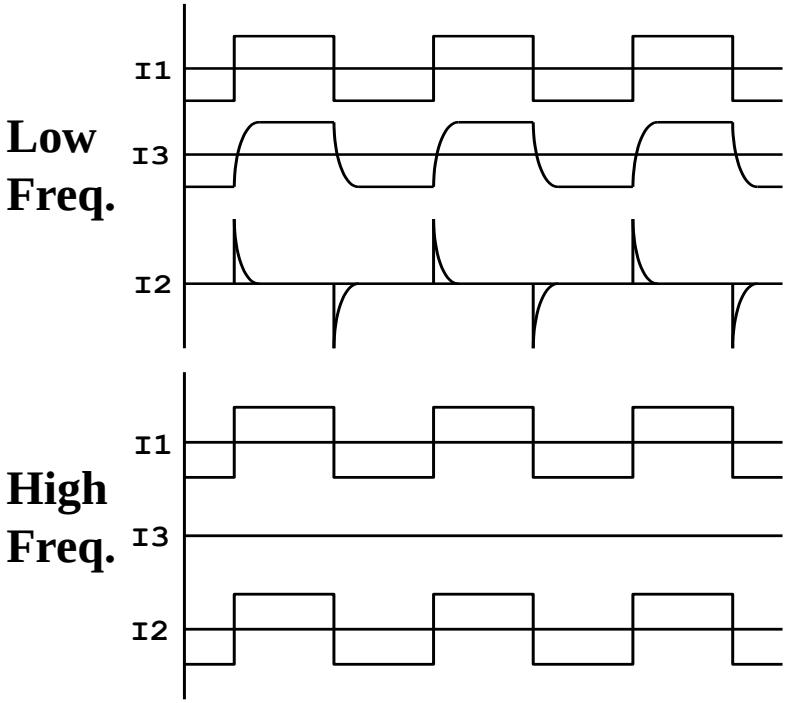


I2 – Lowest inductance path (High freq. path, > 10 kHz)

I3 – Lowest resistance path (Low freq. path, < 1 kHz)

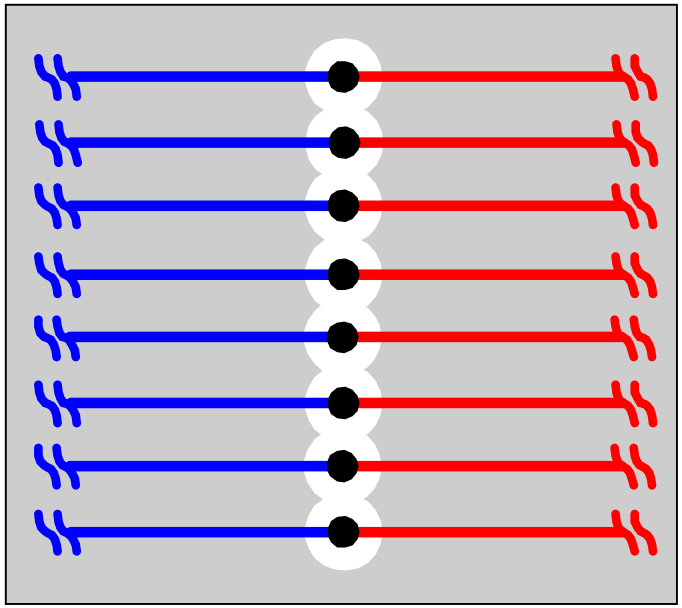




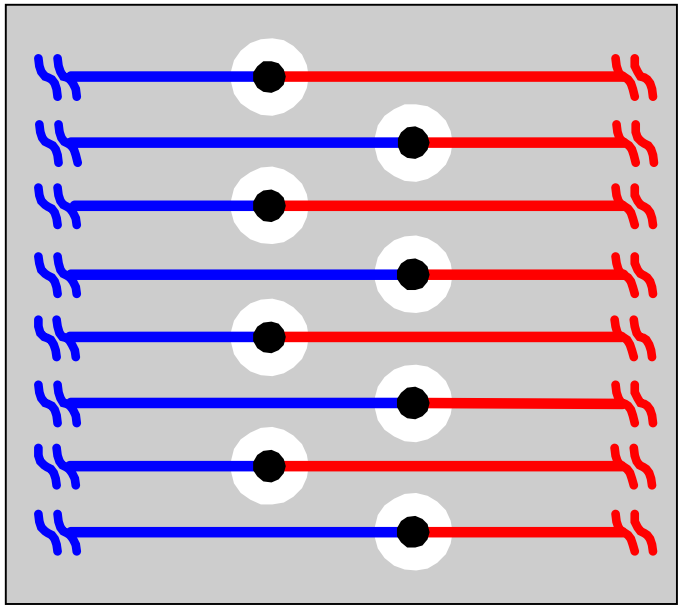


Stagger Vias to Avoid Split in Return Plane

When several traces on a circuit board move from one layer on the board to a different layer, be careful not to make a split in the return plane due to the via voids.



BAD – Split in plane



BETTER – No split in plane

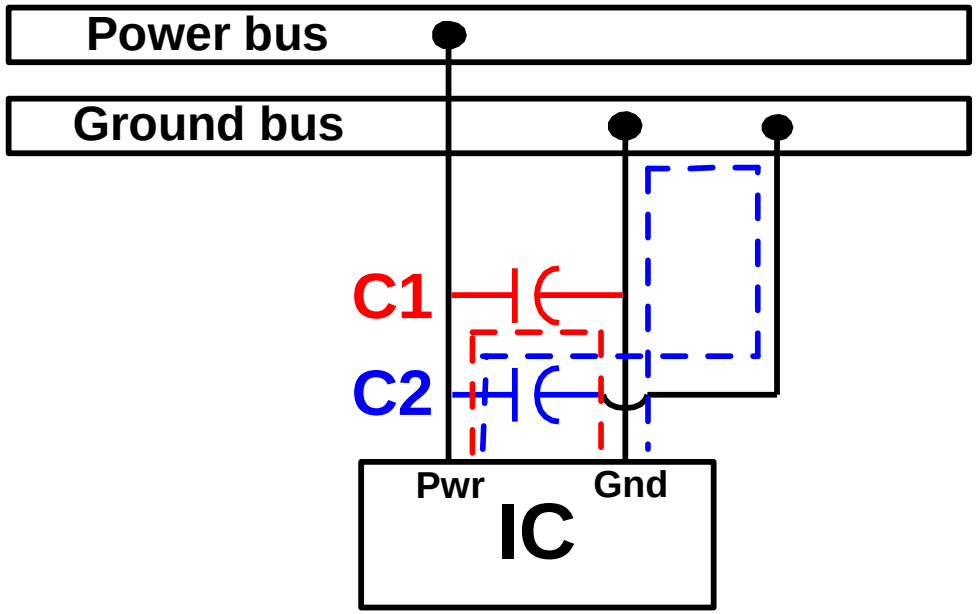
Make sure return currents can flow close to the circuit traces.

Power Bus Decoupling

Power Bus Decoupling

Decoupling capacitors should be electrically close to the IC it is decoupling. That is, the loop area (inductance) should be minimized. Trace out the current loop from the cap-to-IC.

Question: Which capacitor is electrically closer to the IC?

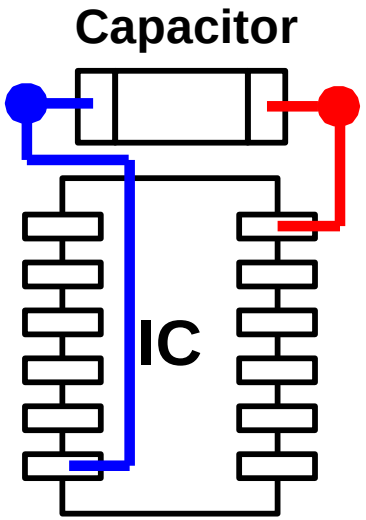


***Answer*: C1 is electrically closer because it has a smaller loop area to the IC it is decoupling.**

Just because a part is physically close does NOT mean it is electrically close.

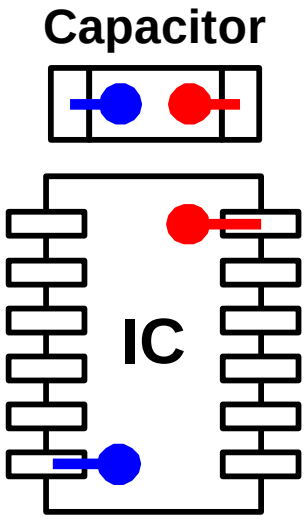
Power Bus Decoupling (2)

Poor Power Decoupling



- > 10 nH loop inductance (IC to Power & Ground)
- Reduces routing paths
- Emissions & susceptibility problems (due to loop)

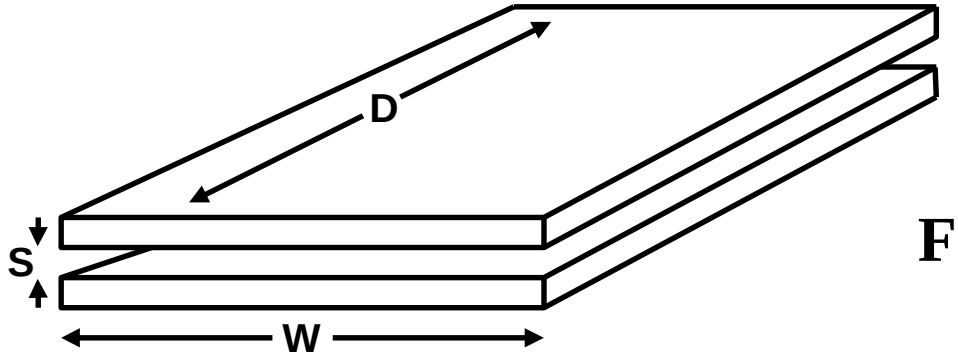
Good Power Decoupling



- Very low inductance (< 5 nH)
- Loop minimized
- Keeps decoupling currents on planes
- More routing flexibility

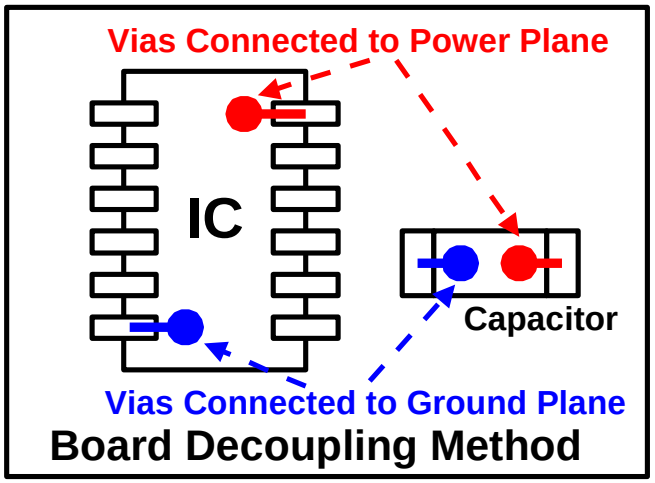
Power Bus Decoupling (3)

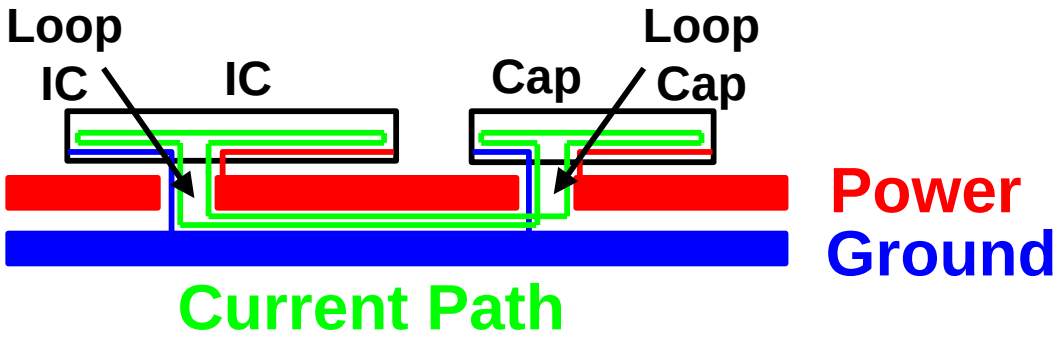
The inductance of a plane above a plane is very low (assuming no plane spits), so the decoupling impedance (inductance) to a power & ground plane structure is determined by the connections to the planes.



$$L \approx \frac{\mu S}{W} D \quad \text{henrys}$$

For W = 20 cm; D = 10 cm
S = .1 mm (4 mils)
L = .06 nH !!!!

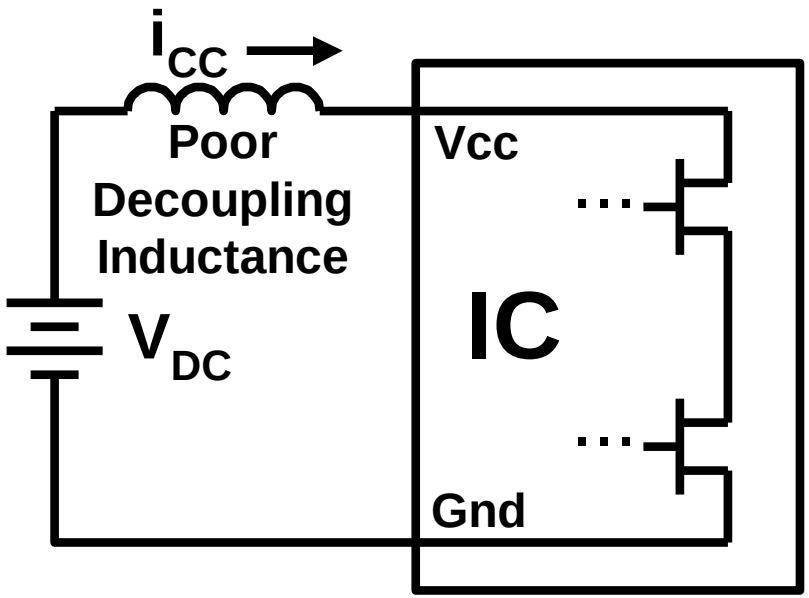


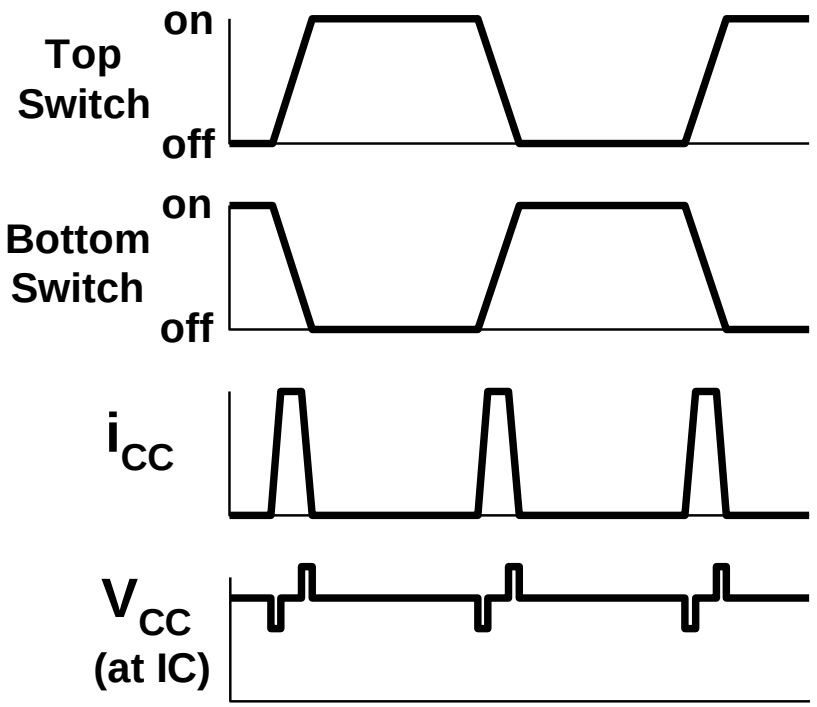


Loop area between planes is very small

Digital IC Shoot-Thru

Digital IC switching transitions have a small period of time (< 2 nS) when the upper and lower output switches are both conducting. There is a very large current drawn from the DC link during this event. The exact value is manufacturing dependent, and varies from vendor to vendor. This can cause EMI problems within the IC due to large di/dt's, or DC voltage variation at the IC due to poor decoupling.





DC Bus & Decoupling Capacitance Procedure

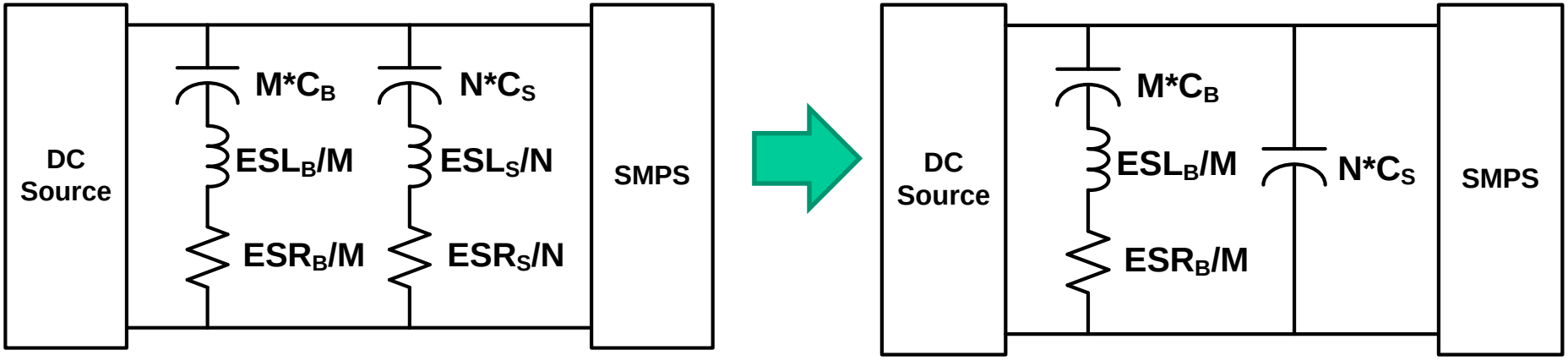
- **Choose a small number of large microfarad energy storage capacitors**
  - **C_B, ESL_B, ESR_B**
- **Choose a large number of small package size (e.g. 0805), same microfarad value, ceramic capacitors**
  - **C_S, ESL_S, ESR_S**
    - **ESL_S mostly depends upon connection method to planes**
  - **Use largest practical capacitor value**
    - **Keeps "characteristic impedance" low (see following slides)**
    - **Ignore .1μF || .01μF || .001μF approach**
- **Connect the small capacitors symmetrically (i.e. all the same) low inductance via connection to power and return (ground) planes**
  - **The makes N small capacitors act like one effective large capacitor**
    - **N Caps : $N*C_S$, ESL_S/N, ESR_S/N**
    - **This eliminates potential resonances between small capacitors**
- **Still need to understand resonance between large & small capacitors**

DC Bus Decoupling

Assume M bulk capacitors (C_B), and N decoupling capacitors (C_S)

C_B >> C_S

Place smaller decoupling capacitors in symmetrically



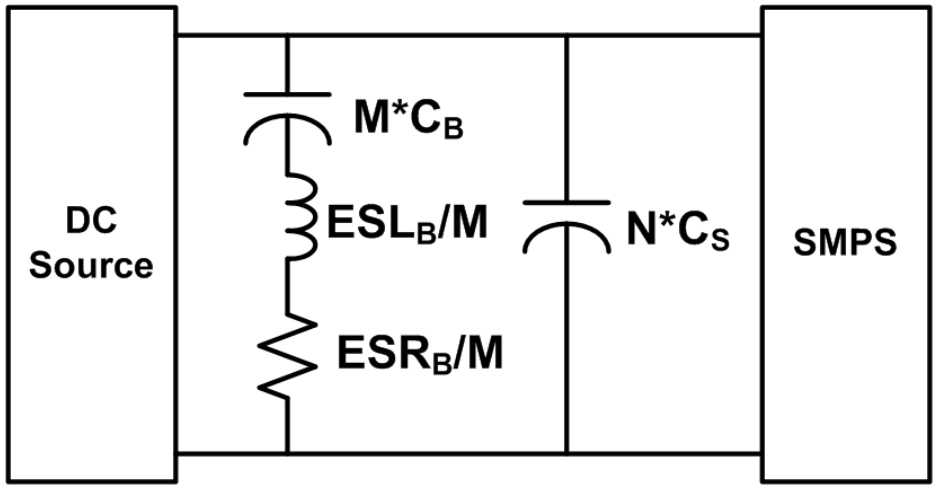
In most applications: N >> M (i.e. Many more decoupling caps than bulk caps)

$M*C_B$ >> $N*C_S$ (More μF in bulk caps)

ESL_B/M >> ESL_S/N (ESL set by bulk caps)

ESR_B/N >> ESL_S/N (ESR set by bulk caps)

Decoupling Forms a Resonant Circuit



$$f_0 = \frac{1}{2\pi\sqrt{(ESL_B / M) * (N * C_S)}}$$

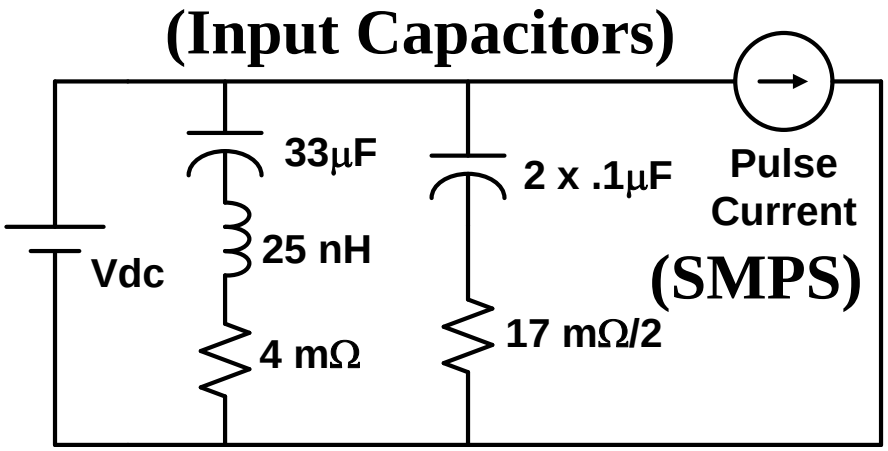
$$Z_0 = \sqrt{\frac{ESL_B / M}{N * C_S}}$$

$$Q = \frac{Z_0}{ESR_B / M}$$

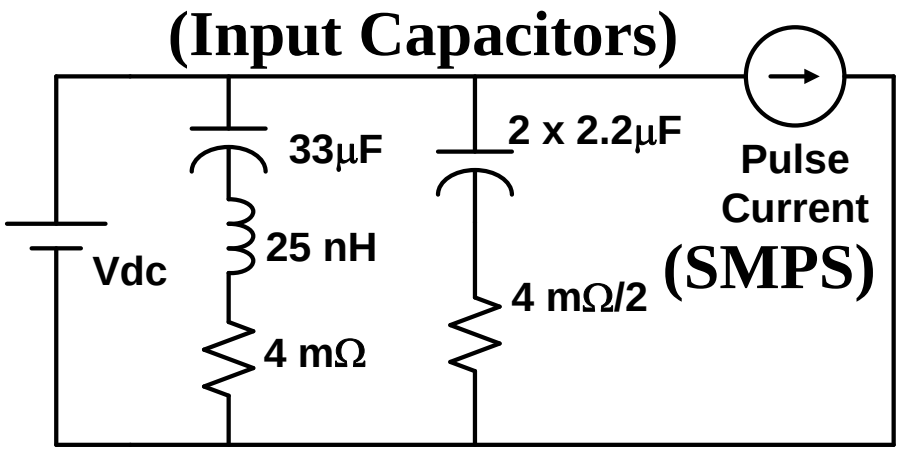
In most applications: $M*C_B >> N*C_S$

$M*C_B$ in series with $N*C_S \approx N*C_S$

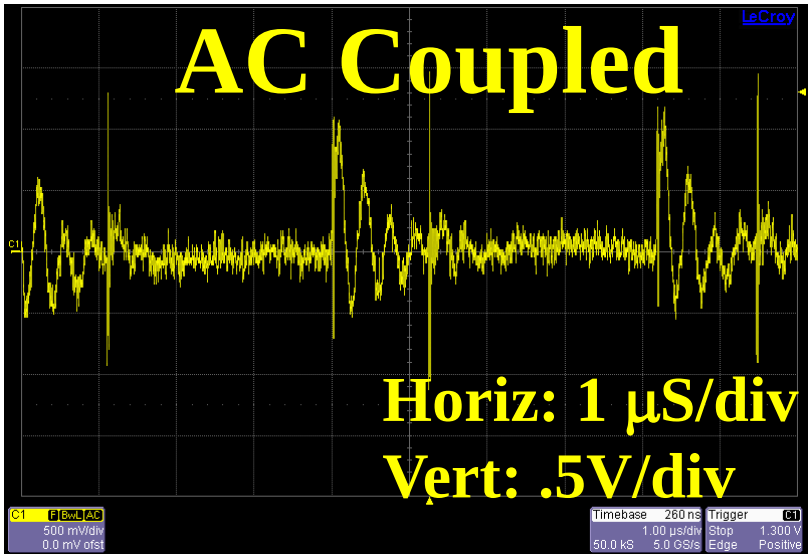
Measured SMPS DC Link

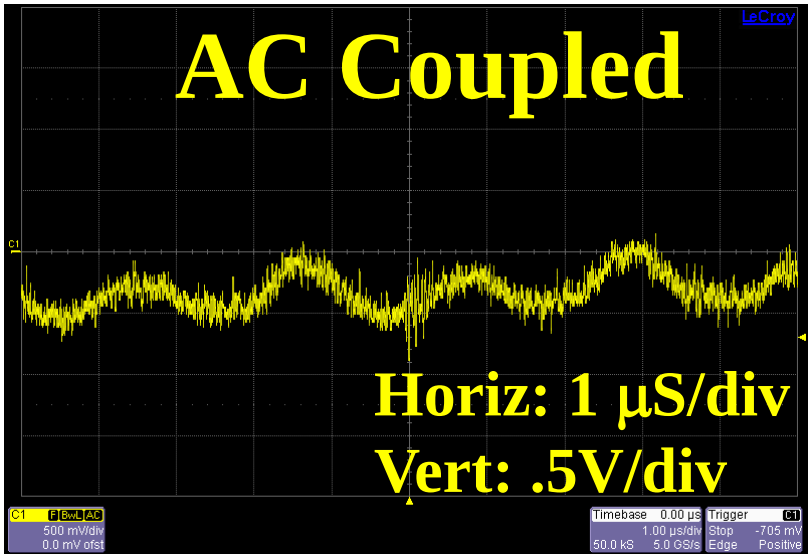


$f_0 = 2.6\,MHz,\ Z_0 = .35\Omega,\ Q \approx 30$



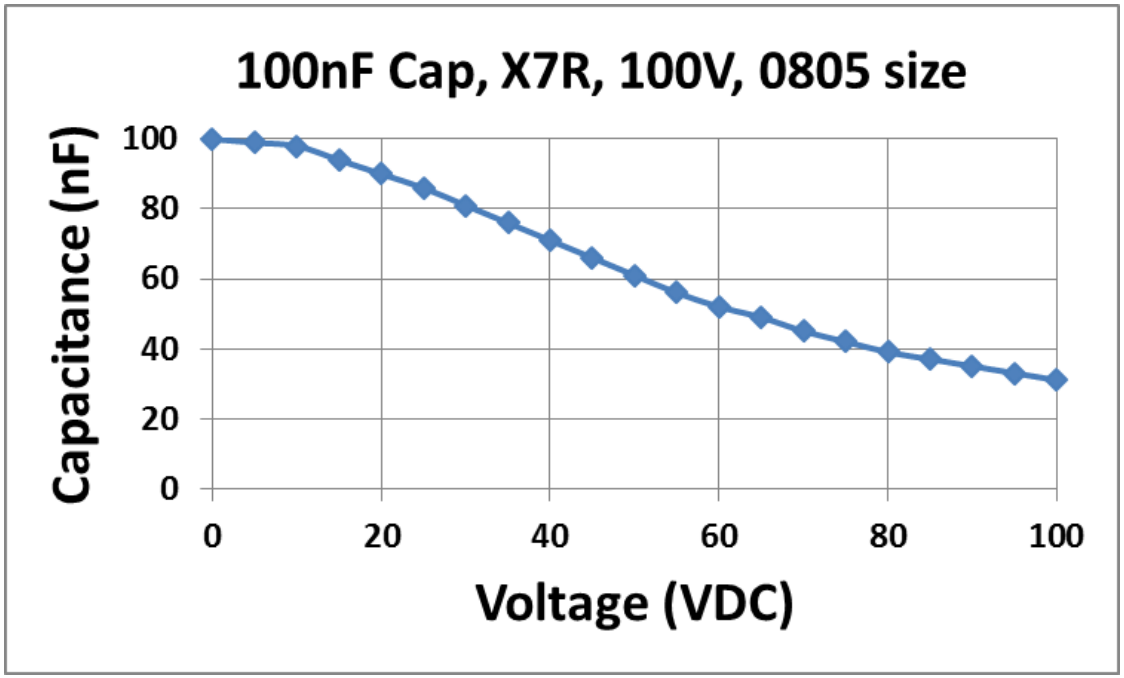
$f_0 = 480\,kHz,\ Z_0 = .075\Omega,\ Q \approx 12$





30 dB Reduction in DM EMI at 2.6 MHz !!!

Voltage Dependency of Ceramic Capacitors

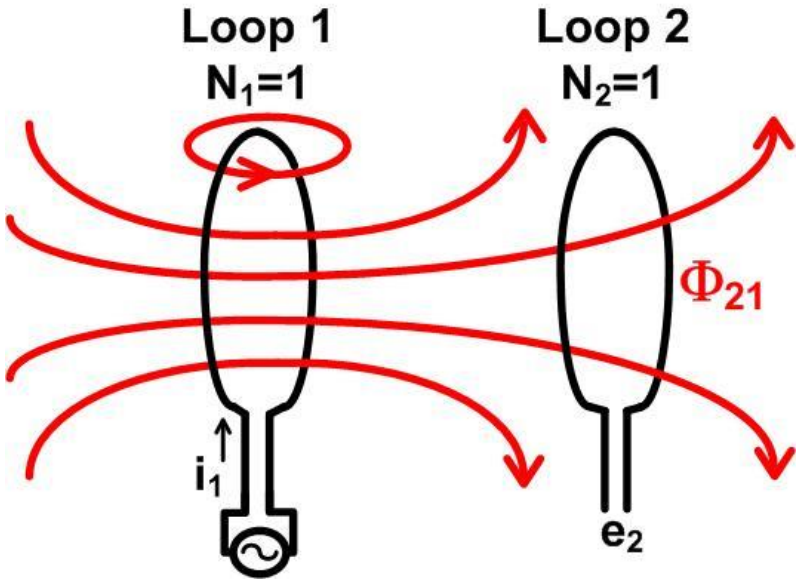


When the capacitor is operated in a DC voltage biased operation, as is the case for most decoupling capacitors, the voltage derated capacitance value should be used.

e.g. at 50VDC this "100nF" capacitor is actually 60nF.
at 100VDC this "100nF" capacitor is actually 32nF.

EMI Filter Degradation Due To Filter Parasitics (Self & Mutual)

Mutual Inductance

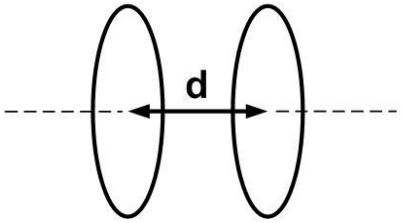


$$M_{21} = M_{12} = M = (N_2 \Phi_{21}) / i_1$$

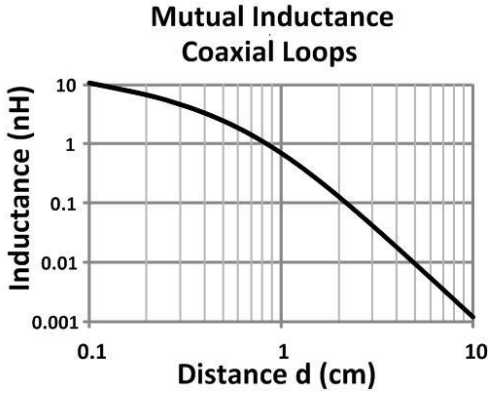
$$e_2 = -N_2 \, d\Phi_{21}/dt = -M \, di_1/dt$$

- Mutual inductance degrades filter performance
- Current in loop 1 controls voltage in loop 2
  - Electrical crosstalk
  - Degrades filter performance
- Mutual inductance can be positive or negative
  - Depends on geometry

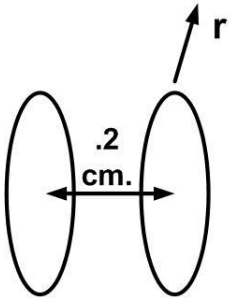
Mutual Inductance of Two Loops



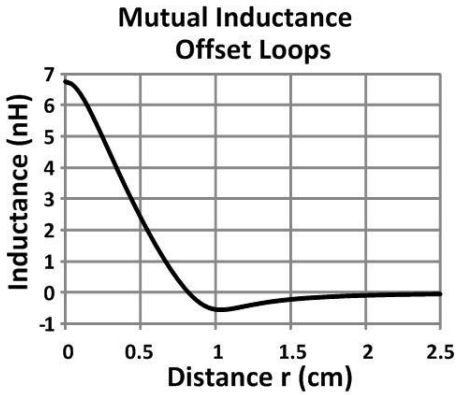
1 cm. diameter coaxial loops



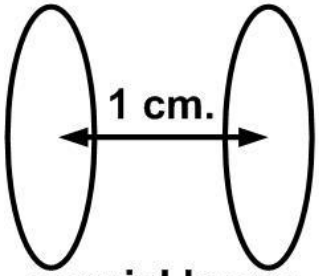
- Decreases rapidly with distance
- M ~ 1/dist^3
  - After separation > diameter
- Not effective if loops are close



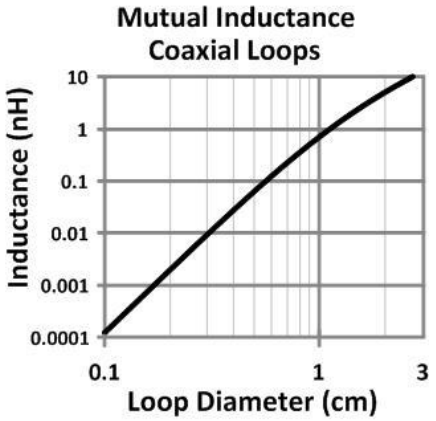
1 cm. diameter parallel loops moved radially



- M falls quickly with offset
- M = 0 for offset ~ .8 diameter
- M changes sign (around M=0)

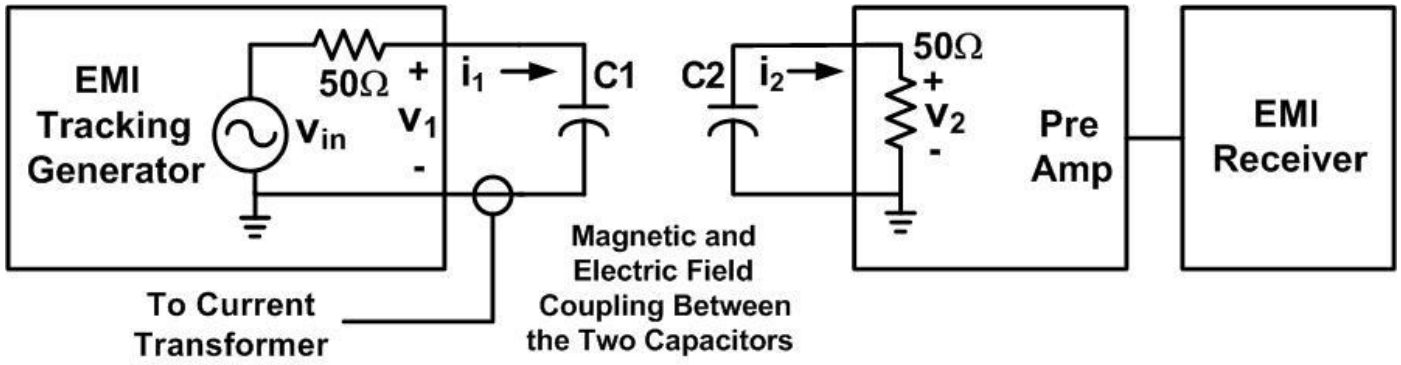


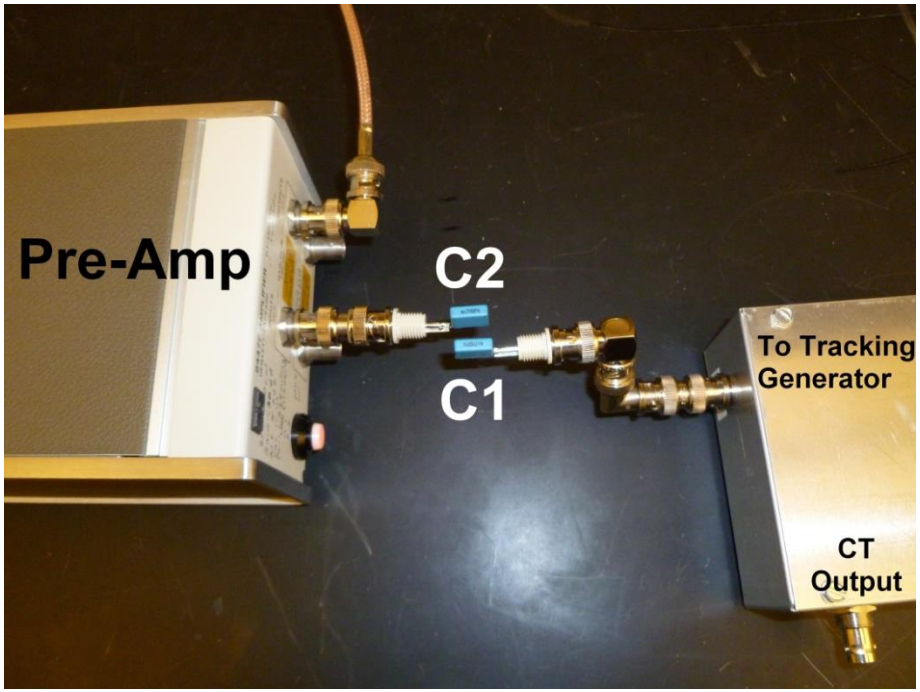
coaxial loops changing diameter



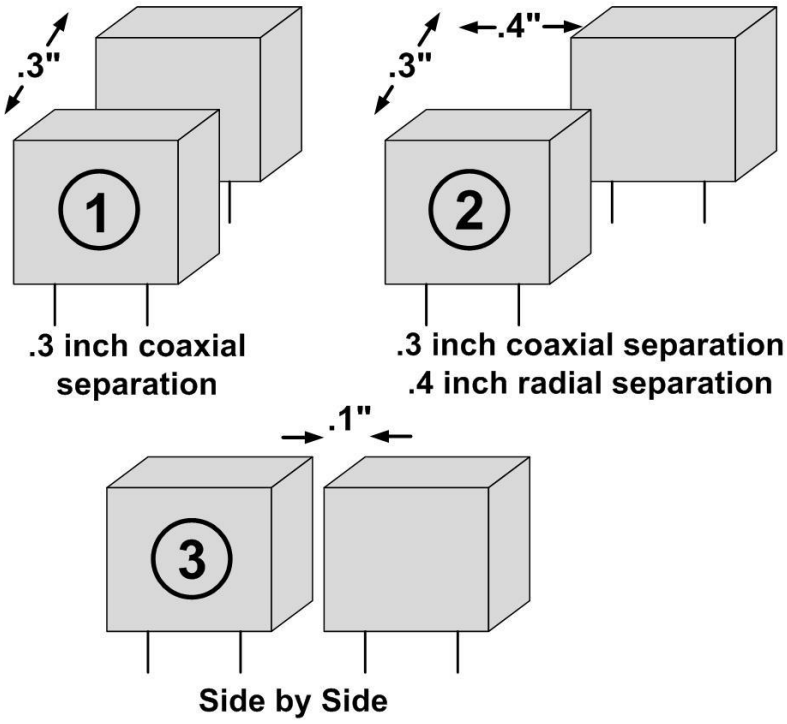
- Reducing loop diameter is very effective to minimize M

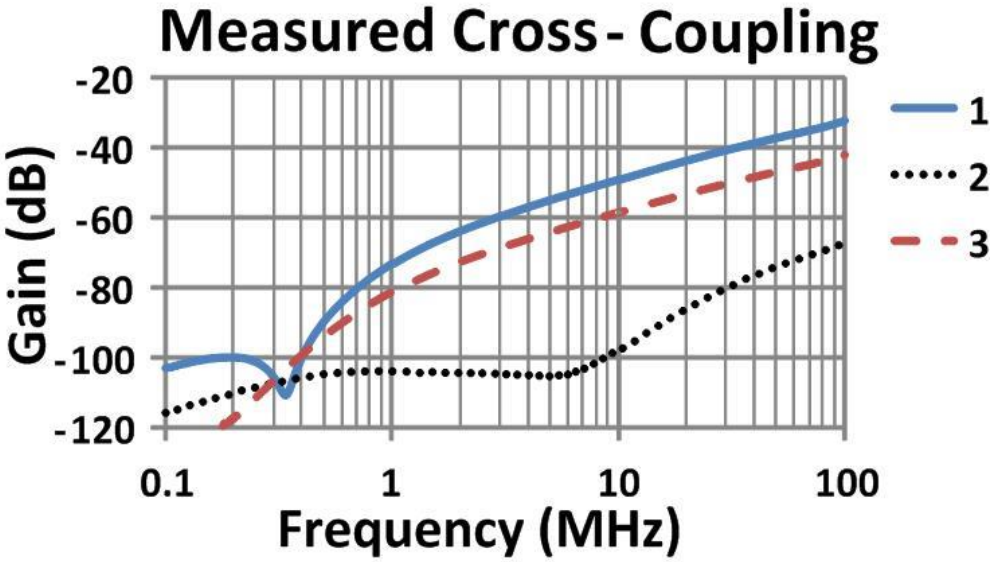
Capacitor Mutual Coupling Setup

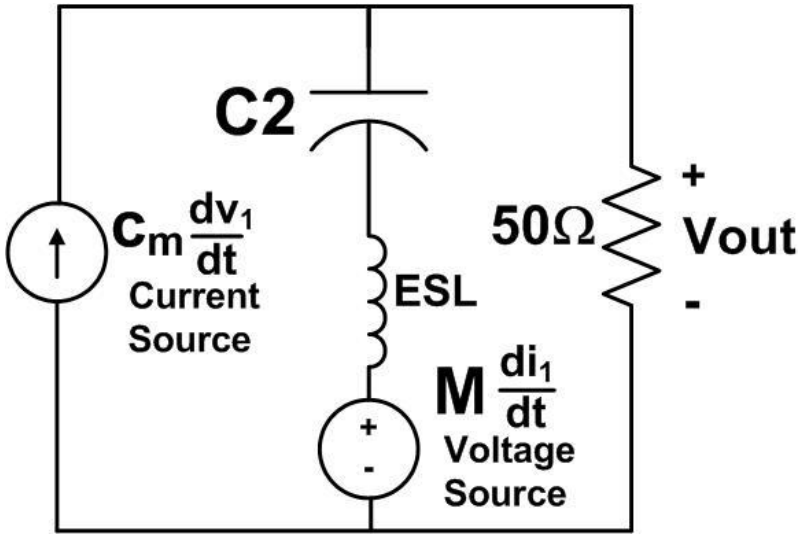




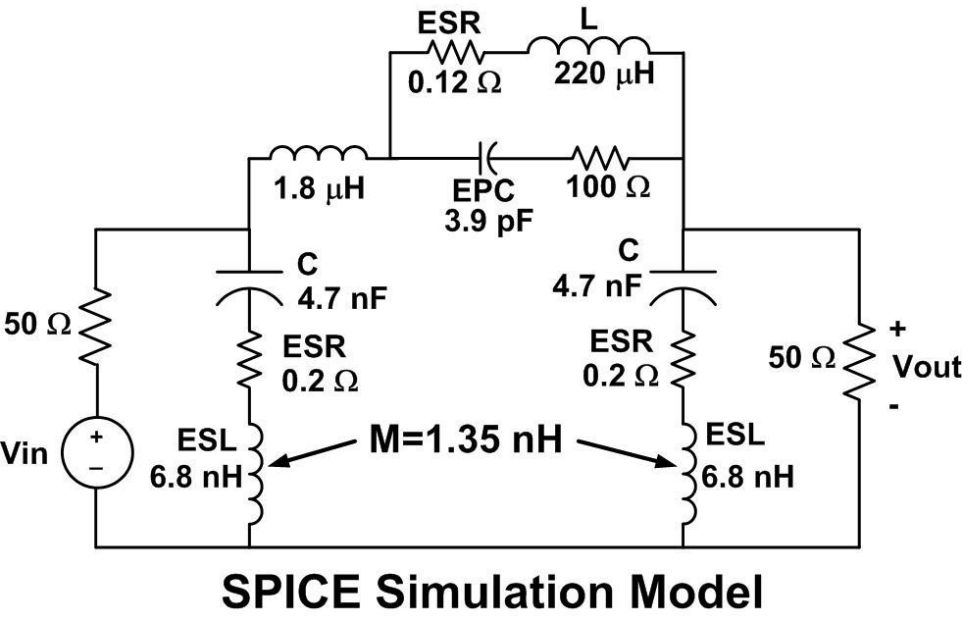
Measured Capacitor Cross-Coupling



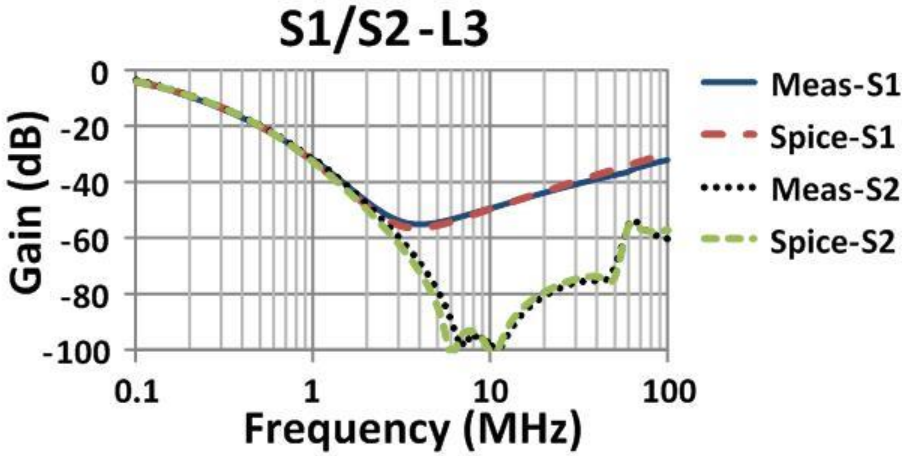




SPICE Simulation Results



SPICE Simulation Model



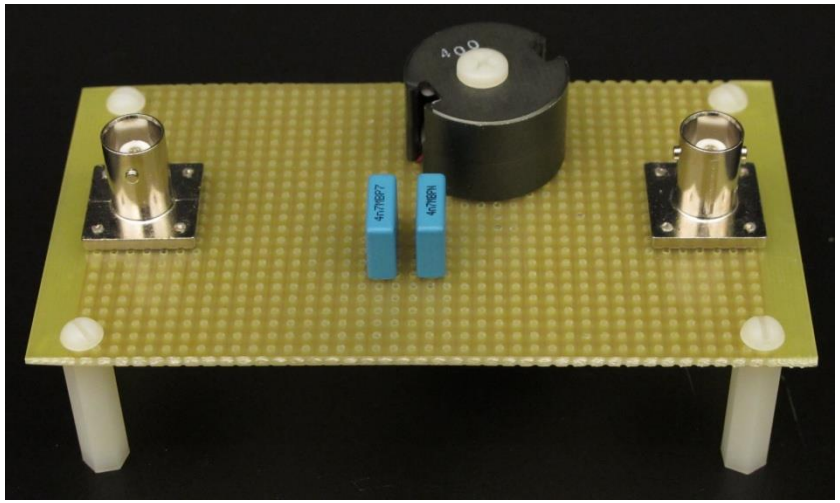
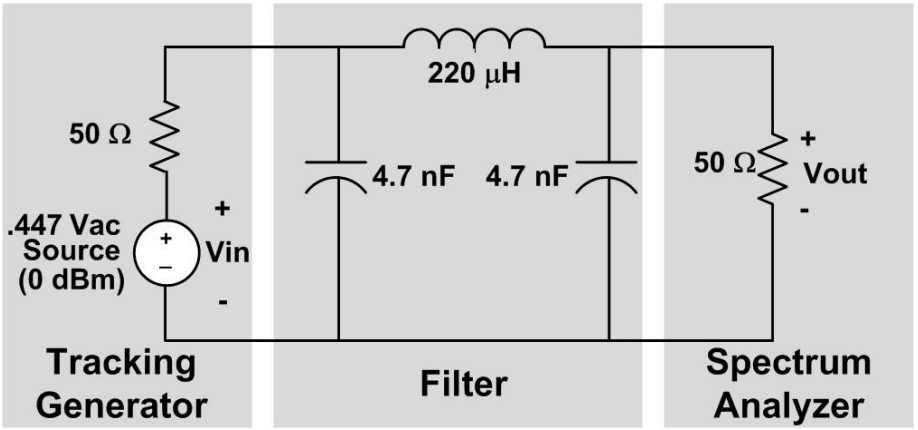
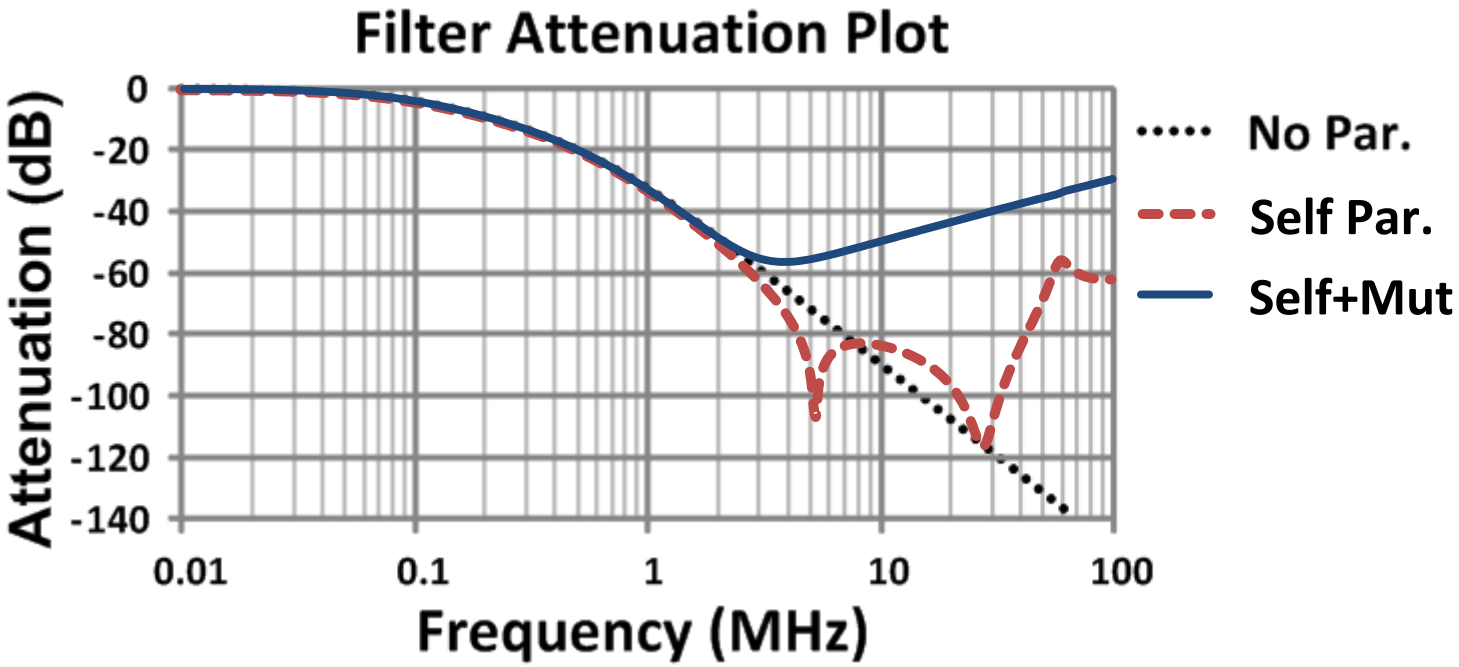


Photo:
Capacitor Setup 1

Effect of Self and Mutual Parasitics





20-40 dB Improvement with good layout (minimize mutual parasitics)

Conclusion

- **EMI Does Not Need to be Complicated**
- **HF Currents Take Path of Lowest Impedance**
  - **Lowest Inductance → Smallest Loop Area**
  - **Best Possible Path**
- **Proper DC Bus Decoupling Minimizes EMI**
  - **Use Low Inductance Interconnect**
  - **Largest μF in Package, Symmetrical Layout, Low Q**
- **Filter Parasitics Important**
  - **ESL of Capacitors, EPC of Inductors**
  - **Part Placement to Minimize Mutual Inductance**
  - **Proper Filter Layout has Big Payoff**