

Politecnico di Torino, Maxwell Room  
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# Davide SCHIAVONE

## EPFL & OpenHW Group



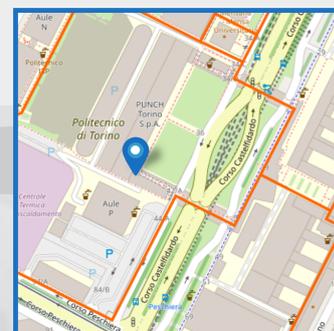
### Bio

Pasquale Davide Schiavone (just Davide) is a PostDoc at the Swiss Federal Institute of Technology Lausanne (EPFL) and Director of Engineering of the OpenHW Group. He obtained the Ph.D. title at the Integrated Systems Laboratory of ETH Zurich in the Digital Systems group in 2020 and the BSc. and MSc. from "Politecnico di Torino" in computer engineering in 2013 and 2016, respectively. His main activities are the RISC-V CPU design and low-power energy-efficient computer architectures for smart embedded systems and edge-computing devices. He visited the Centre of Bio-Inspired Technology at Imperial College London in the Next Generation Neural Interfaces group from January to June 2018. He delivers training workshops to companies and universities.

### Abstract

Thanks to the advances in data analytics algorithms, edge-computing devices are asked to be more energy efficient and performant, still meeting the low-power constraints. On one side, scaling down the transistor size has been working well so far, but it often is not enough. Therefore, specialized architectures (but still versatile) are needed to increase computational and energy efficiency. The ETH Zurich and University of Bologna PULP project faces this challenge by building a multicore microcontroller that leverages near-threshold computing (NTC) and parallel execution based on open-source hardware and open-source customized RISC-V ISA. The success of PULP and its IPs required an organization that curates the maintenance and support of such IPs, providing bug fixes, documentation, and on top of all industrial-grade verification. Such an organization is the OpenHW Group, and as of today, it counts more than 96 members including companies and universities. The availability of open-source high-quality industrial-grade IPs democratized the access of such IPs further, with more universities and companies embracing the projects in a positive feedback loop manner. In this talk, I will discuss the challenges of today's edge-computing platforms, the solutions proposed by the PULP team, and the next generation of edge-computing architectures. I will show some examples of PULP chip implementations and their applications, with performance and energy numbers. and an introduction to the OpenHW Group, its members, work-in-progress activities, and milestones will be presented. Finally, I will show the activities in progress at EPFL concerning RISC-V and its collaboration with the Polytechnic of Turin.

### Location:

Maxwell Room,  
DET, 5th floorPolitecnico di Torino  
IEEE Student Branch