Tech Talk: Introduction to DSP-based SerDes

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Politecnico di Torino, Maxwell Room
May 31st, 2022 - 5:00 PM

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Darjin Esposito

Synopsys

Bio

Darjn Esposito is currently a Senior ASIC Digital Design Engineer at Synopsys, where he is working on the design of high-speed SerDes PHYs. Previously he has worked both in academia and in industry, mainly in the areas of DSP and approximate arithmetic circuits.

Matteo Pisati

Synopsys

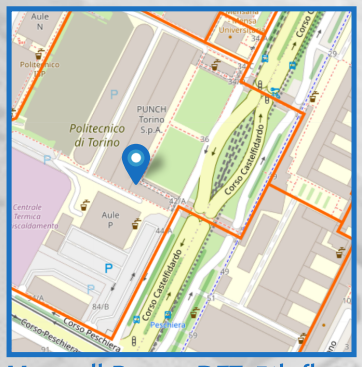
Bio

Matteo Pisati is currently R&D Director at Synopsys, where he is leading the Pavia design center. He has 20+ years' experience in the SerDes field, starting from the MS. and Ph.D. degrees at University of Pavia ('01, '05), going through his experience in the industry, from STMicroelectronics till to Synopsys.

Abstract

The ever-increasing demand for compute power and data processing in accelerators, GPUs, telecommunication networks and mobile devices is requiring wireline and radio frequency transceivers to operate at increasing bandwidths, exacerbating the channel losses. Recent advances in ADCs have enabled the use of DSP techniques to combat sever channel loss and impairments. In this talk an introduction to DSP-based SerDes will be covered, with a focus on the digital design challenges.

Location:



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