EDA Technologies Fueling IoT Implementation, Current and Future

Michael Thompson
Internet of Things (IoT) Summit, RWW 2018
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IoT Standards/Applications
Industry Trends and Business Considerations

Profitability

• Economy of Scale vs Performance, Development Costs
  – Is smaller better; smaller process node-more devices
  – One process does not fit all
  – Multi-Technologies needed
  – Manufacturability

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.”

Gordon Moore

*Cramming more components on to Integrated Circuits*

Electronic Vol 38 Num 8, April 19, 1965
High Level System Partitioning

RF Front End Communications
- RF/AFE
- DFE
- PHY
- MAC

Interfaces

Security

Memory

CPU

DSP Core
- Audio & Voice
- Noise, Image, Video Processing
- Vector Processing

Sensors Interface

Power Management

Sensor(s)
Some EDA Challenges

- Shrinking Device/Process Size – Advanced Nodes
- Manufacturing Advanced Nodes
- Multi-Technology Designs
  - Si, SiGe, SOI, InP, GaN, GaAs
  - Surface Mount Devices (SMD)
  - Alumina, Duroid, Flexible Substrated
- Model Support of Devices
- Multi-Technology Simulation
- Physical Effects

Design teams need to easily and quickly prototype designs requiring agile editing to quickly work through design optimization but that use manufacturable parts and processes that can be controlled. The specification of the design and design validation must be based on Standard’s requirements.
Advanced Nodes
Double Patterning LELE

SiO$_2$

SiN
Smaller and smaller process nodes have unique fabrication requirements

The way we design at 7/8nm is very different than 28nm…
Virtuoso® Advanced Node

- Virtuoso® Advanced Node is the industry standard for advanced node custom/analog design
- Breakthrough release supporting novel design methodologies required at advanced nodes
- Continued partnership with leading foundries and customers to define and develop new custom design methodologies

“Through our strong collaboration and continued partnership with Cadence, we have been able to develop and deploy a custom design methodology based on the Virtuoso Advanced-Node Platform. With our recent successful tapeout, we took advantage of its many unique capabilities designed to manage the challenges presented at 7nm.”

Ching San Wu, general manager of Analog Design and Circuit Technology at MediaTek
Virtuoso® Advanced Node ICADV 12.X
A brief history

First advanced node release
FinFET editing
First generation DPT support
16nm/14nm rules support
In-design DRC support

12.1

Advanced layout methodology
Electrically driven optimization
Place & route integration
7nm and beyond rules support
Next generation MPT support

12.2

Fully colored MPT flows
Enhanced FinFET editing
SADP routing support
10nm rules support
In-design electrical checking

12.3

12.1 Launched Nov 2012
12.2 Launched Nov 2015
12.3 Launched Dec 2016
Fundamental challenges designing at advanced nodes

- The reality is that as process nodes get smaller and smaller, custom layout times get longer
  - Project schedules are also simultaneously being reduced
  - To maintain this, the layout teams need to be larger
    - Hire more contractors…
    - Need a better approach

- Collaborate closely with customers and foundries to define targets to build solutions/PDKs/methodologies to address this problem
Foundry collaboration and enablement is key
Closing remarks

Though 7nm and below presents a host of new challenges, Virtuoso® Advanced Node has been expanded with close collaboration with foundries and early adopters to detect, prevent, and fix problems before they occur.

Virtuoso Advanced Node has been updated to handle color-aware layout, new high-density interconnect layers, and all new 7/8nm DRM rules.

Just the beginning — Cadence continues to proactively collaborating to define new flows, methodologies, and functionality for an even better designer experience at 7nm and beyond.
Front-End Shrink

Real Estate Is Expensive
Radio Design Flow Challenges

RF sections at one time were sacrosanct and the designer could count on stay-out regions. That no longer occurs.
The reduction of the RF volume continues to place more and more importance on Extraction and EM simulation.
Integrated EM, Multi-Engine Support  
FEM, MoM, PEEC, FDTD

- Integrated RFIC solution by leveraging the Virtuoso® platform and Sigrity™ PowerSI® 3D-EM Extraction Option

- Sigrity 3D-EM setup for passive structure extraction inside the Virtuoso platform and launch Sigrity 3D-EM simulation
3D EM in Virtuoso
RF-module Simulations
Annotating Extracted view on RF-module Master Schematic
EM In Design Flow
Design Flow
Design Flow Goals

Golden Schematic

- Design Trade-Offs, Optimization
- Design Review, Sign-Off
- Layout Generation
- Design Verification
- Manufacturing
Adding RF and Module Elements

- Multi-Technology: IC, SMD, Laminate, Board
- Any Angle Placement
- Arcs, Rounded End Caps, Transmission Lines
- Editing
- Library Sorting Features

Expanded Transmission Line Library
Bondwire Construction
Dynamic Voiding
Library Structure for SMD Piece Parts
Multi-Technology (Die and Package) Editing in Concert
RF Design Flow

Single Unified EM Analysis Environment
Common EM View

Multiple EM Analysis Techniques

- PEEC
  Quasi Static
- MoM
- Sigrity
  3DEM
- FDTD
Design To Test
Design Two Test Flow

<table>
<thead>
<tr>
<th>Behavioral System Models</th>
<th>Design &amp; Verification</th>
<th>Pre-Silicon Chip Validation</th>
<th>Silicon Bring-up Characterization</th>
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<td>Analog</td>
<td>Prototype</td>
<td>Silicon</td>
<td>Silicon</td>
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```
always@ (clock):
  B <= A;
  C <= B;
  D <= C;
end
```
Virtual PA Test
Like Continuous Process Improvement in manufacturing, the EDA industry faces similar challenges and paradigm shifts. Considerable R&D effort is expended each year for the EDA industry to track and work with foundry advancements, device model changes, and new Standards.
Thank You For Your Attention.....

....and Happy Connections