Printed Circuit Board EMC Design Reviews

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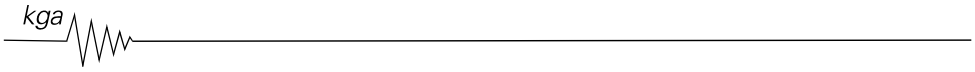
Why Do Circuit Board EMC Reviews?



Identify/prevent/fix problems early in design phase

- A few hours now can save lots of grief later

Easy to do, so why not just do it?

- NOT a full blown review -- focus on EMI/EMC issues only
- Software not needed (but can be helpful)
- One or two hours often enough

Best Times?

- Phase I - Block Diagram
- Phase II - Schematic
- Phase III - Board Artwork

Three General Tasks
(Before you Start)

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Identify *EMC Threats*

- Five Key Threats
  - Radiated & Conducted Emissions (RE/CE)
  - Radio Transmitters (RFI)
  - Electrostatic Discharge (ESD)
  - Power Disturbances (EFT, Lightning, Power Quality)
  - Self Compatibility (Signal Integrity, Mixed Technlogies)
- *Applicable regulations may NOT be adequate*

Identify *Key Circuits*

- Digital - RE/CE, ESD, EFT,SI
- Analog - RFI, RE
- Power - CE, EFT, Lightning, PQ

Identify *Other Design Constraints*

- Cost, volume, weight, space, power...
- *Don't forget to include the "cost of failure"*

EMC Circuit Board Review
(Top Ten EMC Concerns)

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Critical Circuits

- Clocks
- Resets/Interrupts/Control
- Analog
- Power Regulators
- RF Transmitters & Receivers

Board Construction

- Stackup
- Split Planes
- Floor Planning & Trace Routing

Board Periphery

- I/O & Power Interfaces
- Grounding

May Not Prevent ALL Problems - But Will Prevent > 90%

Design Review Tip #1
CLOCK CIRCUITS

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Problems

- Clocks are primary sources of high frequency emissions
- Other highly repetitive circuits also contribute to emissions
  - Memory control (ALE)
  - Busses

Solutions

- High frequency decoupling directly at Vcc
  - Supplement with series ferrites
- Series resistors in output
  - 10-33 ohms typical
- Crystals or resonators next to oscillator

Example
CLOCKS

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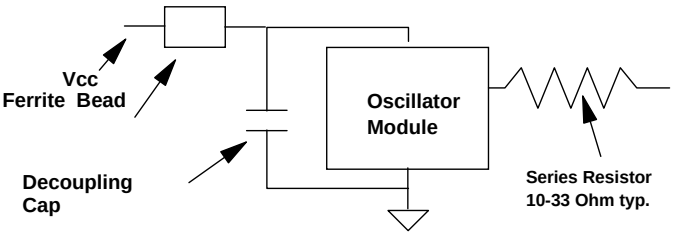
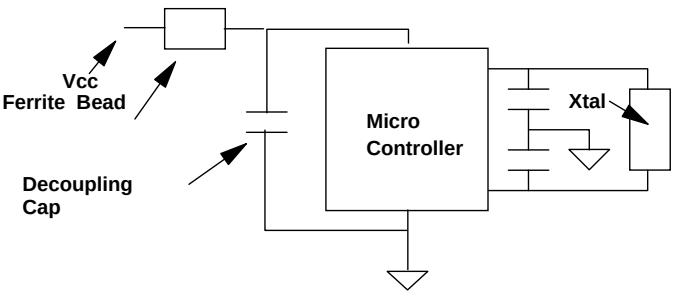
Example 1



Example 2



Clocks are the major source of radiated emissions

Design Review Tip # 2
RESET/INTERRUPT/CONTROL CIRCUITS

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Problems

- Reset circuits are very vulnerable to ESD, EFT, and transients
- Interrupt & control circuits also vulnerable
  - Non-Maskable Interrupts critical
  - Read/Write control critical
- Lines to mechanical switches are especially vulnerable

Solutions

- Filter wherever reset enters from off-board
- Protect voltage supervisor at component
  - Decouple supervisor at Vcc
  - Decouple supervisor at reference
  - Decouple output if over 2 inches
- Supplement with ferrites as needed
- Apply similar fixes to interrupt/control circuits

Example
RESET CONTROLLER

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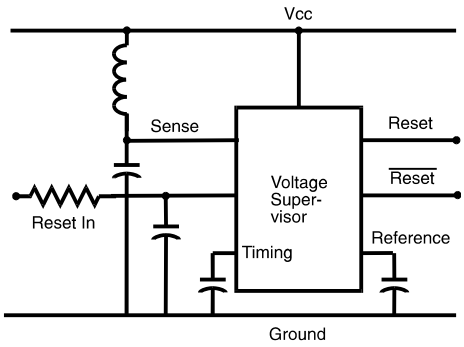

Reset Circuits are the Susceptibility Equivalent of Clocks

Design Review Tip # 3
ANALOG CIRCUITS

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Problems

- RFI upsets sensitive analog circuits
- Parasitic oscillations also possible

Solutions

- Decouple all voltage supplies to analog chip with HF caps
- High frequency filter all lines to chip which leave the board
  - Both input and output
- High frequency filter reference voltage (if not grounded)
- Consider small cap (10-33 pF typical) across inputs
  - Only as a last resort - may affect circuit operation
- Filtering often necessary at remote sensor too

Example
ANALOG INPUTS & OUTPUTS

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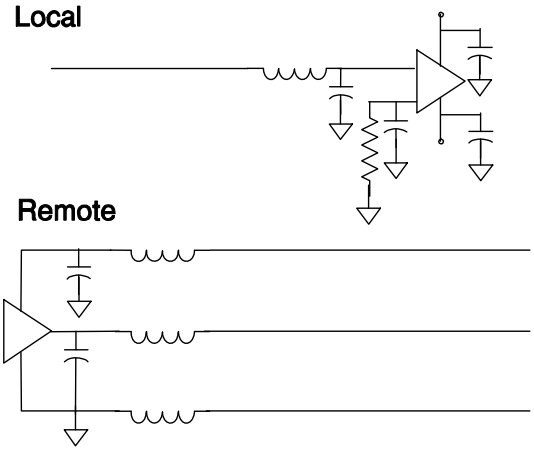

Low frequency **circuits can still be upset by** ***high frequency*** **EMI**

Design Review Tip # 4
VOLTAGE REGULATORS

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Problems

- Upset from RFI
  - Rectification results in out of tolerance Vcc
- Parasitic Oscillations
  - Common in VHF/UHF frequency range

Solutions

- High frequency decoupling at input/output (1000 pF typical)
- Short, direct connections mandatory
- Connection to device "neutral" pin - not necessarily "ground"
- May supplement with series ferrites if needed

Example
REGULATOR "RF" EMISSIONS & IMMUNITY

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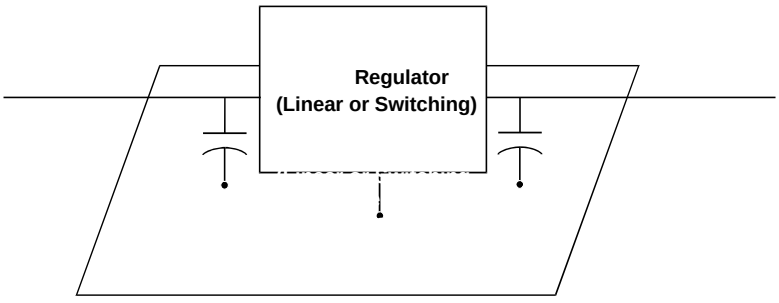

Regulators can cause subtle EMI problems

Design Review Tip # 5
RF TRANSMITTERS & RECEIVERS

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Problems

- On board receivers jammed by digital and other "noise"
  - GPS particularly critical due to extremely low levels
  - Wi-Fi and cellular also vulnerable
- On board transmitters jam analog circuits

Solutions

- Protect receiver inputs
  - May need special bandpass filtering
- Internal shielding ala "TV tuner"
- Clock management -- avoid harmonics
  - Example - GPS L1 = 1.57542 GHz
- Antenna location and cable routing
- DSP or other software techniques
- Avoid "Frequency Hopping" & "Direct Sequencing" in same bands

Newly Emerging Problems...

Design Review Tip # 6
BOARD STACKUP

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Problems

- Multiple trace layers with no adjacent planes
- Random stackup of power/ground planes
  - Power planes optimized for delivering power, not EMC
  - Ground planes not optimized at all
- Random splits in planes with no thought to adjacent traces

Solutions

- Keep Every Signal Layer Adjacent to a Plane
  - Close coupling to planes preferred
- Keep Respective Power & Ground Planes Adjacent
  - Can insert traces in between with some loss of coupling
- Bury High Speed Traces
  - Residual emissions from components
- Maintain a Symmetrical Stackup
  - Preferred for mechanical and thermal reasons
- Consider Outer Ground Planes
  - Can connect with vias around edge to form a "Faraday cage"

Example
SIX LAYERS & BEYOND

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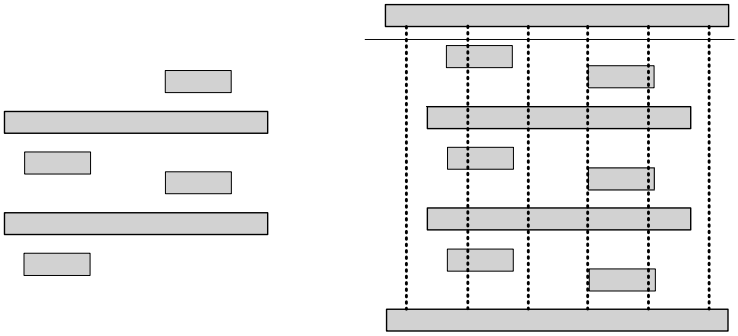

Six Layer Board With Embedded Traces

Ten Layer Board With Outer Layers Stitched

For six layers or more, embed critical traces
- Clocks and Busses
- Resets, Interrupts, Control Lines
- Use Close Spacing between Traces and Planes

Design Review Tip # 7
SPLIT PLANES

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Problems
- Traces across cuts
  - High speed traces critical, but even "slow" traces can cause problems
- Overlapping planes
  - Can allow unwanted coupling at high frequencies (ESD, RFI)

Solutions
- Don't cross cuts with high frequency traces
  - Can bridge with small capacitor (1000 pF typical)
- Eliminate "Over & Back" Traces
  - Provide adjacent returns with filtering as needed
- Always Align the Planes

Example
MIXED TECHNOLOGY ISOLATION
Analog, digital, power

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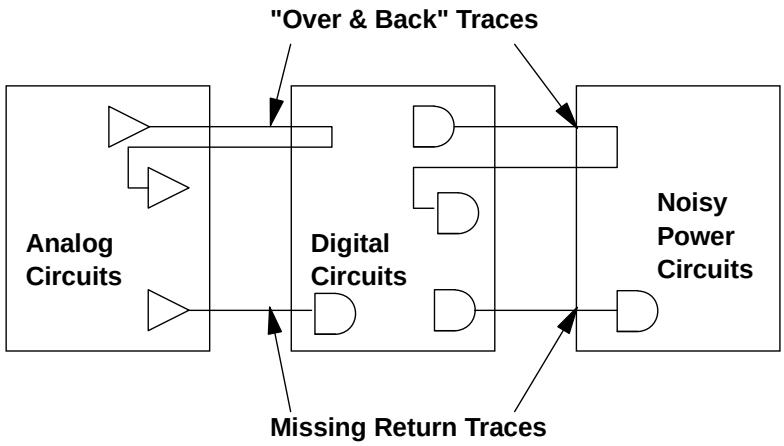

Example
ALWAYS ALIGN THE PLANES

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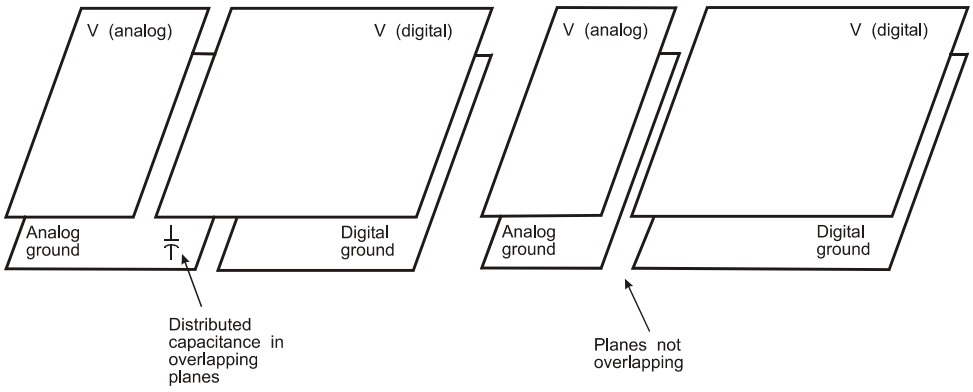

Prevent Problem by Eliminating Overlaps - Stack, Don't Overlap

Design Review Tip # 8
FLOOR PLANNING & TRACE ROUTING

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Problem

- Random placing of components
- Random trace routing
  - *Kimmel's Law - Autorouters will route to maximize EMI.*

Solutions

- Placement
  - Segregate components according to frequency
  - Position devices for minimum clock runs
  - Avoid placing critical circuits (clocks, resets) near I/O ports
- Routing
  - Separate high and low speed signal lines
  - Route high speed lines first; keep short and direct
  - Check for traces across cuts
  - Be aware of crosstalk
  - Manually route critical traces when possible

Example
GOOD FLOOR PLANNING

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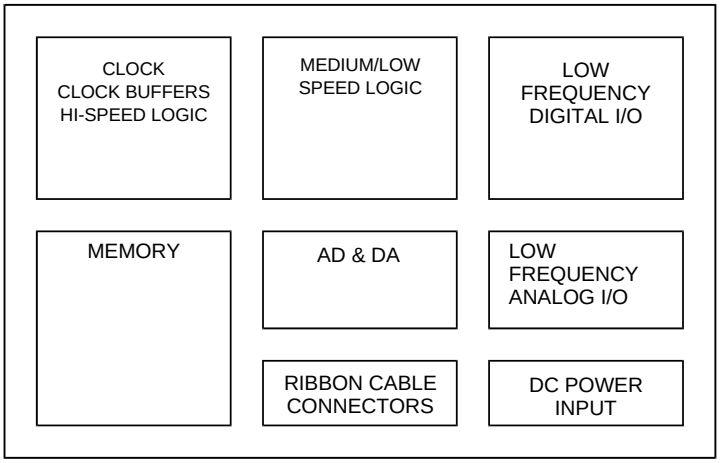

Good partitioning is essential to good trace routing

Example
POOR CLOCK LAYOUT

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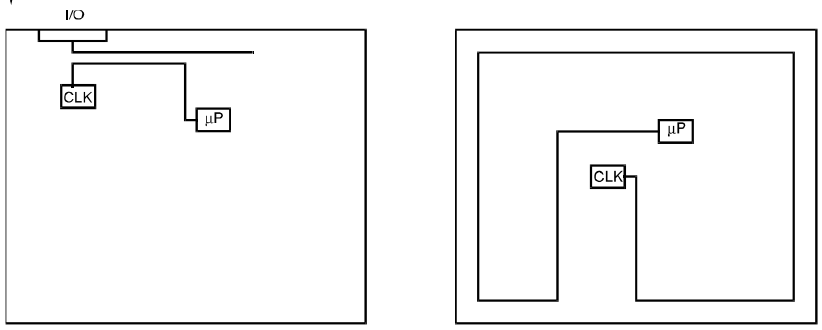

Example 1

Clock next to I/O

Example 2

Clock Routing

Poor layout results in increased emissions
- Clock lines couple to I/O lines
- Clock lines radiate directly

Poor Clock Routing is a Major Contributor to Emissions Failures

Design Review Tip # 9
PROTECT THE PERIPHERY

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Problems
- Power & I/O connected to the "outside world"
- Busses may need attention too

Solutions
- Power Interface
  - Minimum - install 0.01 µF caps across all power inputs
  - For more protection - add series ferrites to VCC lines
- Input/Output Lines
  - Add low pass filters protection to all I/O lines - ferrites, caps, or RC
  - Filter everything above 10X the data rate
  - Add transient protection to I/O lines exposed to ESD, etc.
- Bus Interfaces
  - Consider small caps on critical lines

Example
I/O BANDWITH SOLUTIONS

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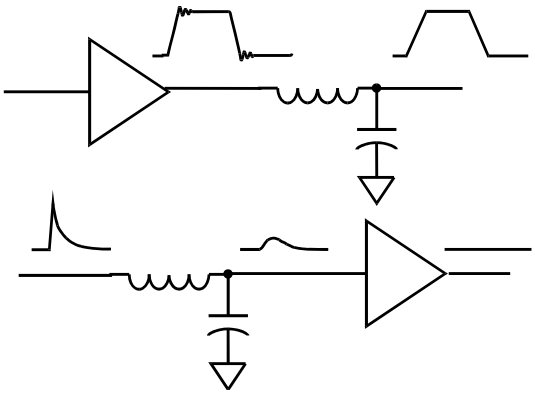
Limit bandwidth to that needed for system requirements

- Select slow circuits
- Limit bandwidth by filtering
- Ensure filtering is adequate at the highest threat frequency



For emissions, keep high frequency currents on the board..
For immunity, keep high frequency currents off the board...

Example
POWER LINE EMI FILTER

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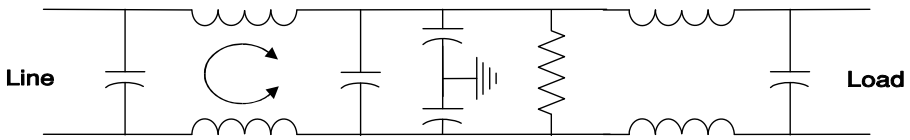

Note both *common mode* and *differential mode* filtering

Design Review Tip # 10
PCB GROUNDING

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Problems

- Confusing grounding approaches
  - Not enough grounds
  - Too many grounds
  - Where to ground?

Solutions

- Digital/RF electronics
  - *Multi-point grounds* with short/fat connections
  - Inductance and wavelength effects predominate
- Low Level/Low Frequency Analog
  - *Single point grounds* to control ground loops
  - Not as critical for "high level" analog
- Mixed technologies
  - *Hybrid grounds*
- Where you ground as important as how you ground

Example
CHASSIS GROUND CONNECTION AT I/O PORTS

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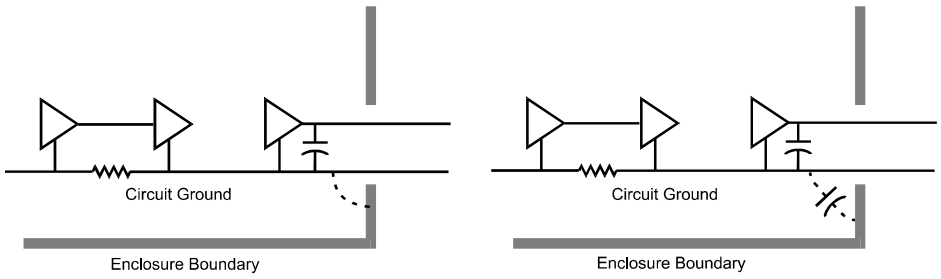

Establish Low Impedance Connection at I/O Ports

Common mode ground noise currents cannot be filtered at the circuit board

Currents must be intercepted at the connector to keep currents off cables

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Example
PCB HYBRID GROUND

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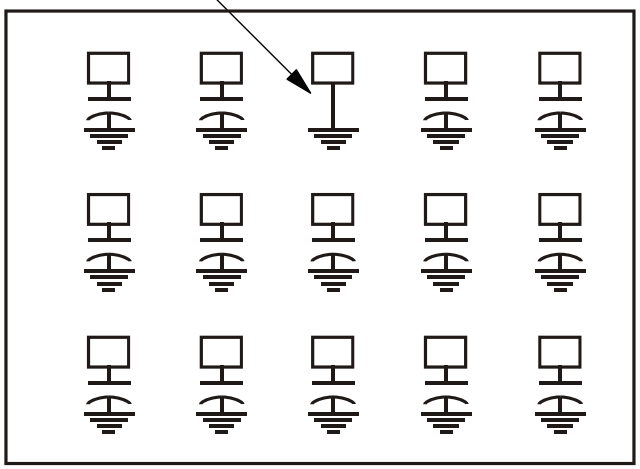
Pad With Solid Connection
To PCB Ground Plane

All Other Pads Connected
By 1000 pF Capacitor



This provides a "Single Point Ground" at 60 Hz
and also provides a "Multi-Point" Ground at RF

DESIGN REVIEW CHECK LIST
Circuit Level

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Clocks
- Vcc - decoupling cap (optional ferrite)
- Clock out - series resistor

Resets/Interrupts/Control
- Vcc - decoupling cap
- Inputs - high frequency filtering
  - Serious filtering on external reset inputs
- Outputs - high frequency filtering as needed

Analog
- Vcc - high frequency decoupling
- Inputs (including reference) - high frequency filtering
  - Optional small cap across inputs
- Outputs - high frequency filtering as needed

Power Regulators
- 1000 pF caps input and output to neutral pin

RF Transmiiter/Receivers
- Receiver inputs - keep noisy circuits/traces/cables separated
- Frequency management of clocks
- Shielding (modules common)

DESIGN REVIEW CHECK LIST
Board Level

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Board Stackup
- Every trace layer adjacent to a plane
- Planes are paired
- High speed traces buried

Split Planes
- No traces across cuts
- No overlapping planes

Floor Planning/Trace Routing
- Components grouped by function/speed
- Critical traces routed to minimize EMI
- No clocks/resets adjacent to I/O

I/O and Power
- Filters and bandwidth on I/O
- High frequency capacitors on power
- Transient protection as needed

PCB Grounding
- I/O chassis grounding at connectors
- Multi-point connections for high frequency boards
- Hybrid or single-point connections for low frequency boards

Closing Thoughts...

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Advantages of an EMC Board Review...
- Save Money
  - One less trip to the test lab can save $10-20K
- Get to Market Sooner
  - Grab market share
- Keep Your Boss Happy
  - If the boss is happy, everybody is happy...

Keep it simple...
- Grab a buddy -- two heads are better than one
  - Don't make it a big production
- Focus on EMC issues only
  - A couple of hours per board is often enough

An ounce of prevention is worth a pound of shielding...