Latch-up Testing

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September 2013

Agenda

- Introduction
- What is Latch-up?
- EAG test capabilities
- Overview of the Latch-up test
- Latch-up Testing Challenges
- Latch-up Test Guidelines
- What's coming in JESD78E
- References and advanced topics

QUIZ QUESTION #1

Q: What's the current revision of the JEDEC latch-up spec?

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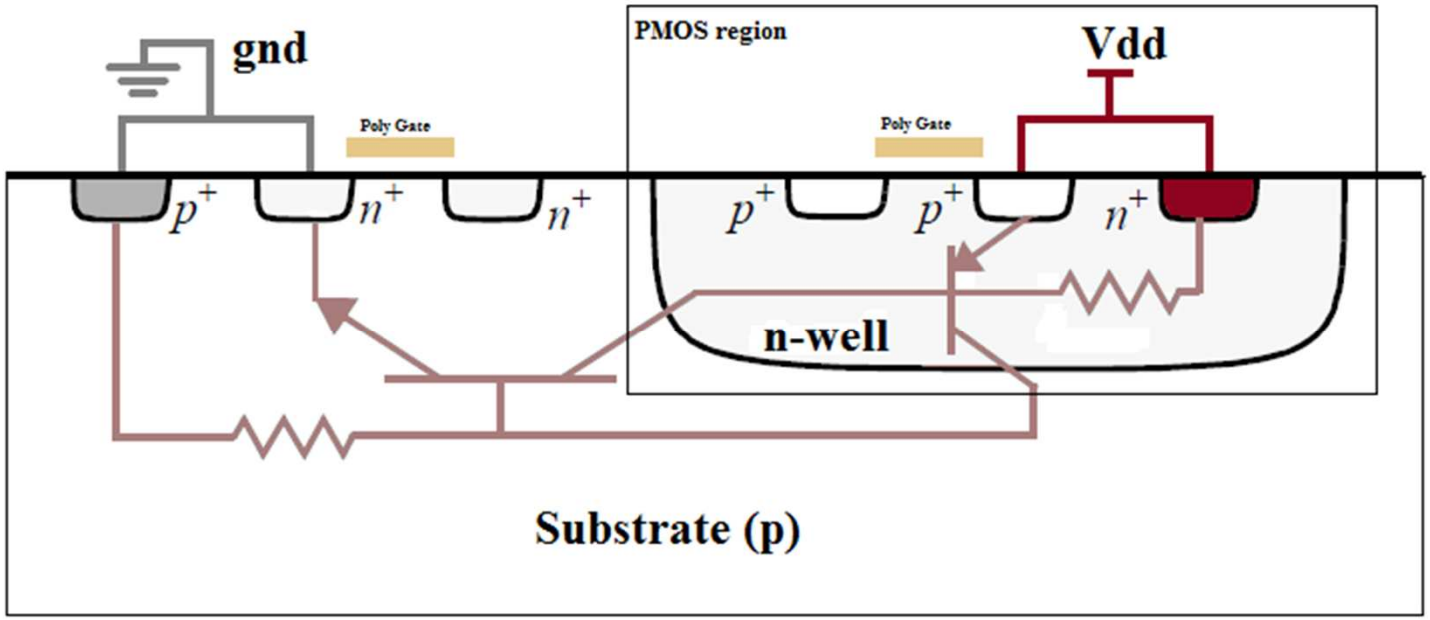
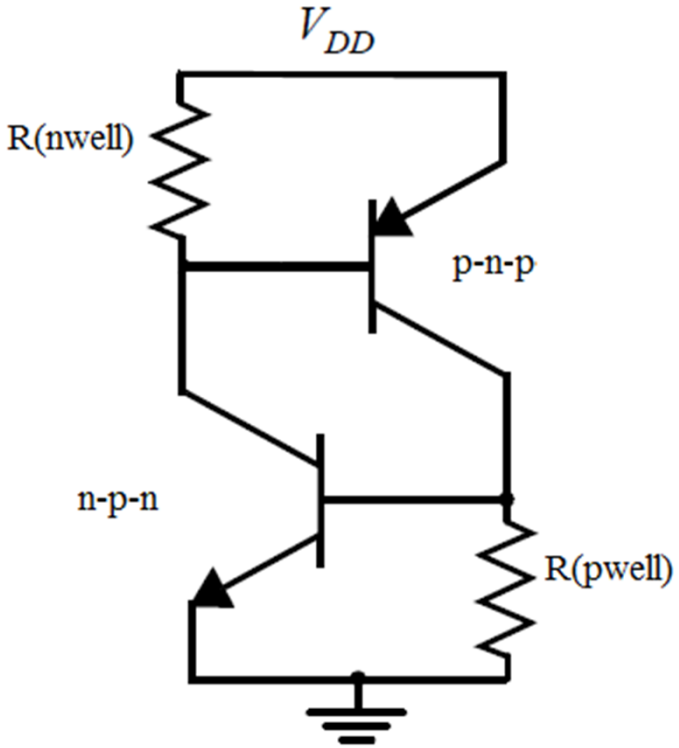
A: Revision D

What is Latch-up?

When a thyristor formed from parasitic transistors in a CMOS, NMOS, or BiCMOS circuit is triggered and causes high current to flow, ***latch-up*** has occurred.



Reducing the Incidence of Latch-up



- Many latch-up problems are reduced by design (increased spacing, lower transistor gain, lower voltages, guard ring structures, etc.)
- Some IC processes (SOI, for instance) eliminate latch-up completely.
- As process technologies shrink, latch-up becomes harder to avoid.

EAG Latch-Up Test Capabilities

- Talented Engineering Staff
- Thermo Fisher Mk.2 & Mk.4 systems
- Four Mk.4 systems in two locations
- All systems fully loaded
- Testing To 2,304 Pins
- Up to seven dedicated supplies
- Vector depth of 256K Vectors
- Vector voltage 0-5V
- Temperature Forcing
- Adapter Boards for all platforms
- PCB design capability

Current Latch-up Spec

- Revision D, November 2011
- NMOS, CMOS, bipolar and combinations
- Class I = Room Temperature
- Class II (recommended) =
  - Maximum operating ambient temperature *OR*
  - Maximum operating case temperature *OR*
  - Maximum operating junction temperature
- Sample size = 3 units (6 units in previous revisions)
- A wide range of currents can be used for the I-test; there's no Class A (+/-100mA) and Class B (other specified current) designation.
- The spec is becoming a characterization spec.

JESD78D – New Test Limits

- Current Limits as per Table 1

Table 1 — Current and voltage trigger conditions

Test	Trigger	
	Force current/voltage	Voltage/current limits
Positive I-Test	< 50 mA	See Footnote 3 in Table 2
	50 to < 100 mA	
	100 to < 150 mA	
	150 to < 200 mA	
	> = 200 mA	
Negative I-Test	> -50 mA	See Footnote 4 in Table 2
	-50 to > -100 mA	
	-100 to > -150 mA	
	-150 to > -200 mA	
	< = -200 mA	
Over-voltage Test	1.5 x VDD or MSV, whichever is less	See Footnote 2 in Table 2

- Positive I-test Voltage Limit: 1.5 x V_{DD} or MSV
- Negative I-test Voltage Limit: -0.5 x V_{DD} or MSV

QUIZ QUESTION #2

Q: What does MSV stand for?

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A: Maximum Stress Voltage

Maximum Stress Voltage (MSV)

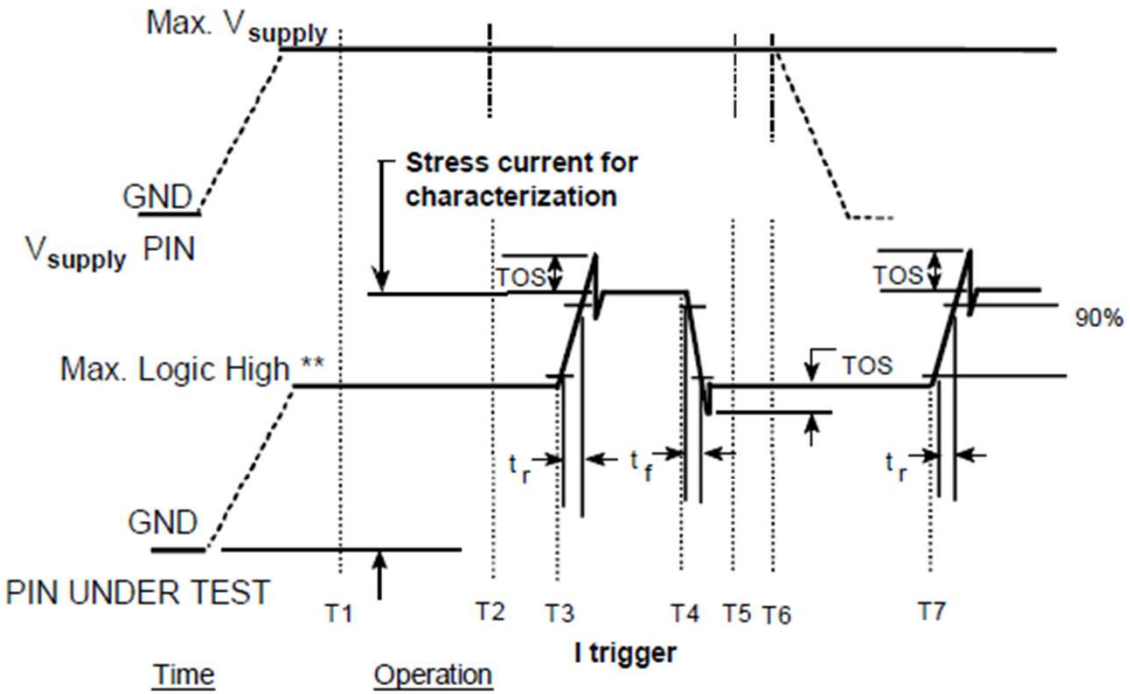
- **Maximum Stress Voltage (MSV)**: The maximum voltage allowed to be placed on any given pin during latch-up immunity testing without causing catastrophic damage to the device due to electrical over-stress (EOS).

  - MSV is *NOT* the same as the absolute maximum voltage rating from the device data sheet.
  - MSV is *higher than the maximum operating voltage* (default is 1.5 x Vmax).
  - MSV can depend on pulse width, pin under test, and polarity.

Overview of the latch-up test

- All power rails are turned on, and the part is put in a stable, low current state, with unstressed inputs LOW or unstressed inputs HIGH.
- Supply currents are measured.
- Stress is applied to the part and then removed.
  - Current test, positive and negative, all non-supply pins, *OR*
  - Supply Overvoltage (SOV) test, each supply group
- Supply currents are measured again.
- If supply current after stress is too high, the test is flagged as a latch-up failure.
- Failure criteria: for Inom ≤ 25mA, >(Inom + 10mA); otherwise, > I.4 x Inom
- Part is powered down (optional).

Positive I-test Sequence



Time	Operation
T1 → T2	Measure nominal I_{supply} (Inom)
T4 → T7	Cool down time (Tcool)
T4 → T5	Wait time prior to I_{supply} measurement. *
T5	Measure I_{supply}
T6	If any $I_{supply} \geq$ the failure criteria defined in 1.3, latch-up has occurred and power must be removed from DUT.

QUIZ QUESTION #3

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1. 100mA is seen on the pin, but the voltage is less than the MSV.
2. The MSV is seen on the pin, but the current injected is less than 100mA.
3. 100mA is seen on the pin, and the voltage is equal to the MSV.

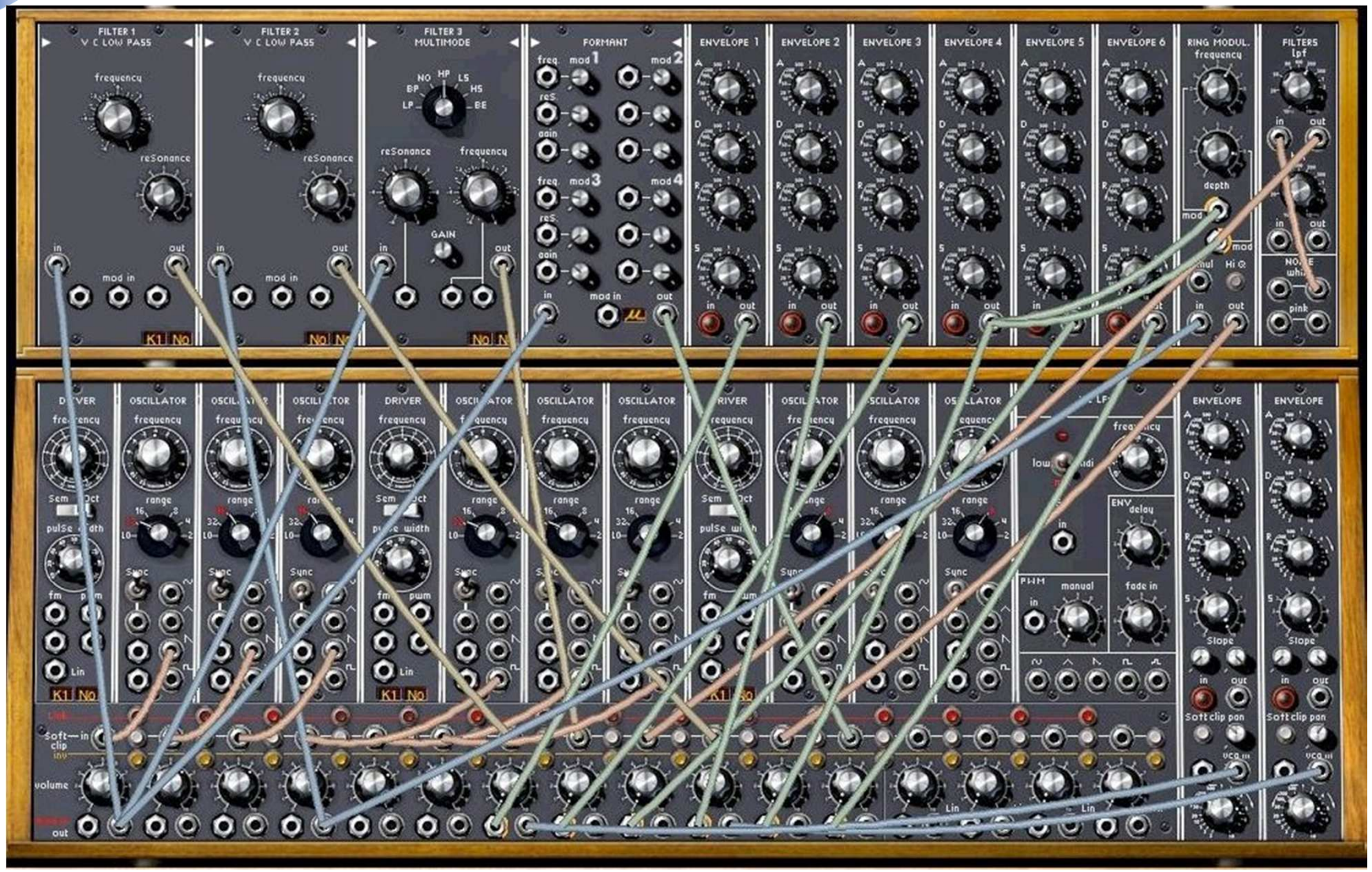
Timing Specifications

Table 3 — Timing specification for I-test and V_{supply} overvoltage test

Symbol	Time interval	Parameter	Limits	
			MIN	MAX
t_r		Trigger rise time	5 µs	5 ms
t_f		Trigger fall time	5 µs	5 ms
T_{width}	T3 to T4	Trigger duration (width)	2x T_r	1 s
TOS		Trigger over-shoot	+/- 5% of pulse voltage	
T_{cool}	T4 to T7	cool down time	> = T_{width}	
$T_{measure}$*	T4 to T5	Waiting time before measuring I_{supply}	3 ms	5 s

* The wait time shall be sufficient to allow for power supply ramp down and stabilization of I_{supply}

Why Latch-up is Challenging:



Too many knobs that you can turn!

QUIZ QUESTION #4

Q: What are the requirements for passing the latch-up test?

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A:

- Part must not show latch-up during the I-test or SOV test.

  AND

- Part must pass ATE.

Stable Low-current State

- Some stable, low-current states include:
  - Reset
  - Sleep
  - Iddq
  - Stand-by
- Stable, repeatable, and realistic are *more important than the absolute lowest current.*
- Leakage in advanced CMOS processes may necessitate high currents on some supplies.

Stable Low-current State (2)

- To put the part in the proper state, you may need:
  - Proper supply sequencing
  - Static preconditioning (subset of pins held always high or always low)
  - Simple reset sequence (4 pins or less, 6 states or less)
  - Vector preconditioning (up to 2304 pins, 256K states, up to 20MHz)
  - External components (not recommended unless absolutely necessary)

Test Guidelines – Supplies

- During stress, supplies should be set to Maximum Vsupply. (There are exceptions in Revision E.)
- Supplies at the same potential may be grouped together.
- Use engineering judgment when grouping supplies.
  - Don’t group high current supplies with low current supplies.
  - Use separate supplies to state inputs when possible.
- Mk.4 system can provide up to seven supplies to bias the part and state inputs.
- Voltage range is 0-100V.
- For <10V, total current on all supplies is up to 18A.
- Maximum current on one supply is 10A.

Test Guidelines – Stating Inputs

- All unstressed inputs, I/Os configured as inputs, and HiZ I/Os will be stated for the inputs LOW and inputs HIGH states.
- All outputs and I/Os configured as outputs will float when not under test.
- Parking the pin under test
  - In the positive I-test, the pin under test should be parked HIGH.
  - In the negative I-test, the pin under test should be parked LOW.
  - Output or I/O pins in an unknown state can be floated prior to the I-test.
- Preconditioned pins
  - In most cases, Pins held LOW only receive the negative I-test, and pins held HIGH only receive the positive I-test.

Test Guidelines – Special Cases

- Differential inputs
  - When p side is low, tie n side high and vice versa.
  - Arbitrarily choose p side low as inputs LOW.
- Outputs of voltage regulators (VREG), VBAT or charge pumps
  - Don’t treat them as supply pins; treat them as output pins.
  - Use engineering judgment to decide the proper way to do the I-test on these pins.
- Disable PLLs prior to latch-up testing if possible.
- I/Os with internal pull-ups to supply may need a separate supply to be stated LOW.
- I/Os with internal pull-downs to GND may need a separate supply to be stated HIGH.

What's coming in JESD78E

- Timing changes
- MSV determination guideline
- Revised test procedure
- When to test with supplies at <Vmax
- Other changes:
  - Annex with analog pin testing example
  - Annex with high voltage testing example
  - Recording and reporting

JESD78E – Timing Changes

- Rise and fall time changes
  - From a minimum of 5 us and a maximum of 5 ms to a minimum of 1 us and a maximum of 100 ms
- Redefine timing points
  - Include new points: two ends of rise time and two ends of fall time
  - Two measurement periods, one for pre-stress and one for post-stress
  - Two cooling periods, one for pre-stress and one for post-stress
  - A more precise definition of pulse width (from the end of rise time to the beginning of fall time)
- Affects Table 3 and Figures 2-4

JESD78E – Determining MSV

- Positive tests (I-test and supply overvoltage)
  - Start with VABSMAX as the VCLAMP and over-voltage values
  - Perform preliminary test to understand the reaction of the device at room and hot temperature
  - Schmoo the VCLAMP and over-voltage values from VABSMAX to the process breakdown voltage (BV) to determine the highest non-destructive voltage as initial MSV
- Negative tests (I-test)
  - Schmoo the negative VCLAMP from -0.7V to -0.5 X VCCMAX to determine the lowest voltage that does not lead to catastrophic damage at both room and hot temperature

JESD78E – Test Procedure

- Breaks sections 4.2 (I-test) and 4.3 (overvoltage test) into subsections: Device preconditioning and stabilization, Test conditions and sequence, Test procedure combinations (logic high versus logic low for unstressed pins)
- Adds a new Table 5 for the I-test of analog pins.
- Adds a new section 4.3.3 for the overvoltage test of analog pins.
- Adds section 6 and Table 6 for the classification of devices. (Similar to Table 1 in the existing spec)

QUIZ QUESTION #5

Q: When is it a good idea to test a part with the supply at less than Vmax?

JESD78E – Testing at <Vmax

- In the I-test, the voltage compliance level should not be set above the maximum stress voltage (MSV).
- Sometimes, the maximum stress voltage of a signal pin may not be high enough to force the desired trigger current.
- In this case it is highly recommended to perform additional tests with the power supply voltage below the maximum operating power supply voltage, so that the signal pin's clamp voltage is a full diode drop V_{diode} above the power supply.
- The lower power supply voltage should still be in its normal operating range.
- For the negative I-test, the compliance voltage should not have an absolute value of <0.7V.

Latch-up References

- Some additional references
  - Haseloff, Eilhard “Latch-Up, ESD, and Other Phenomena” (TI Application Report, 2000)
  - Wybo, Geert (et al), “Analysis Methodology for Latch-up: Realistic Worst Case Stress Conditions for the Current Injection I-test” (RCJ symposium Japan 2008)
  - Dasgupta, Dr.Nandita, Lecture on Latch-up

    http://www.youtube.com/watch?v=QlwcPjHpnH0&feature=related
    (Department of Electrical Engineering, IIT Madras)
- Other latch-up topics beyond the scope of today’s discussion
  - Radiation, ESD, or other transient induced latch-up
  - High voltage latch-up testing
  - Latch-up testing with one or more high current supplies

Microelectronics Test and Engineering

- **ATE Test Development and Pilot / Production Test**
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