# IEEE Components, Packaging and Manufacturing Technology Society – OC Chapter

## Tuesday, April 30, 2013 Technical Meeting

# DRAM Market Forces of Fragmentation & Consolidation

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### Orange County, California USA

## Abstract

The market for DRAMs (Dynamic Random-Access Memory) has been a dominant force in computer architecture choices, and a healthy friction always exists between the compromises made for mass adoption and the needs of specific applications. One mainstream architecture thread – Fast Page through SDRAM through DDR – has dominated the scene but there have been a number of interesting successes and failures to fray from that thread, and many more are on the horizon. Sometimes it's amazing what tricks people play to squeeze performance from a technology. Throughout these transitions and experiments one truism never changes: the tradeoff of volume and price drives success.

## Biography



Bill Gervasi has been involved in the definition of Double Data Rate SDRAM since its earliest inception. His background is in computer sciences and career highlights include 19 years at Intel where over the years he was systems hardware designer, software designer, and major accounts manager. Bill Gervasi joined Intel in 1976 in the computer systems group manufacturing department, eventually leaving Intel in 1995. During that period, the computer industry changed from computers that filled rooms the size of basketball courts to desktop and laptop form factors in nearly every home in the world.

Since then, Mr. Gervasi specialized in the computer memory technology arena, getting involved in international standards and battles for global dominance for this key part of computer systems. He subsequently was with S3 where he was a graphics architecture specialist and at Transmeta as memory technology analyst. Most recently he has entered the memory modules world through management positions at Netlist, SimpleTech, and US Modular driving unique memory module configurations.

Mr. Gervasi is credited with successfully introducing 4 rank and DDR3 registered DIMMs into the JEDEC standardization process. He has served on the JEDEC Board of Directors and chaired committees for DRAM parametrics and small form factor memory modules throughout the development of DDR1, DDR2, and DDR3. As a chairman of the JEDEC standards organization, he has had a role in paving the memory industry roadmap, and contributed to spreading these standards to the world including engagement with foreign governments. Bill is a public speaker in this niche, generating both excitement and controversy with his aggressive vision for change and progress. Mr. Gervasi holds numerous patents in memory and packaging design, and has performed expert witness testimony in major patent cases.

Bill Gervasi speaks often at technology trade events and offers training for memory technology. He offers computer memory design, marketing, and analysis services through his company, "Discobolus Designs," and is the author of Nerd Story a humorous personal history of the computer revolution, available online (ISBN 978-1-4524-4622-6). Find out more at http://www.discobolusdesigns.com

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Date: **Tuesday, April 30, 2013**

Location: **Broadcom Corporation, 5300 California Ave., Irvine, CA 92617 – Bldg. 2 Conf. Room 2-1037 Salt Creek**
Check in at the Security Gate and proceed to Bldg. 2. You will be escorted into the building.

Time: **5:00-5:30pm: Social time, 5:30-7:00pm: Presentation, 7:00pm: Dinner**

RSVP: **IEEE members and non-members all are welcome to attend. Please RSVP at** http://tinyurl.com/cvl8ez7. Please be at the Bldg. 2 entrance by 5:30 pm; no escorts after that. For questions regarding RSVP, please contact Cristina Nicoara (cnicoara@broadcom.com).

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