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IEEE Components, Packaging and Manufacturing Technology Society – OC Chapter

Thursday, August 29, 2013 Technical Meeting

Wafer Bonding Enables New Technologies and Applications for 3D-IC

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Abstract

3D packaging saves considerable space and increases device speeds by stacking the devices in a single package for power reduction and performance improvement. Whether this bonding process for the stacked chips are activated by temperature, plasma, or chemicals, the technology of wafer bonding is unifying different materials to create new devices and micro components that cannot be fabricated using silicon alone. Wafer bonding is fueling silicon-on-insulator (SOI), MEMS, MOEMS, and 3D-IC packaging.

Biography

Mr. Mark Franklin joined Teikoku Taping Systems in 2011 as Vice President and Chief Technologist responsible for advanced technical roadmap development. Mr. Franklin received his B.S.E.E. from Templeton University and holds eight patents in plasma etch, MEMS processing methods and wafer bonding. Mr. Franklin has served in engineering positions at Texas Instruments machine science and Technology Center, LSI Logics Top secret government contract facility, Silicon Genesis where lead a team that designed the surface activation source now used by EV Group and at Suss MicroTec.

Date:	**Thursday, August 29, 2013**
Location:	**Broadcom Corporation, 5300 California Ave., Irvine, CA 92617 – Bldg. 2 Room 2-1037 Salt Creek** Check in at the Security Gate and proceed to Bldg. 2. You will be escorted into the building.
Time:	**5:30-6:00pm: Social time, 6:00-7:00pm: Presentation, 7:00pm: Dinner (free for attendees!)**
RSVP:	**IEEE members and non-members all are welcome. Please RSVP at http://tinyurl.com/nupuou6** Please be at the Bldg. 2 entrance by 6:00 pm; no escorts after that. For questions regarding RSVP, please contact Cristina Nicoara (cnicoara@broadcom.com).

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