IEEE Components, Packaging and Manufacturing Technology Society – OC Chapter

Thursday, September 12, 2013 Technical Meeting

Integrated Circuit ESD/Latch-up Mechanisms and Testing

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Abstract

Design engineers are increasingly being challenged to reduce the incidence of latch-up. At the same time, this task is made more difficult as devices become more complex and process technologies continue to shrink. The JEDEC latch-up spec is also constantly evolving. In this presentation, attendees will learn:

- An overview of latch-up test and spec
- Test guidelines, techniques, and best practices
- Why latch-up is challenging
- What's coming in JESD78E

Biography

Mr. Barry Fernelius is the manager of the ESD and latch-up labs at Evans Analytical Group. He has been working in the semiconductor industry since 1981, and he's been involved with the JEDEC ESD and latch-up specs for more than twenty years. He's also been a fab engineer for Hewlett-Packard and a senior reliability engineer for Agilent and Avago.

Date: **Thursday, September 12, 2013**

Location: **Broadcom Corporation, 5300 California Ave., Irvine, CA 92617 – Bldg. 2 Room 2-1034 Trestles**
Check in at the Security Gate and proceed to Bldg. 2. You will be escorted into the building.

Time: **5:30-6:00pm: Social time, 6:00-7:00pm: Presentation, 7:00pm: Dinner (free for attendees!)**

RSVP: **IEEE members and non-members all are welcome. Please RSVP at http://tinyurl.com/ohang2c**
Please be at the Bldg. 2 entrance by 6:00 pm; no escorts after that. For questions regarding RSVP, please contact Cristina Nicoara (cnicoara@broadcom.com).

For more information please contact the following officers of the IEEE CPMT OC Chapter:

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