Micro-Transfer-Printing (µTP): Technology Overview

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IEEE CPMT Orange County Chapter Meeting

Irvine, CA

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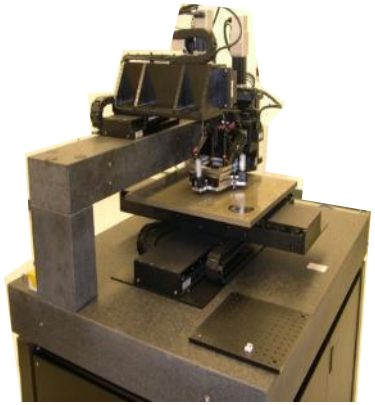
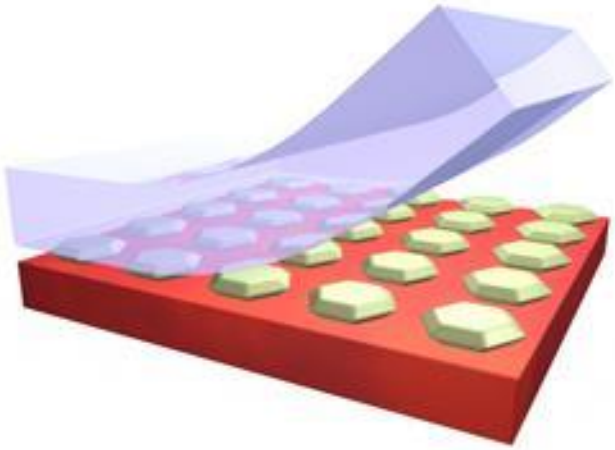
Outline

- Micro-Transfer-Printing: Origins & Science
- Micro-Transfer-Printing: Technology
- “Printable” Systems & Applications

“Micro-Transfer-Printing”

- Utilization of a elastomer stamp to deterministically transfer microscale devices from their native substrates onto non-native substrates.





µTP Lineage

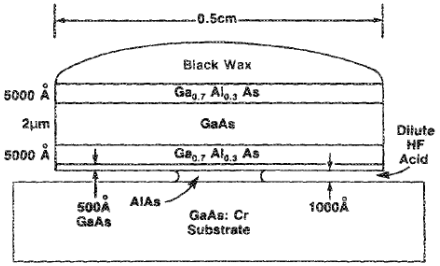
- 2003-2006: Core technology invented by Professor John Rogers group at UIUC.

- 2006: Semprius spins-out of UIUC to commercialize transfer-printing.
- 2011: Semprius focuses on the manufacture of high-concentration photovoltaics (HCPV)

- 2013: X-Celeprint acquires the exclusive rights to Micro-Transfer-Printing. Semprius retains rights for photovoltaics.
- X-Celeprint is the sole developer and licensor of Micro-Transfer-Printing technology and will support end-users with application-specific process development, technology-transfer and hardware.
- Headquarters: Tyndall National Institute, Cork, Ireland

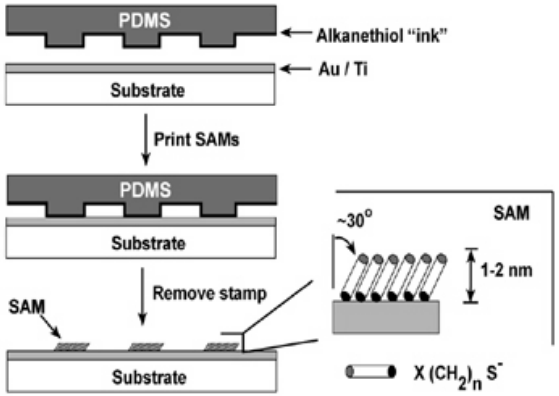
Origins of µTP Technology

Epitaxial Lift-off (ELO)
Yablonovitch 1987

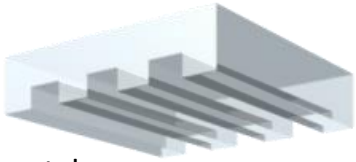


"Soft lithography" for large-area, flexible devices using low-temperature (organic) semiconductor materials

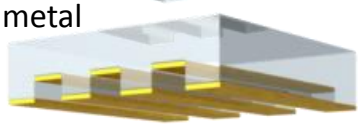
Micro-contact printing



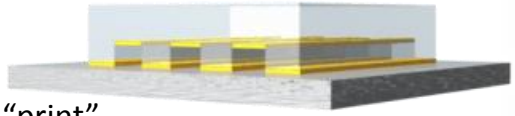
i. stamp



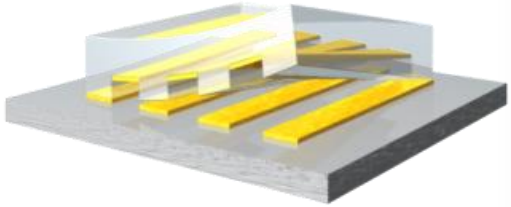
ii. apply metal

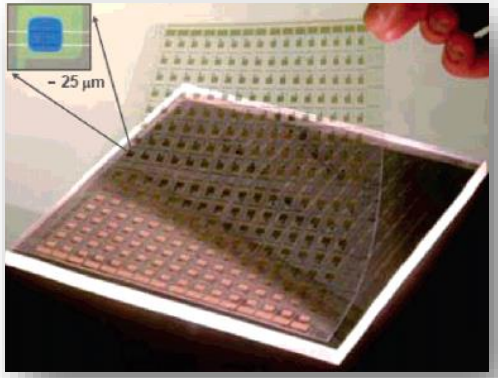


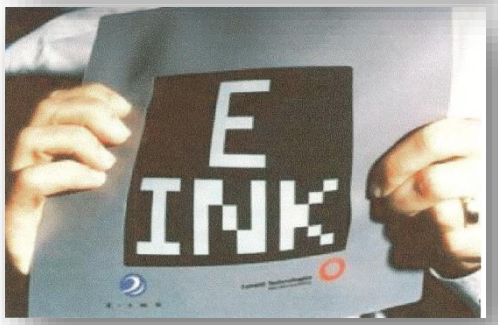
iii. contact



iv. "print"



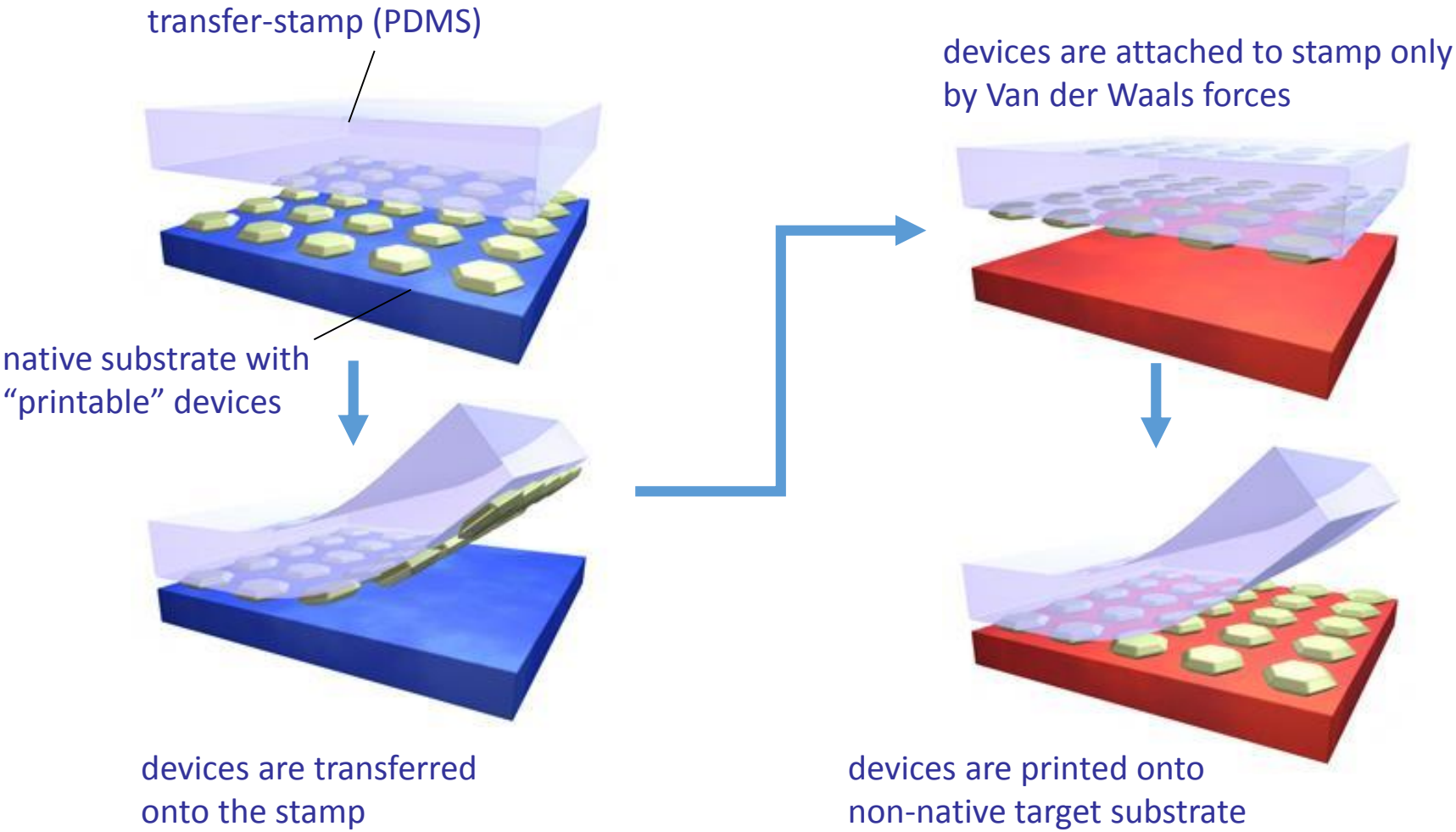




X-Celeprint

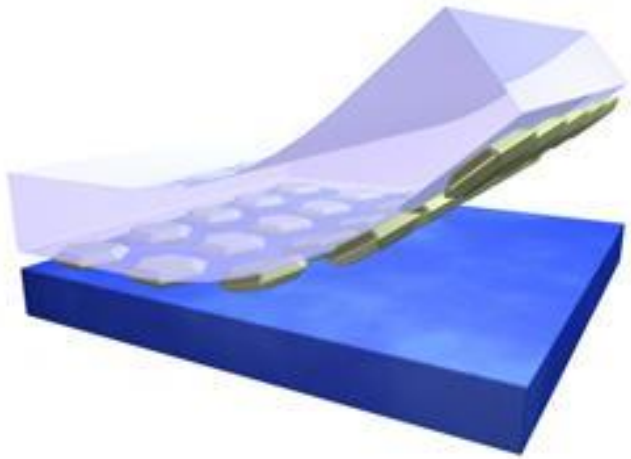
ELO, "soft lithography" and MEMS are all precursors

Micro-Transfer-Printing

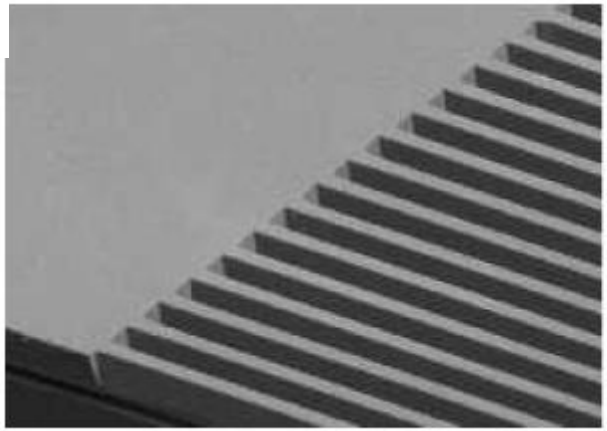


Nature Mater. **5** 33-38 (2006)

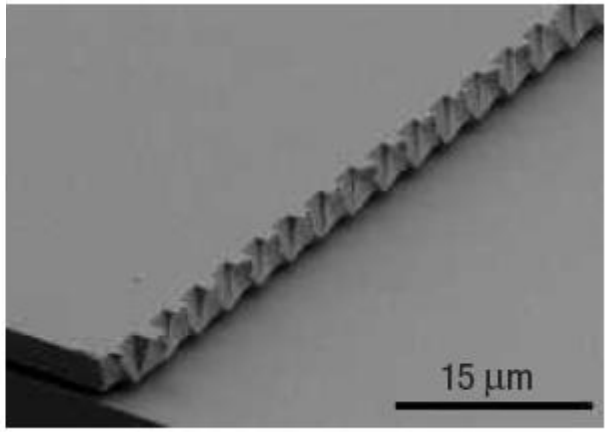
Kinetically Controlled Adhesion



"The adhesion between the solid objects and the stamp is rate-sensitive owing to the viscoelastic behavior of the elastomer"



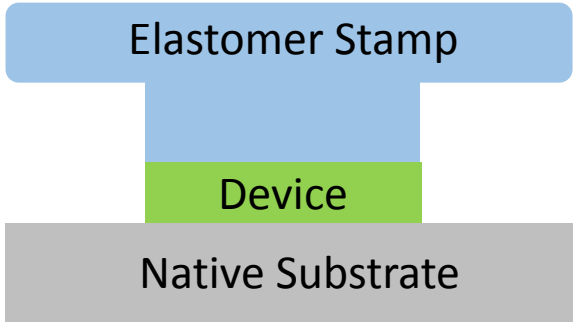
slow lift-off

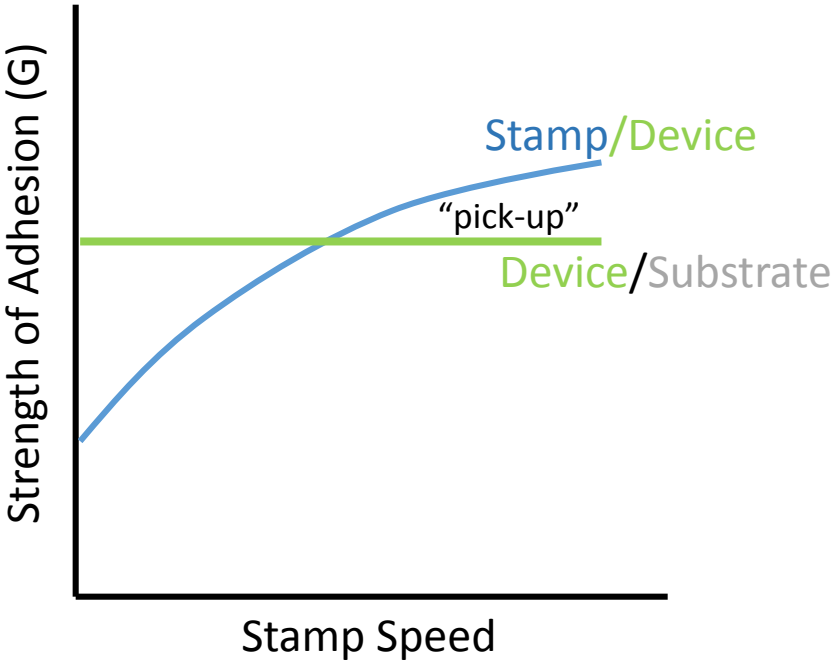


fast lift-off
> 10 cm s^{-1}

Nature Mater. **5** 33-38 (2006)

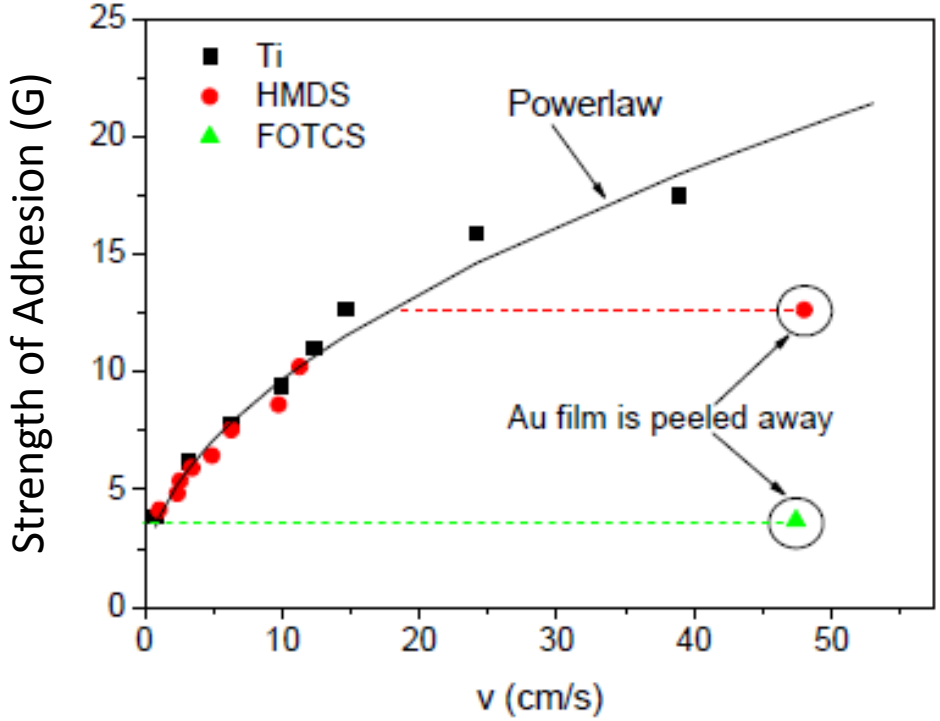
Competing Adhesion ("pick-up")





- During "pick-up", the stamp must move at high speed to take advantage of the strong stamp-device adhesion

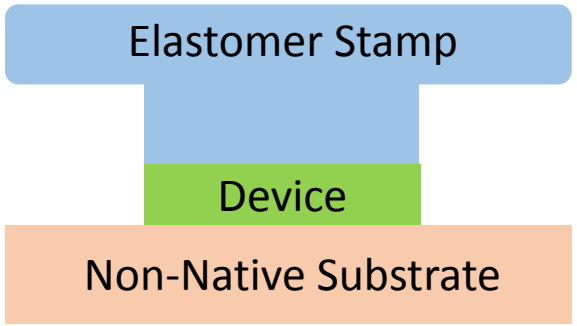
Example: “picking-up” evaporated Au

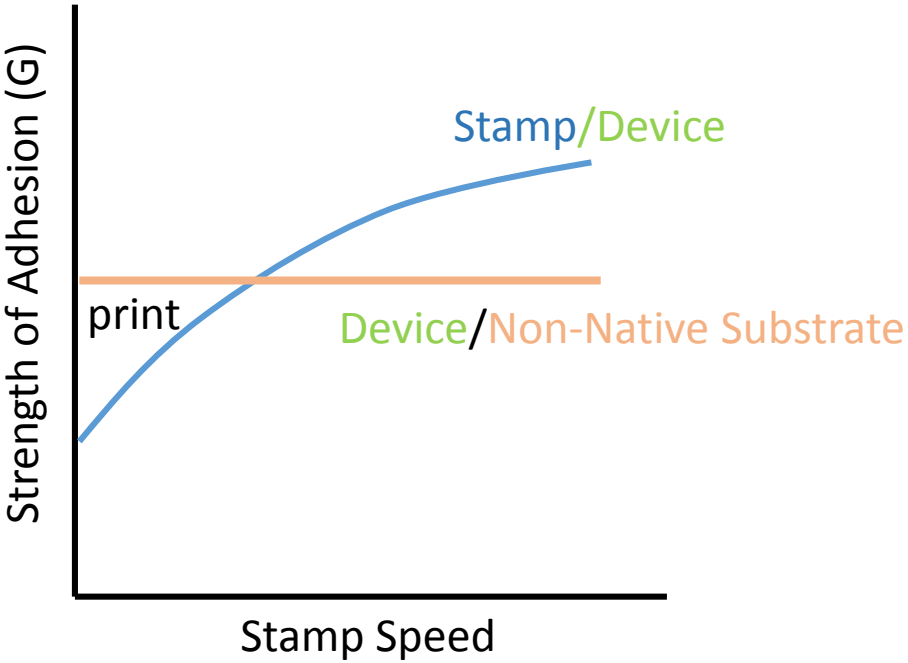


(tridecafluoro-1,1,2,2-tetrahydrooctyl) trichlorosilane (FOTCS)

Langmuir, Vol. 23, No. 25, 2007

Competing Adhesion ("print")

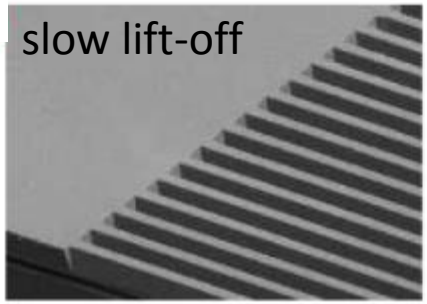


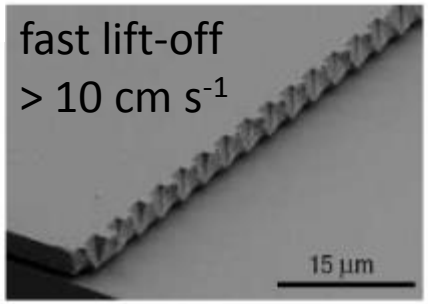


- Stamp must move slowly to utilize weak bonding between the stamp and device

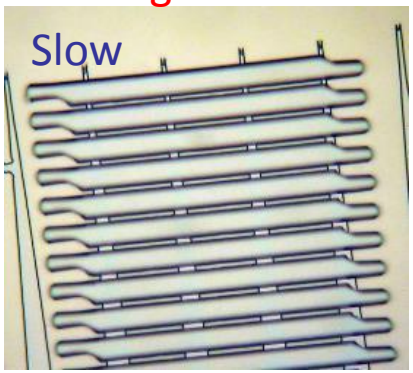
Example: Single-Crystal Silicon Beams

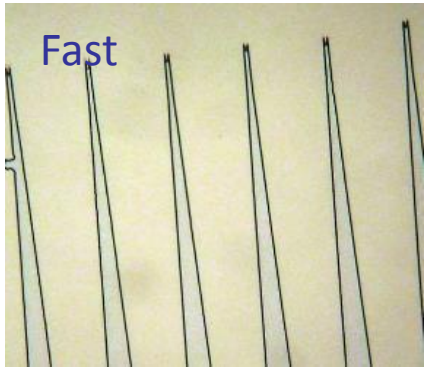
Pick-up

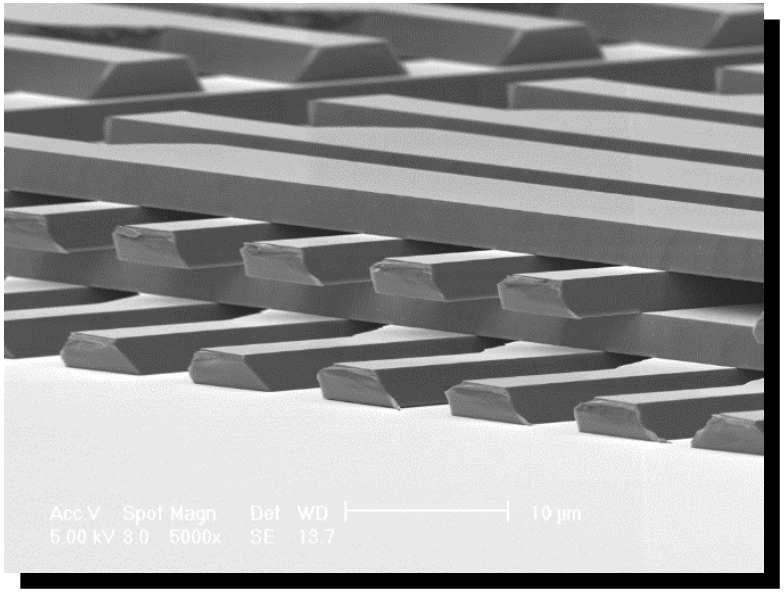




Printing





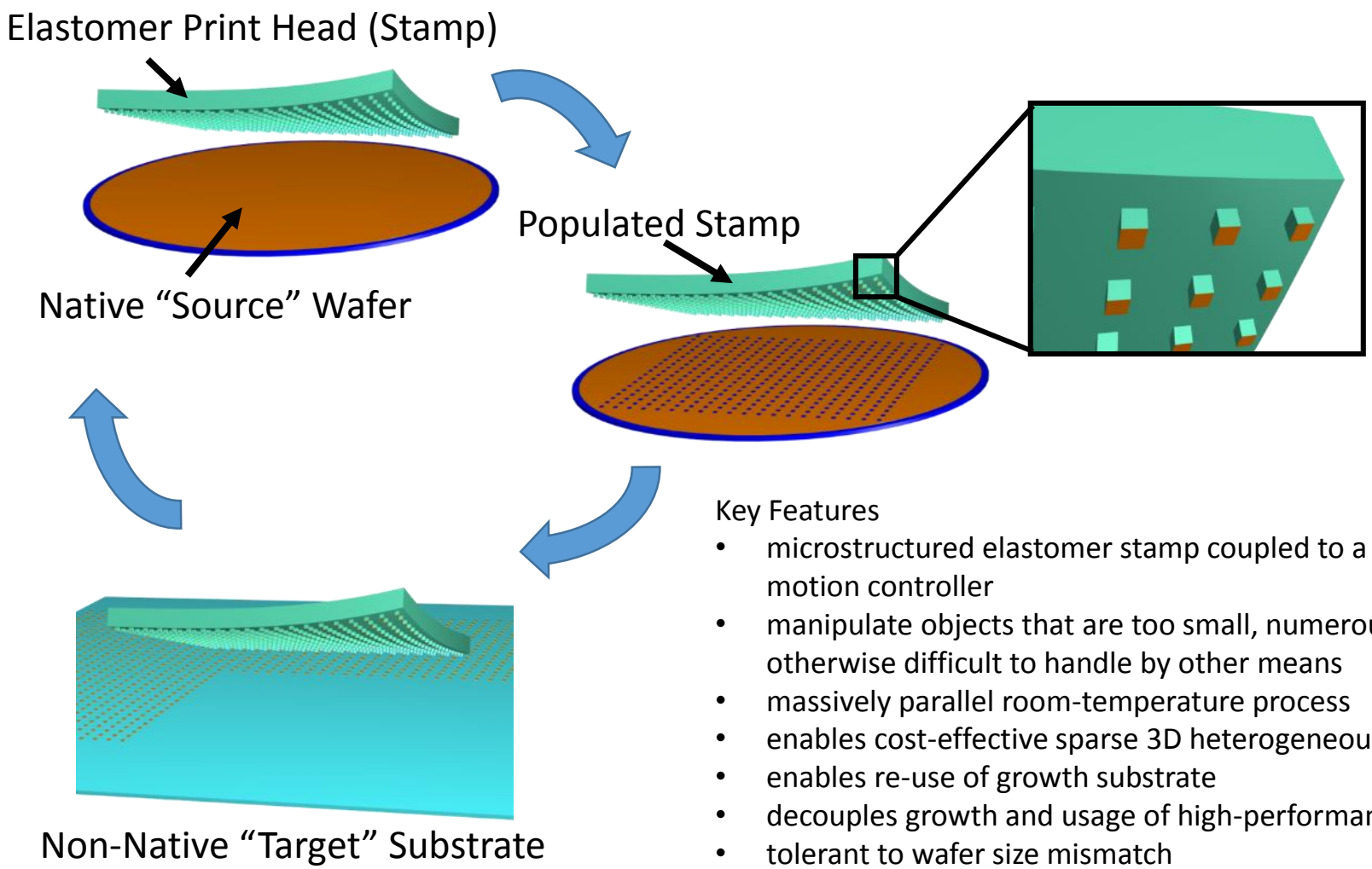


Nature Mater. **5** 33-38 (2006)

Outline

- Micro-Transfer-Printing: Origins & Science
- Micro-Transfer-Printing: Technology
- “Printable” Systems & Applications

Micro-Transfer-Printing Technology



Key Features

- microstructured elastomer stamp coupled to a precision motion controller
- manipulate objects that are too small, numerous, fragile, or otherwise difficult to handle by other means
- massively parallel room-temperature process
- enables cost-effective sparse 3D heterogeneous integration
- enables re-use of growth substrate
- decouples growth and usage of high-performance materials
- tolerant to wafer size mismatch
- placement accuracy* +/- 1.5 µm (3-sigma)
- process yields* > 99%

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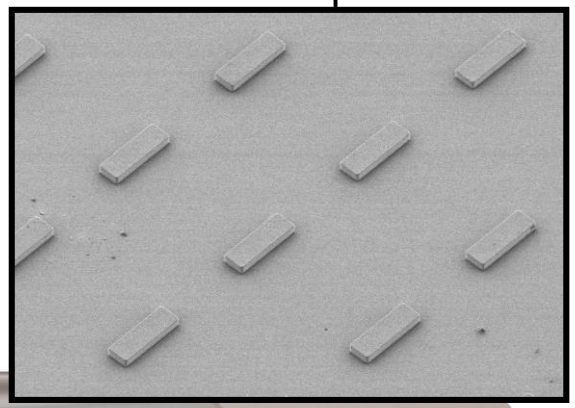
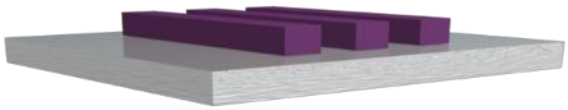
* application dependent

Stamp Technology

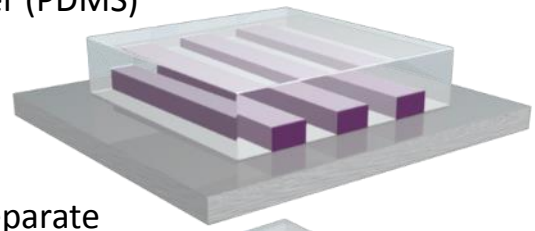
SEM of stamp surface



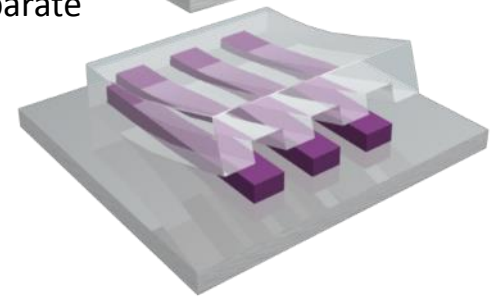
i. Prepare master, e.g. by photolithography

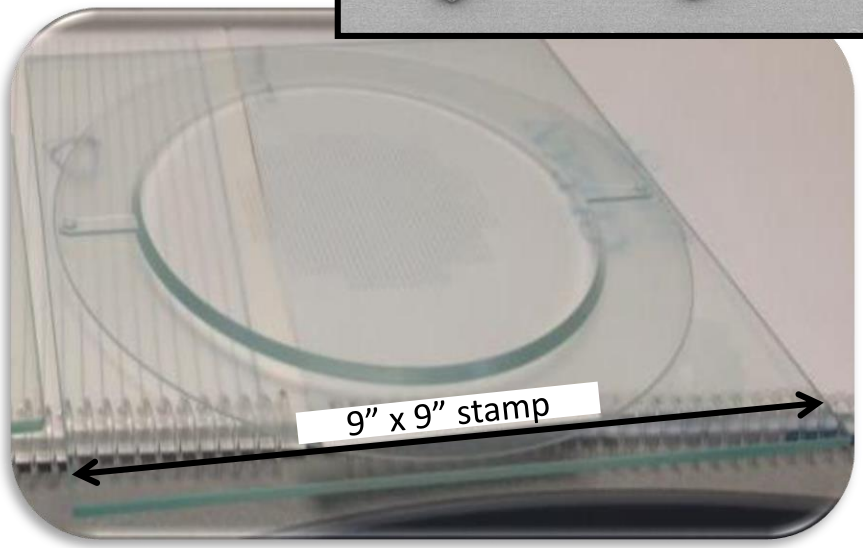


ii. Cast prepolymer (PDMS)



iii. Cure stamp; separate from master

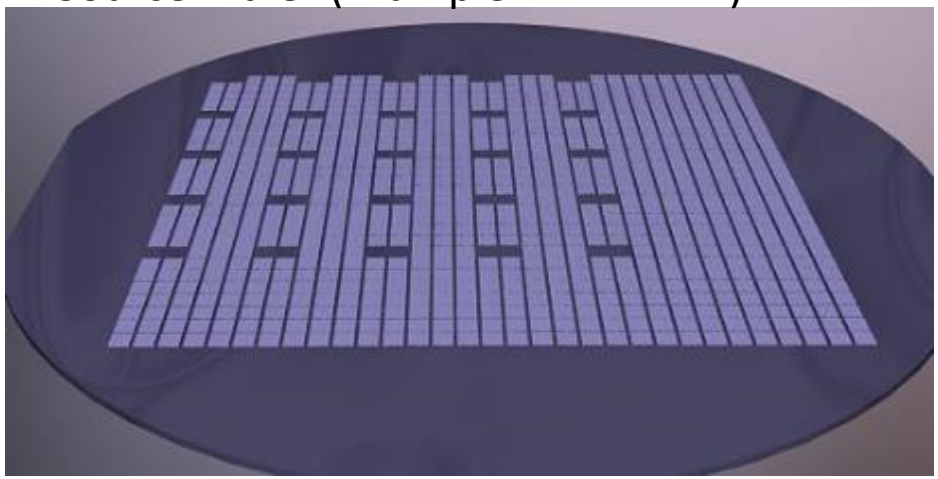




- Stamps are fabricated by casting PDMS against a microfabricated master wafer.
- Stamps as large as 150mm (active area) have been developed.

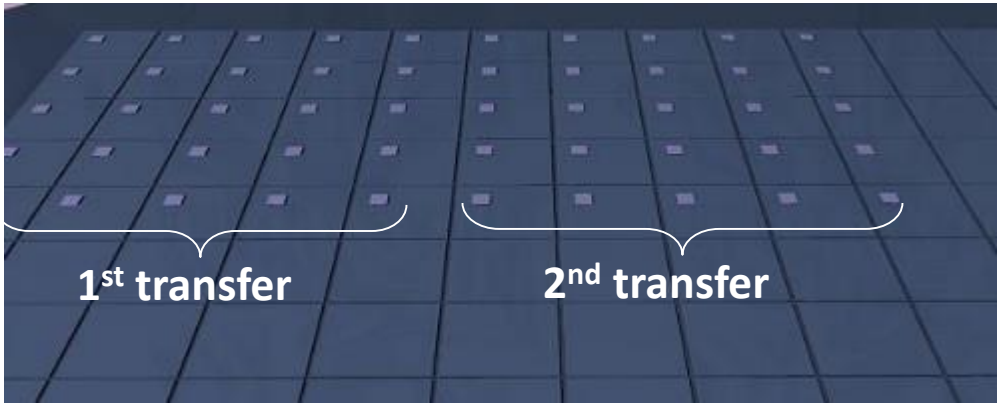
Sparse Heterogeneous Integration

Source Wafer (Example → InP HBT)



→ produce devices at high density on native growth substrate
→ use small devices only where needed in the target application

Non-native "Target" Substrate



"Area Magnification"

- With µTP, the source of the high-performance devices (eg. InP HBTs) can be used to fully populate a much larger target substrate.
- For example, a 4" InP wafer might be used to populate a full 200/300mm wafer.

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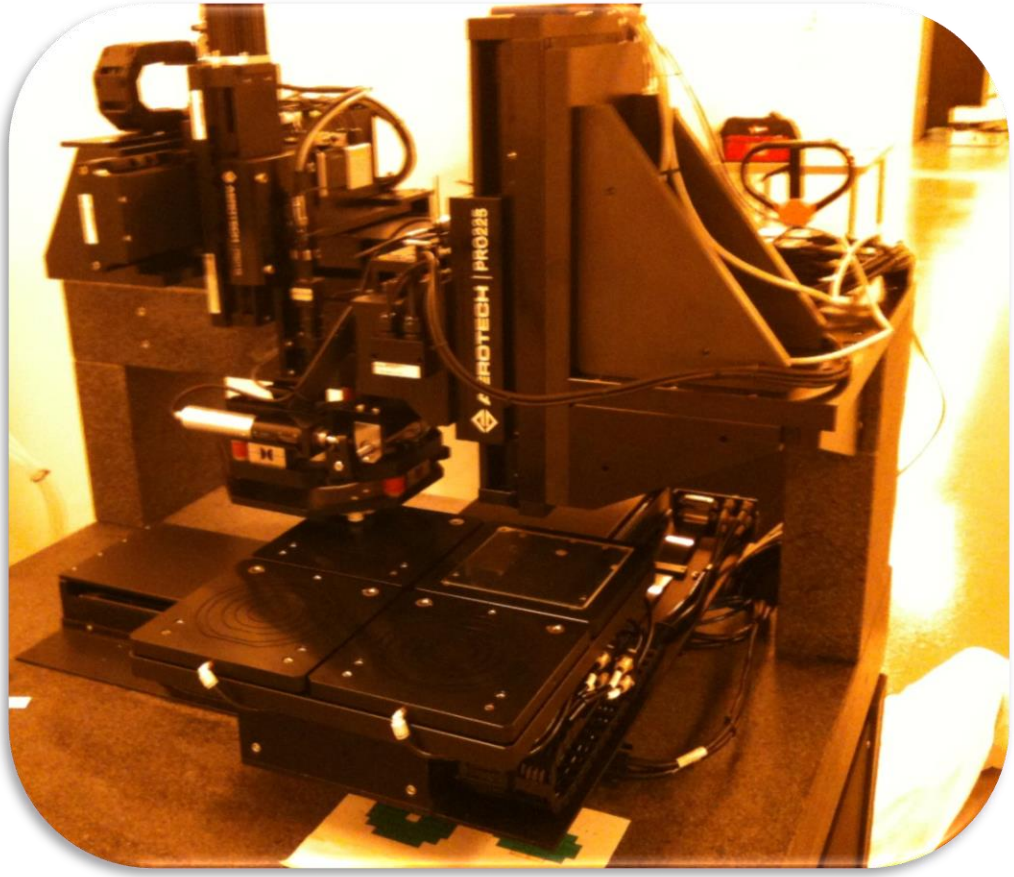
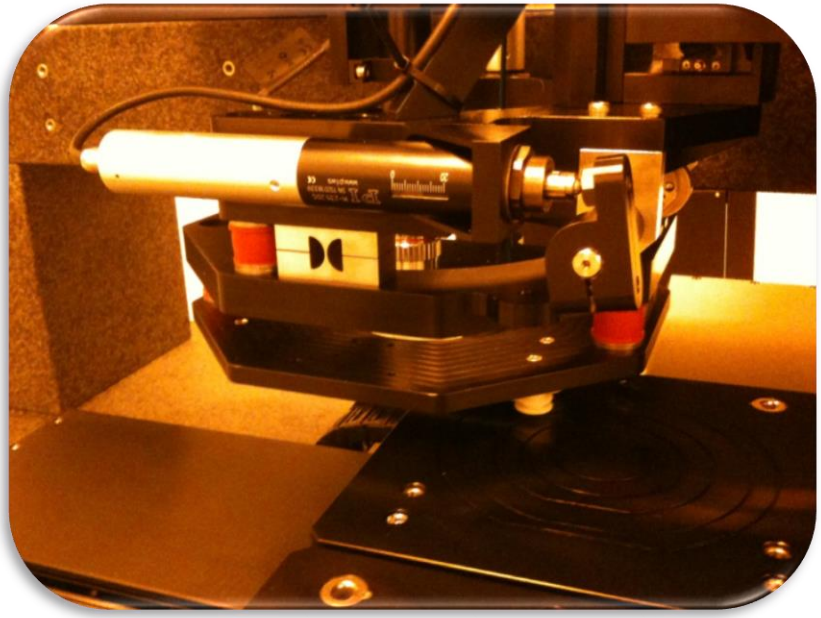
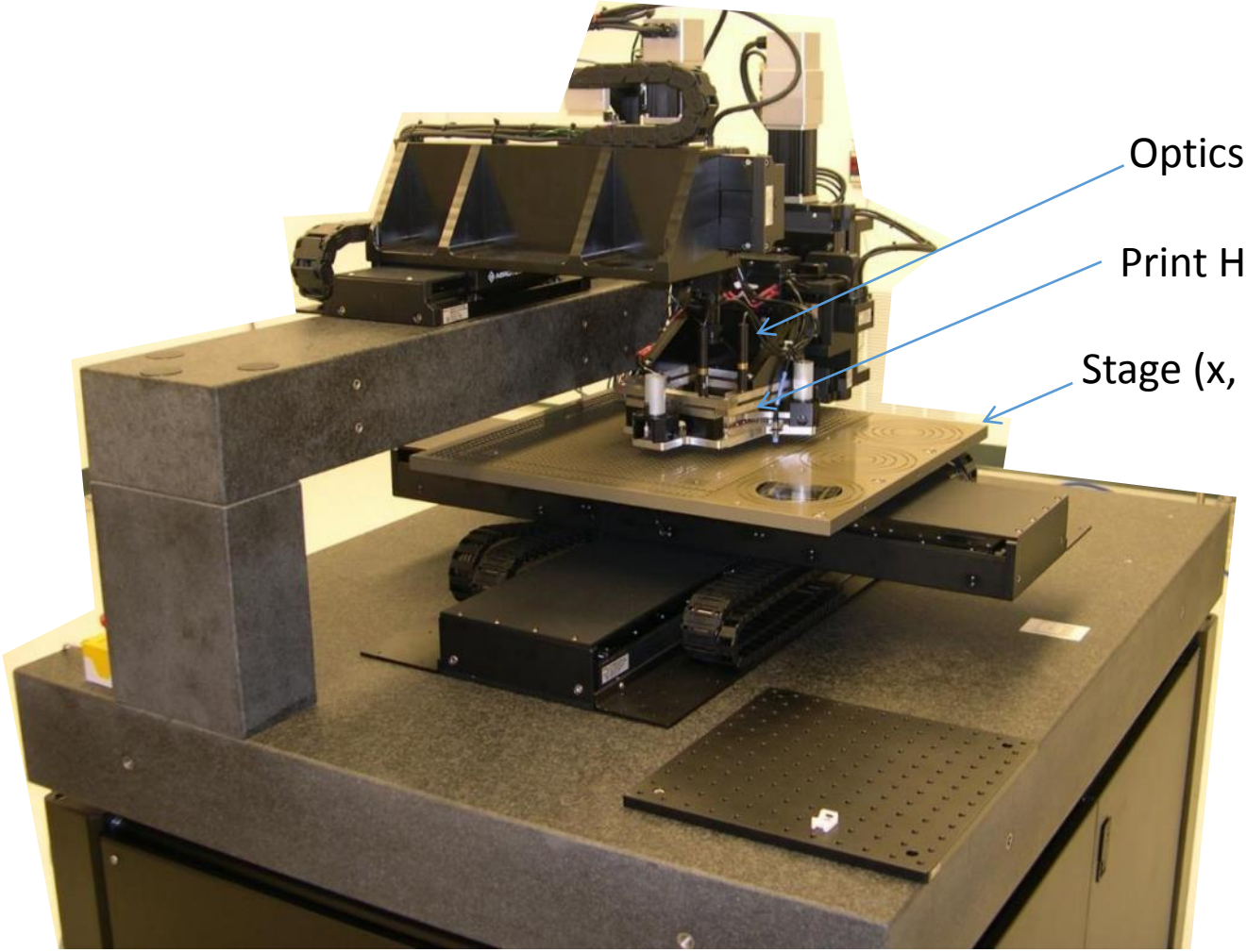
Wafer-to-Wafer µTP Tool





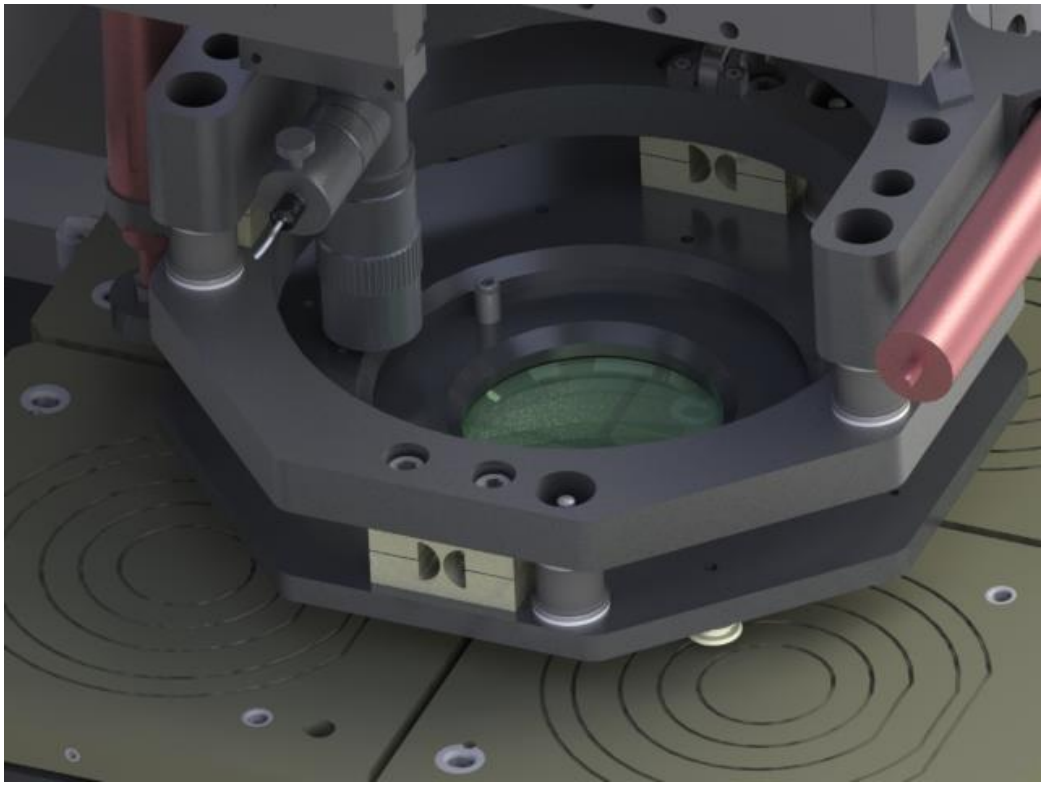
- Designed to populate a 150mm diameter area in one print cycle.
- Process tact time < 30 seconds

Wafer-to-Panel µTP Tool

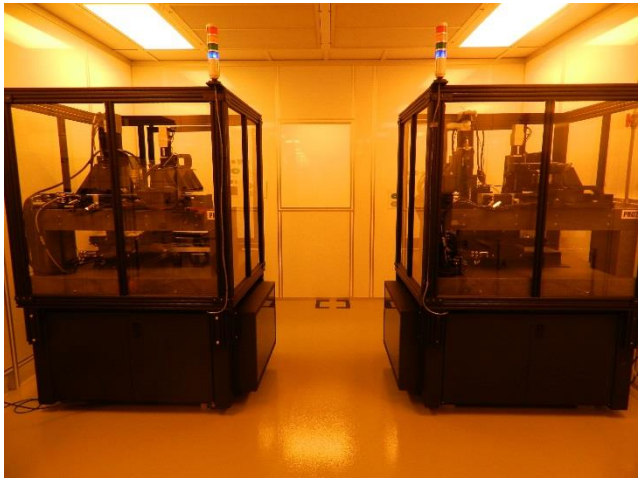


- Designed to populate Gen2+ (400mm x 500mm) glass and plastic panels

µTP Hardware



Production W2W Printers at Semprius CPV Pilot Plant in Henderson, NC.



- X-Celeprint will design, manufacture and support µTP hardware.
- The print tools can be customized for specific applications.

X-Celeprint Operations

X-Celeprint Headquarters
100mm III-V cleanroom
Experts in photonics and III-V processing

Not-for-profit Research Institute
Research Triangle Park, North Carolina
4”, 6”, 8” and 12” capability
Experts in wafer-bumping and RDL

- X-Celeprint has current µTP and wafer processing capability in North Carolina
- A new µTP tool is scheduled to be installed within Tyndall in Q2

X-FAB

X-Celeprint Headquarters
100mm III-V cleanroom
Experts in photonics and III-V processing

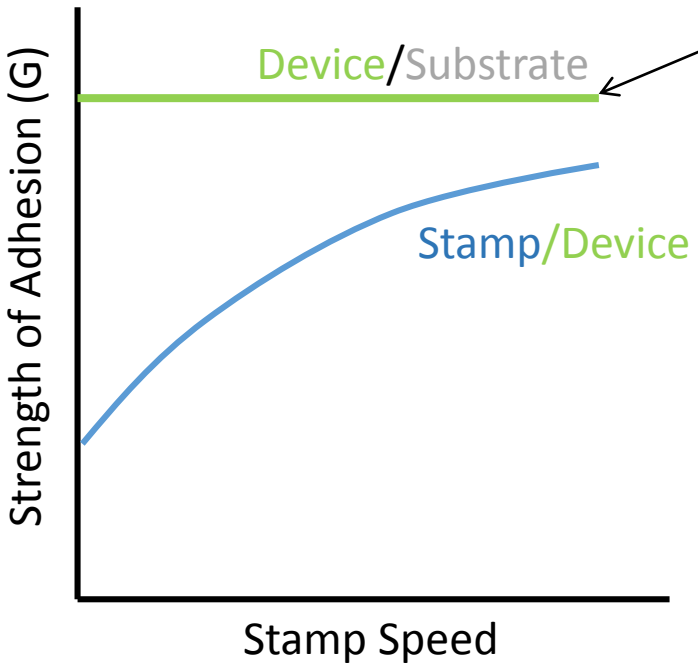
Not-for-profit Research Institute
Research Triangle Park, North Carolina
100mm, 150mm, 200mm and some 300mm
Experts in wafer-bumping and RDL

X-FAB, a sibling company of X-Celeprint, is considering the possibility of a "heterogeneous integration" foundry that would offer Micro-Transfer-Printing and Wafer-Level interconnect processes.

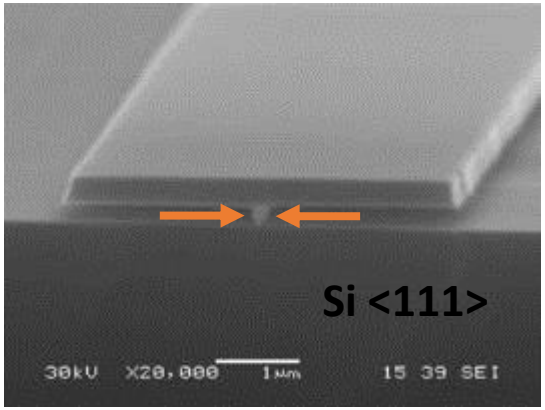
Outline

- Micro-Transfer-Printing: Origins & Science
- Micro-Transfer-Printing: Technology
- “Printable” Systems & Applications
  - Single Crystal Silicon
  - Silicon Integrated Circuits
  - Compound Semiconductors

Printable Systems



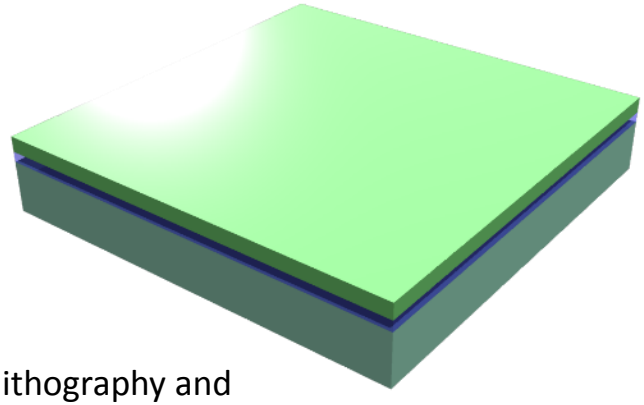
Most materials of interest are challenging to "pick-up" in their as-grown form.



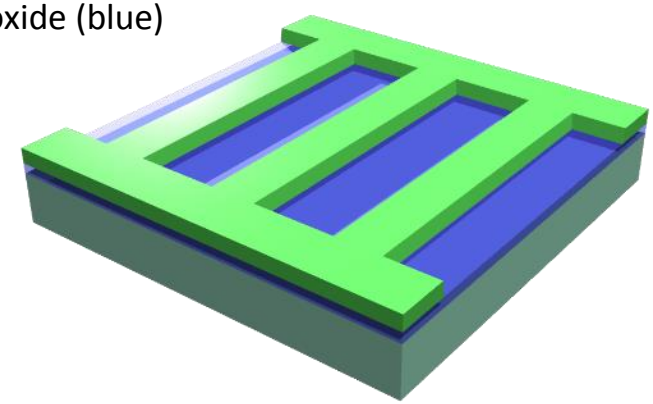
Primary strategy to achieve "pickable" devices is to utilize engineered sacrificial layers underneath the device layers of interest.

Printable Single-Crystal Silicon

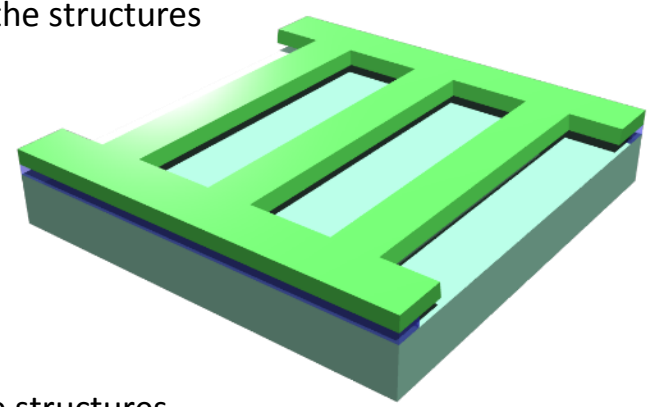
i. Silicon-on-insulator (SOI) wafer



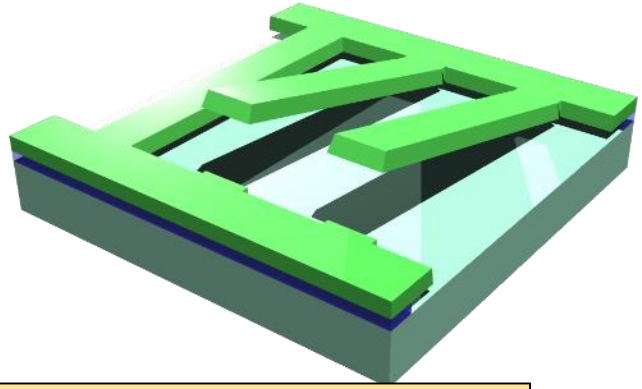
ii. Photolithography and etch top silicon to expose buried oxide (blue)



iii. Etch buried oxide to undercut the structures



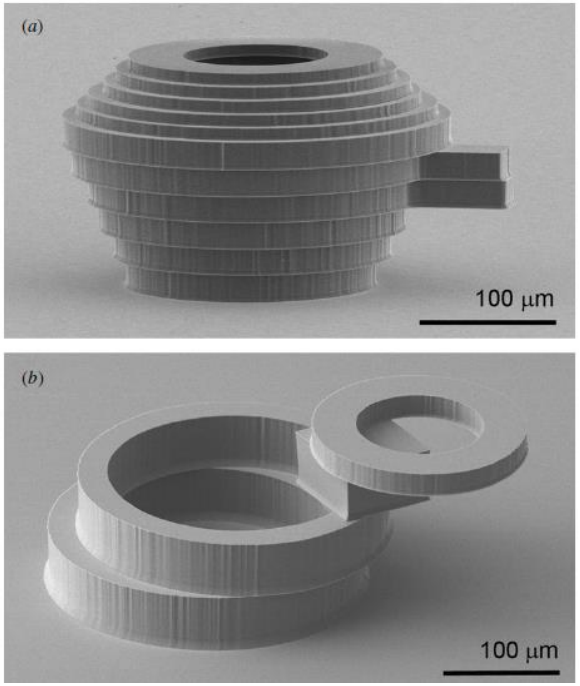
iv. Retrieve structures



Printable single-crystal silicon can be achieved using SOI wafers, where the buried oxide layer serves as the sacrificial layer.

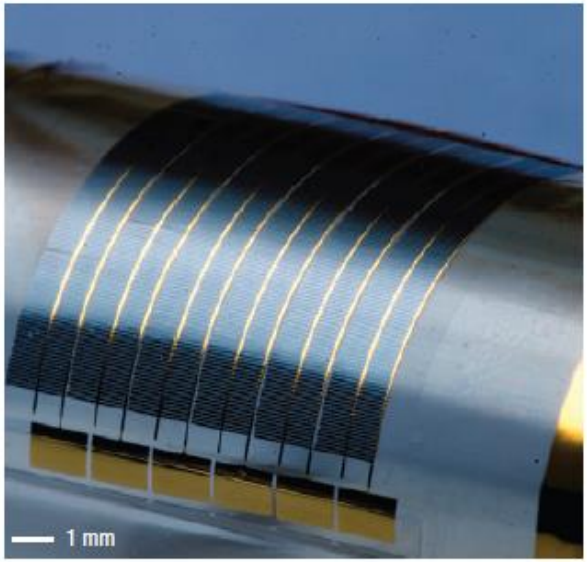
Examples of Printed Silicon

Si Micro Masonry



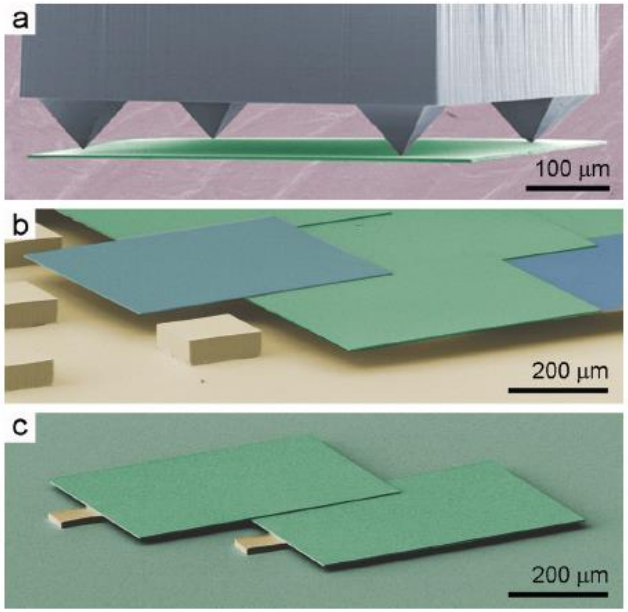
J. Micromech. Microeng. **22** (2012) 055018 (7pp)

Flexible Si Solar Cells



Nature Materials 7, 907-915 (2008).

Imbricate Scales



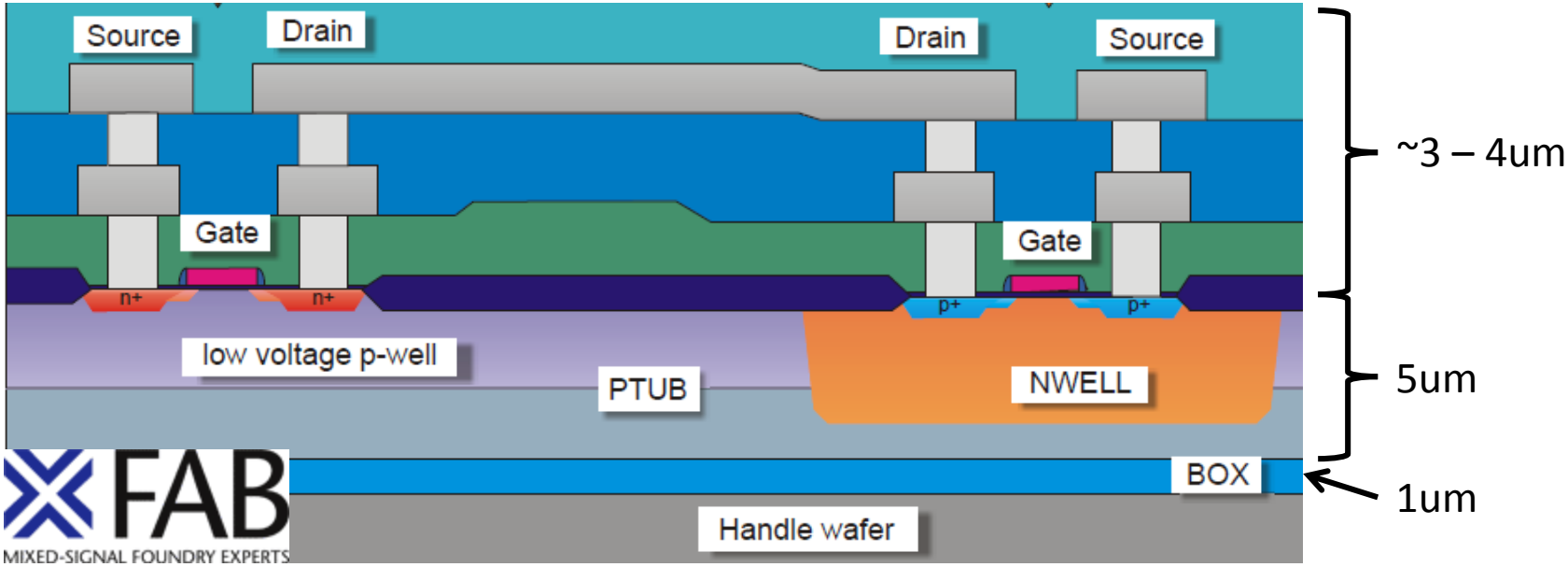
small 2012, *8,* No. 6, 901–906

http://rogers.matse.illinois.edu

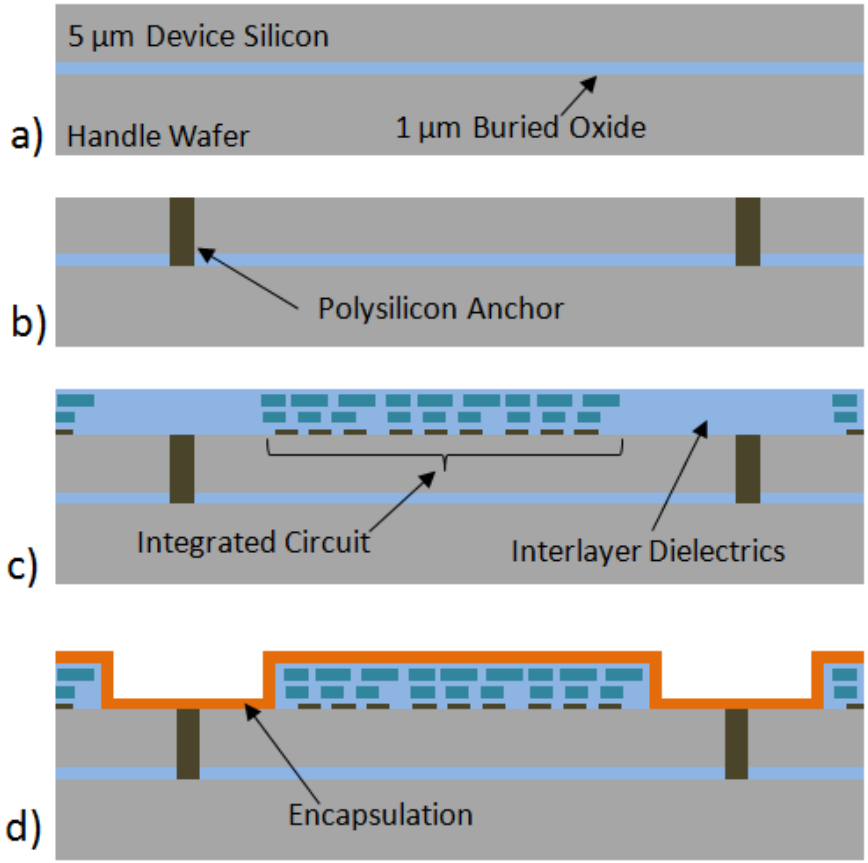
Printable Integrated Circuits

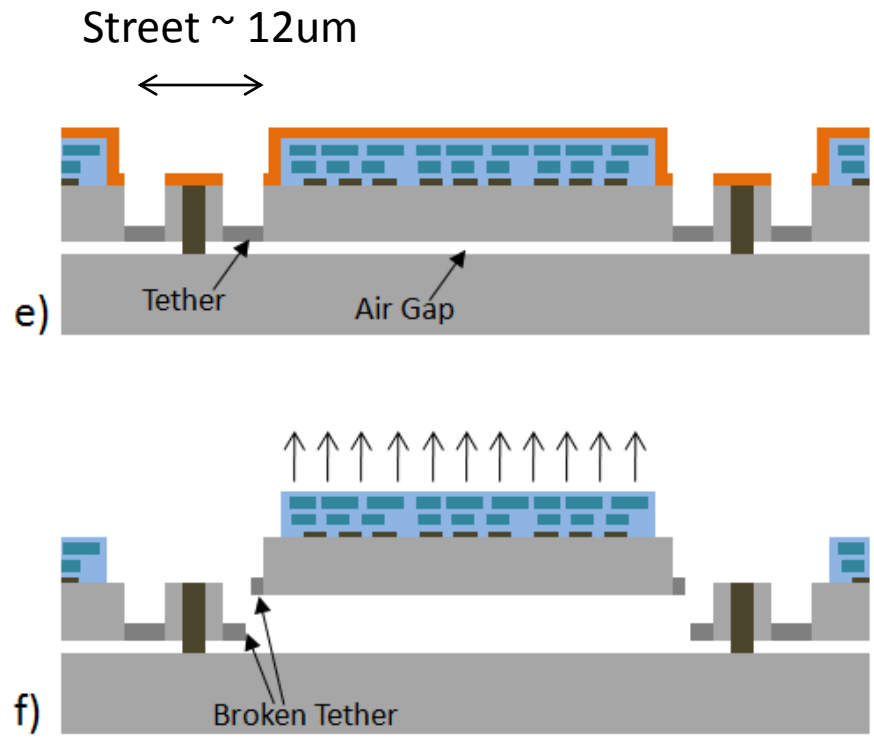
- In 2007 Semprius/XFAB began developing technology for making “printable” integrated circuits
- The platform utilized was the commercially available 0.6um (2P,3M) SOI-CMOS process (XT06) available from XFAB in Erfurt, Germany.
- The XT06 process uses a SOI substrate with a 5um thick device silicon layer and a 1um thick buried oxide (BOx) layer.

XT06 Cross-section



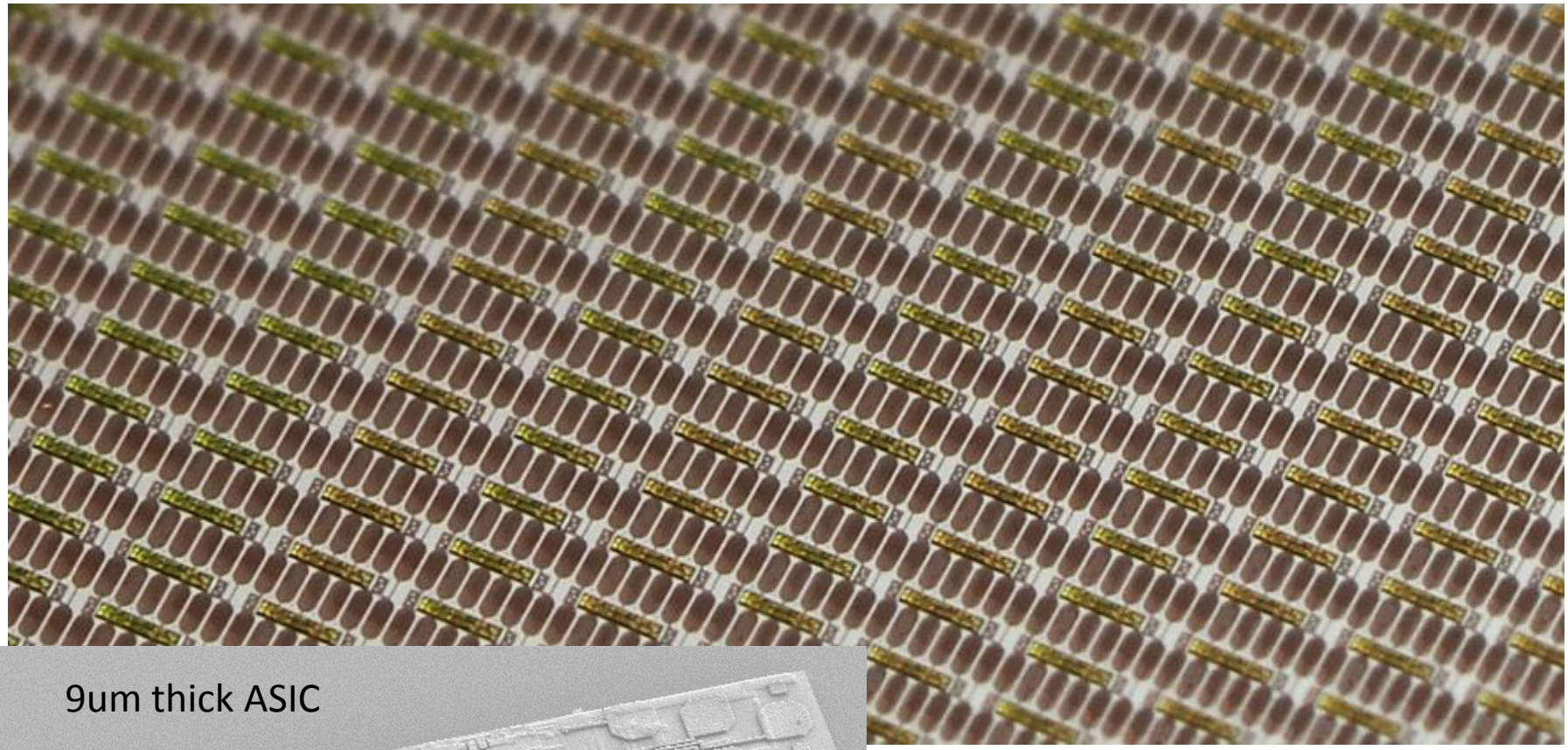
Printable IC Process Flow

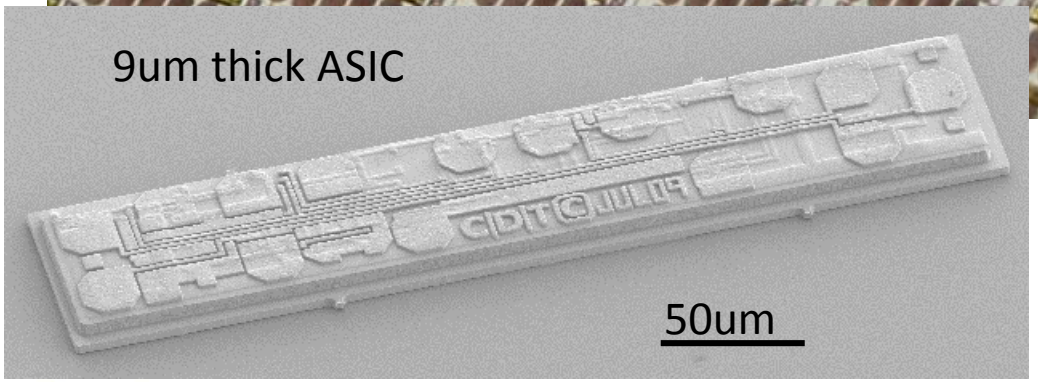




Process for making high-density printable IC chips

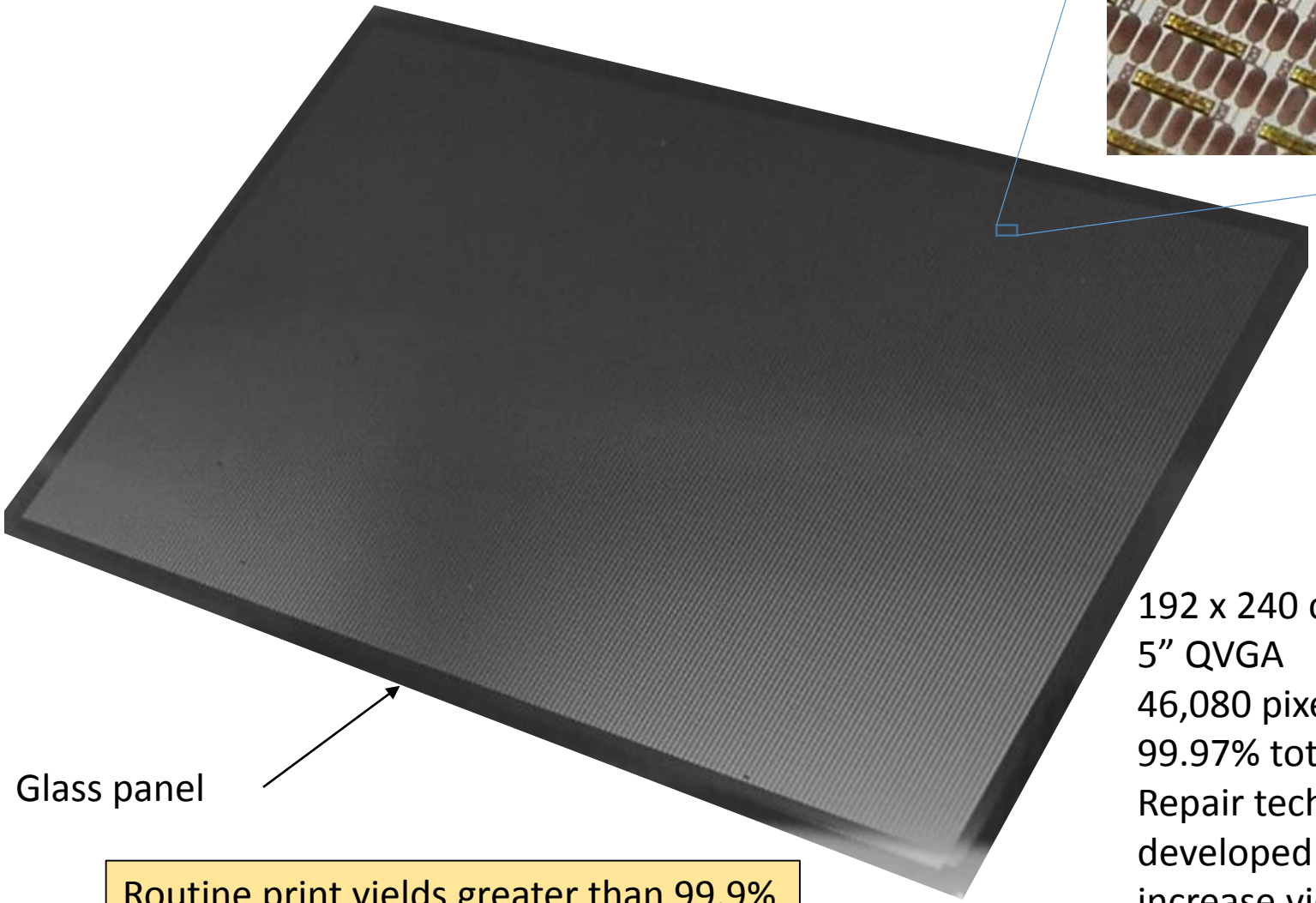
Printed IC Display Backplane

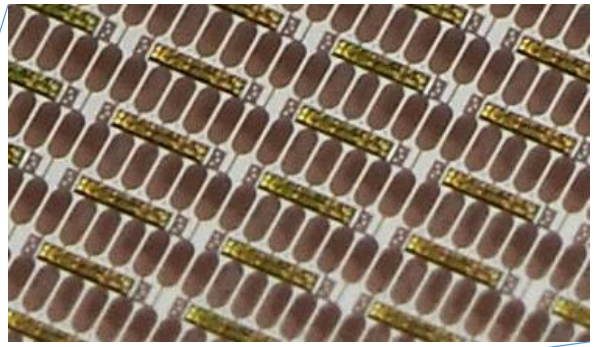




- The pixel driver ASIC has > 250 transistors
- The chip includes both digital and analog circuits

Backplane Printing Yield





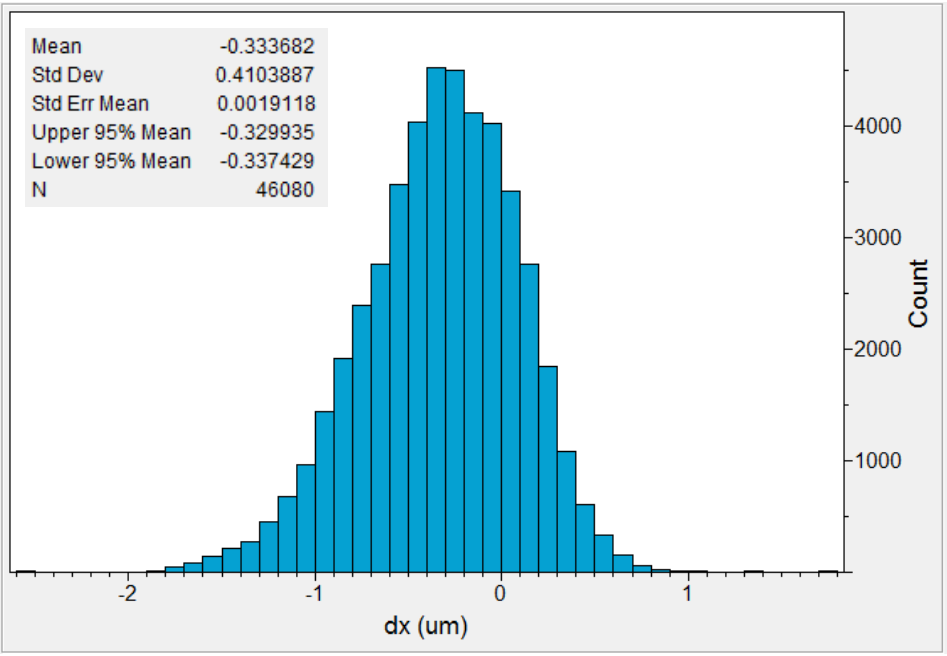
Glass panel

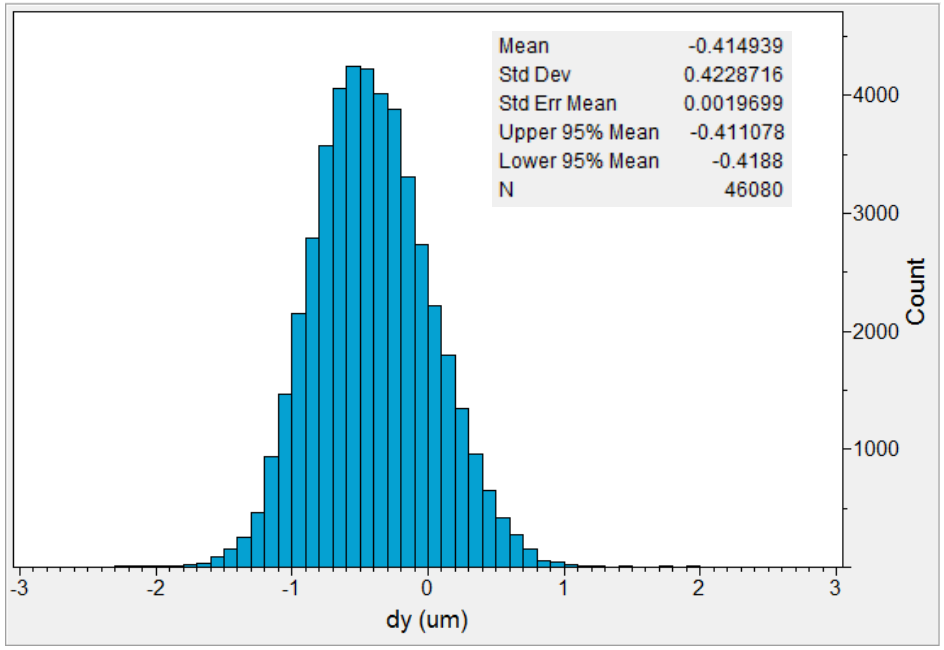
192 x 240 chip array
5” QVGA
46,080 pixel driver ICs
99.97% total yield
Repair techniques have been developed to further increase yield.

Routine print yields greater than 99.9%

X-Celeprint

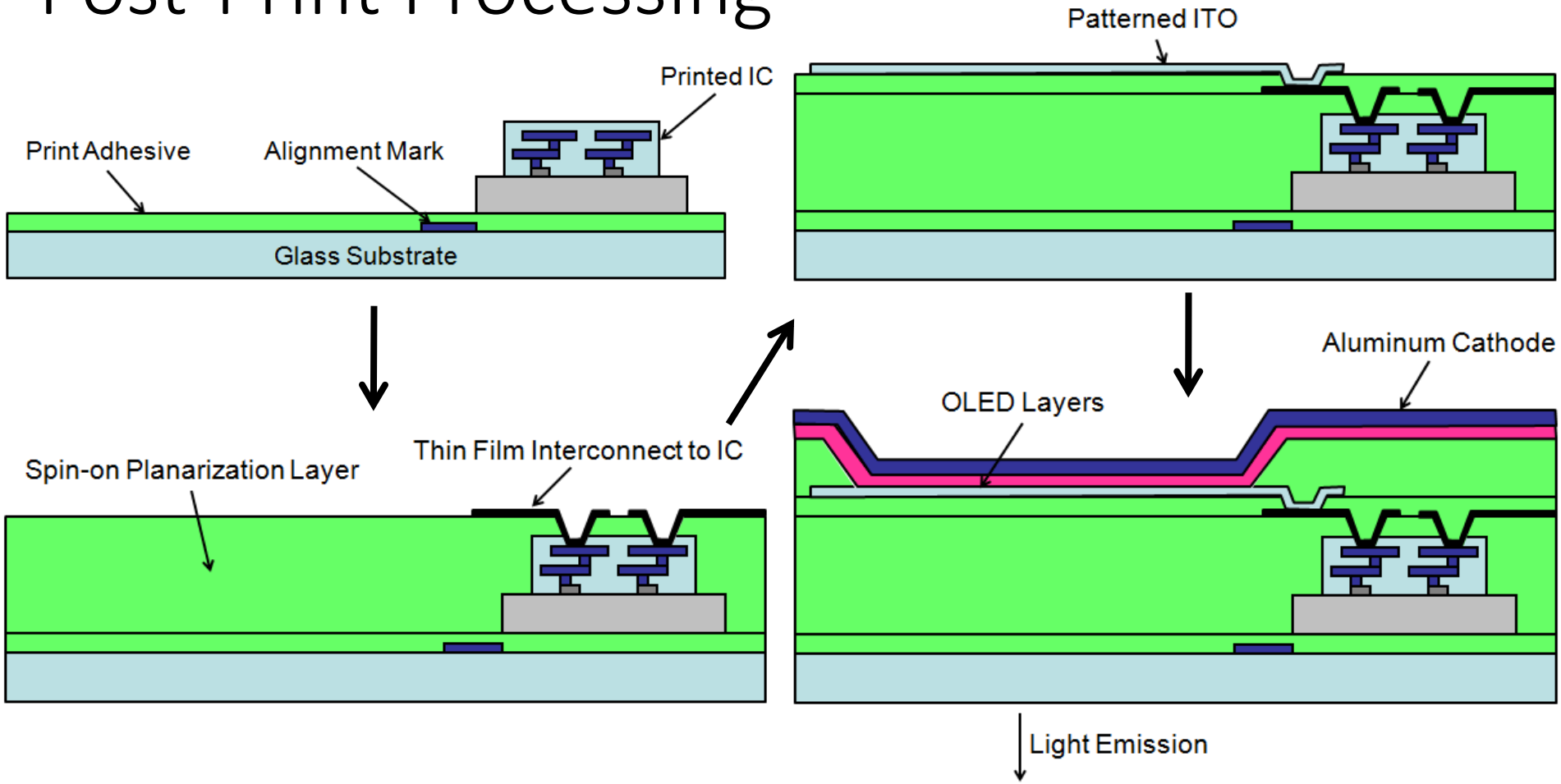
Placement Accuracy





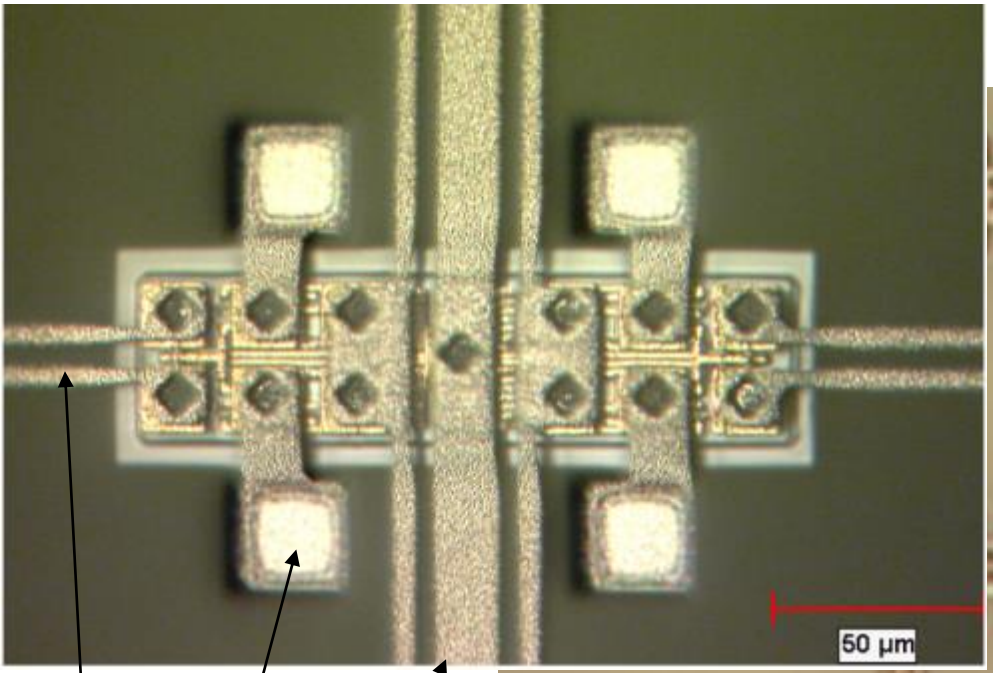
Placement accuracy of printed ASICs was +/- 1.5um (3 sigma)

Post-Print Processing

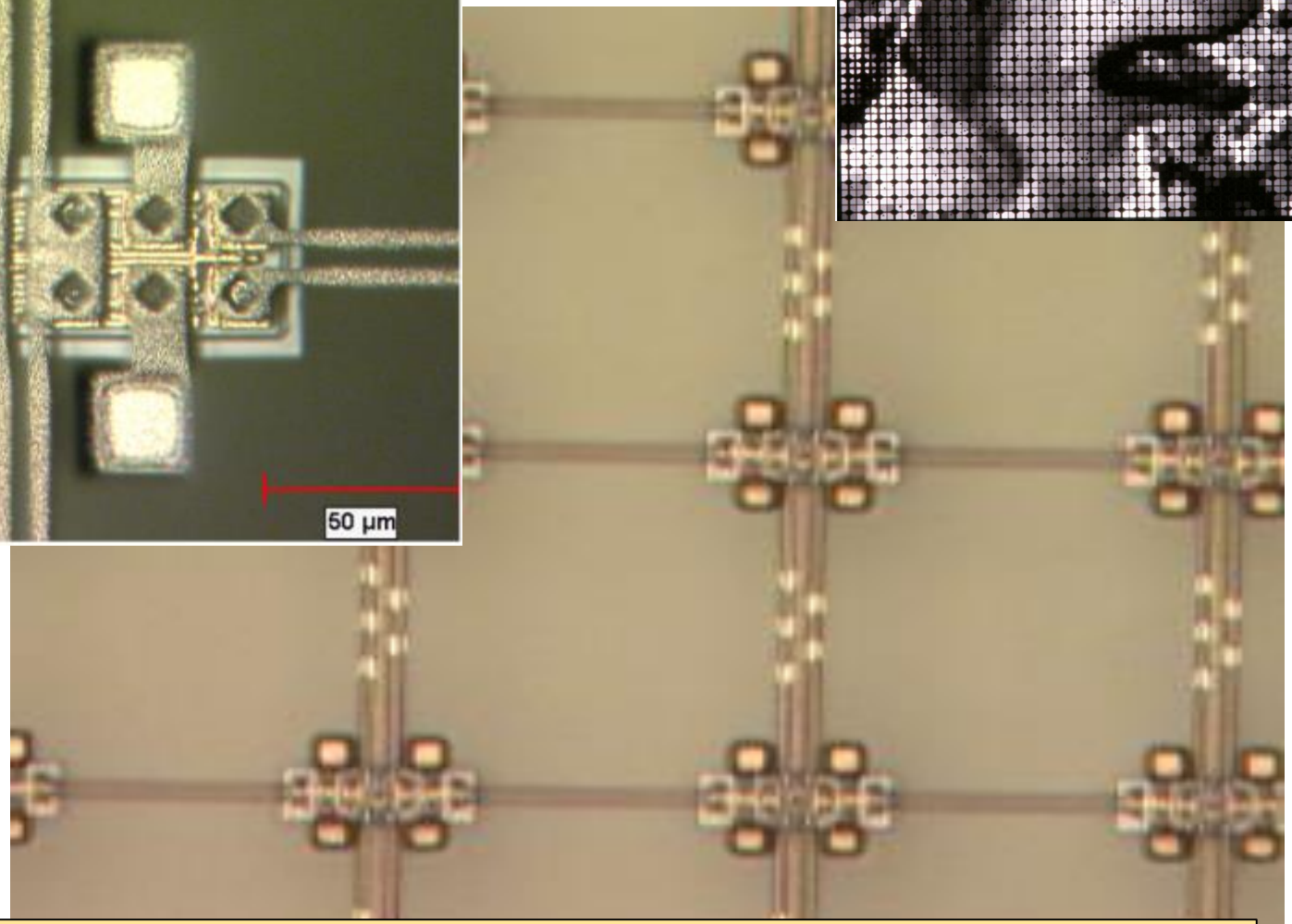


- Once print adhesive is cured the populated substrate can be processed just like any other device substrate (wet processing, photo, dry etching, etc…)
- In this case, the printed ASICs were embedded in a spin-on dielectric before metallization.

Interconnected Backplane



370 um pitch



Anode connection pad

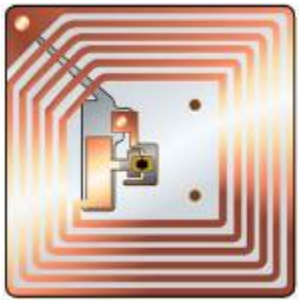
Data wires (2) and Power wire

Row-Select wires (2)

The printed ASICs are thin (~10um), so standard spin-on planarization and thin-film metallization can be used for interconnection

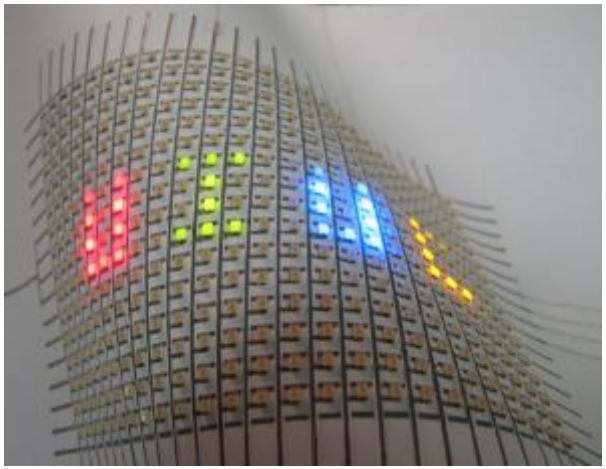
Applications of Printable CMOS

RFID



Smart Cards

Flexible Electronics



Flexible Display Backplanes

Advanced Digital X-ray

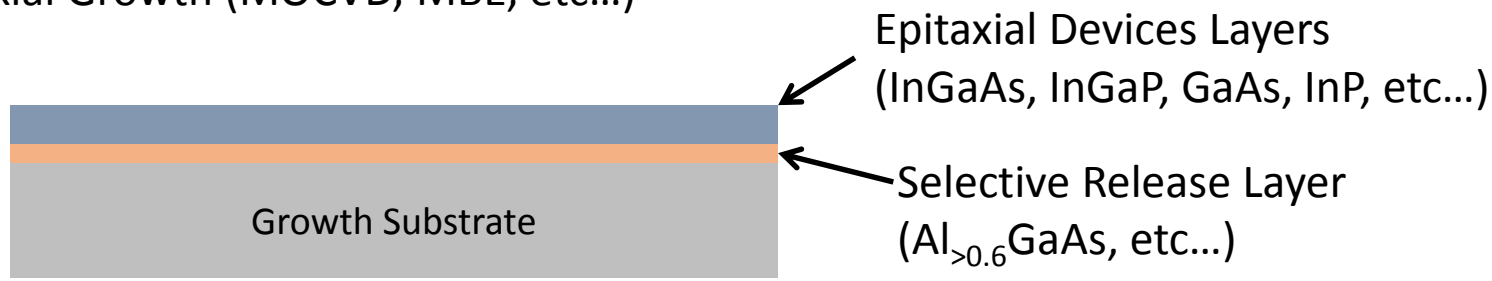
Get CMOS performance on non-native substrates!

Outline

- Micro-Transfer-Printing: Origins & Science
- Micro-Transfer-Printing: Technology
- “Printable” Systems & Applications
  - Single Crystal Silicon
  - Silicon Integrated Circuits
  - Compound Semiconductors

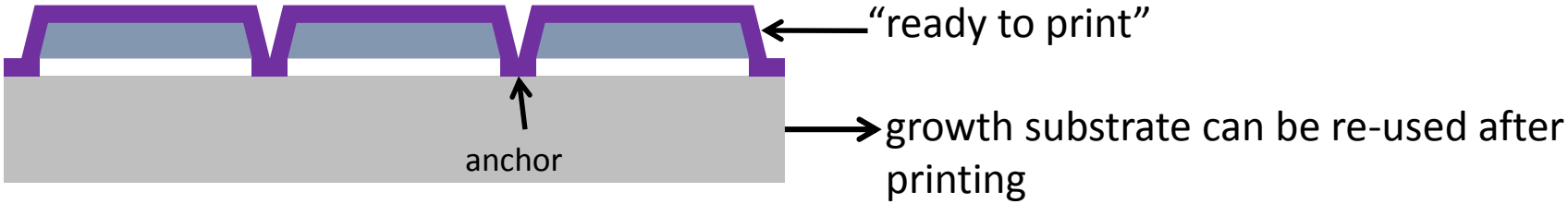
Printable Compound Semiconductors

1. Epitaxial Growth (MOCVD, MBE, etc…)



2. Patterning of material down to substrate

3. Formation of anchor and removal of release layer

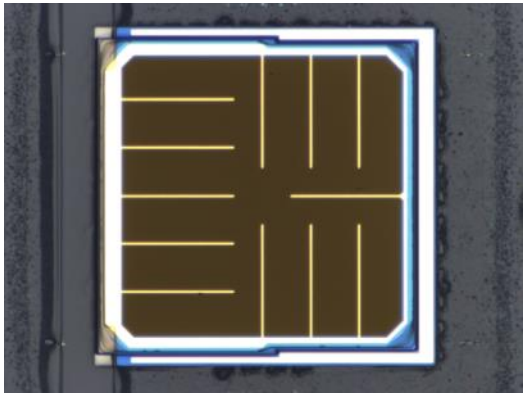


Epitaxial compound semiconductors are very practical systems for printing because lattice-matched sacrificial layers can be introduced under the device layers.

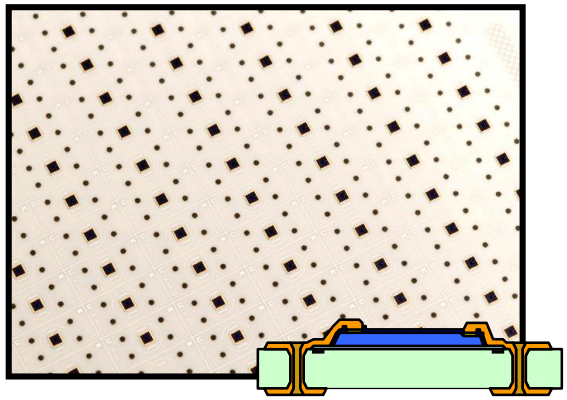
Examples of Printed GaAs-based Devices

SEMPRIUS

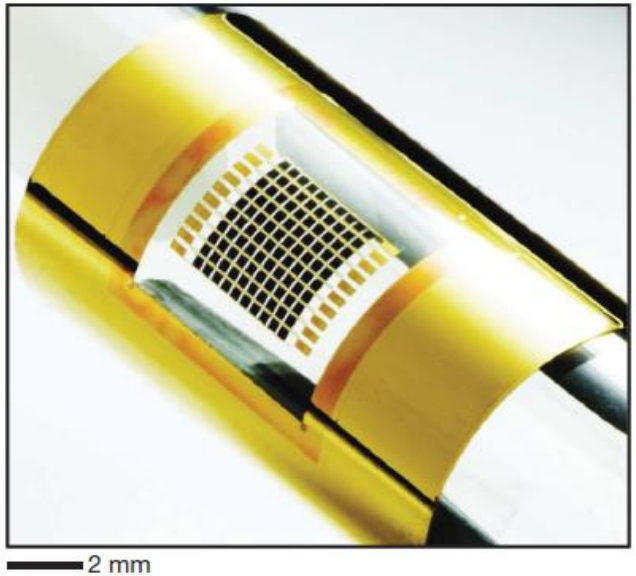
43% efficient solar cell printed to as-fired ceramic. Cell contains InGaP, InGaAs, GaAs.



600um x 600um x 10um

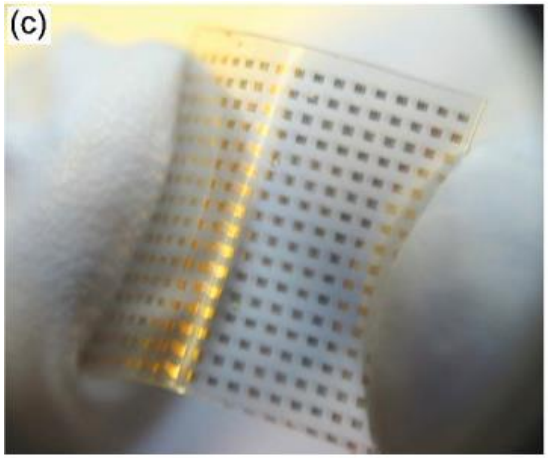


Flexible GaAs Solar Cells



J. Yoon, S. Jo, I.S. Chun, I. Jung, H.-S. Kim, M. Meitl, E. Menard, X. Li, J.J. Coleman, U. Paik and J.A. Rogers, "GaAs Photovoltaics and Optoelectronics Using Releasable Multilayer Epitaxial Assemblies," Nature 465, 329-333 (2010).

GaAs MeSFETS on Plastic



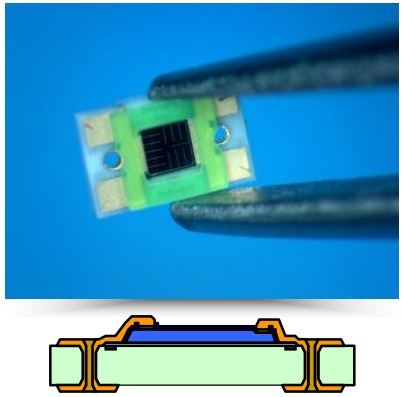
Applied Physics Letters 87, 083501 (2005)

http://rogers.matse.illinois.edu

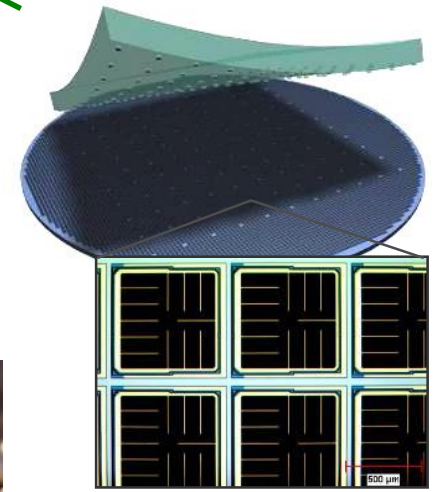
X-Celeprint

Elements of the Semprius Concentrator Photovoltaic (CPV) Module Design

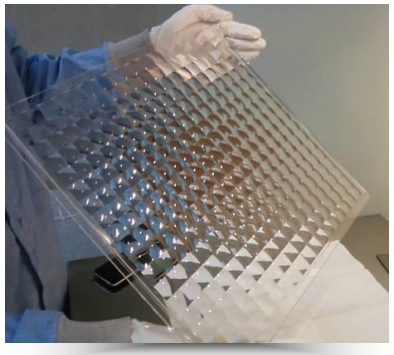
Surface-mount interposer



Transfer printed microcells



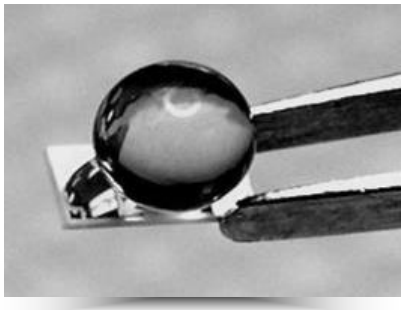
Silicone-on-glass primary lens



Low-profile module enclosure

Monolithic backplane

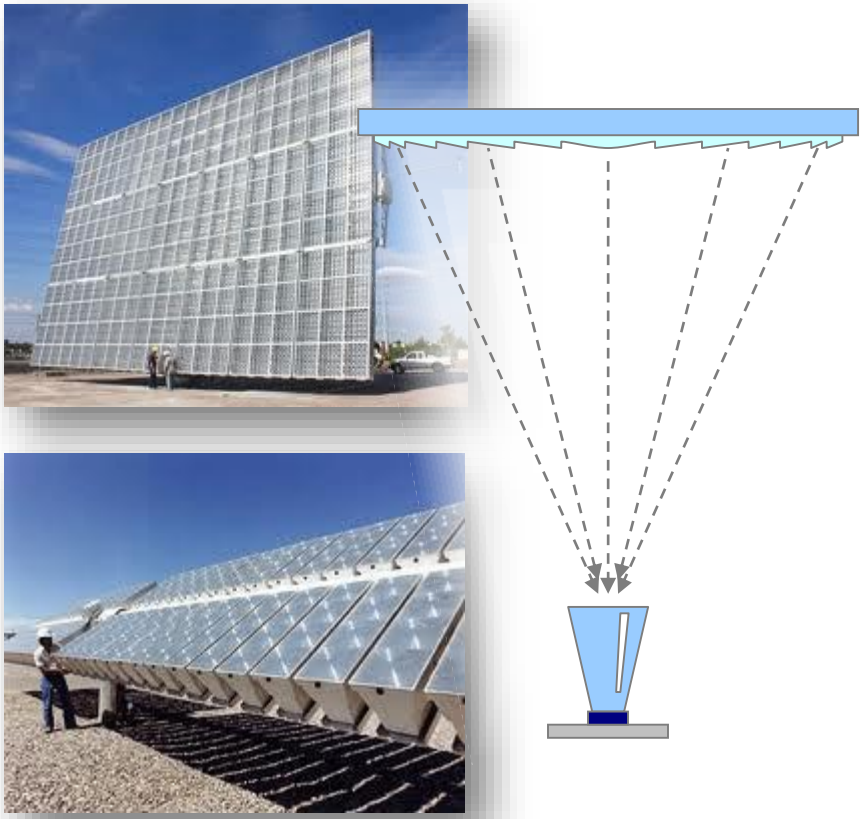
Secondary ball lens



Concentrator Photovoltaics (CPV) and Energy Extraction

- The most efficient solar PV technology for geographies with strong solar resources
- Focus sunlight onto high-efficiency multi-junction cells

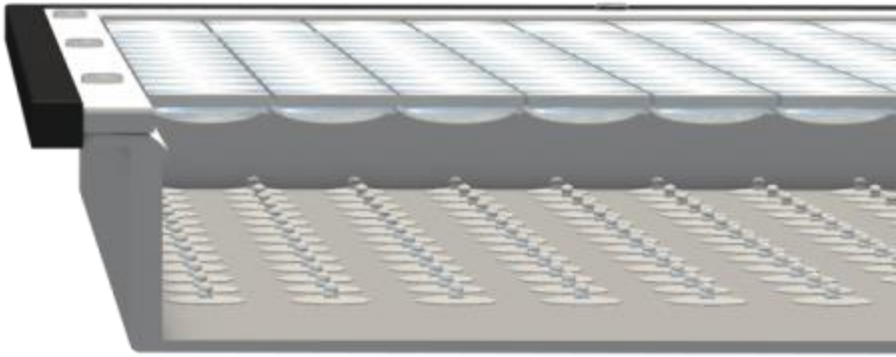
Conventional approach to CPV



Smaller is better.

- more efficient extraction of useful energy
- easier to expel waste heat
- reduced materials requirements & weight

→ performance & cost advantages

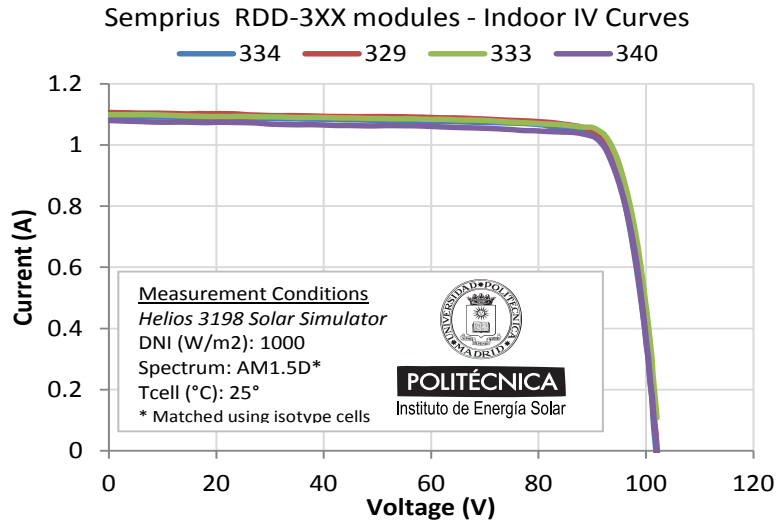


Need to overcome assembly challenges

- reduce per-part cost
- maintain precise alignment

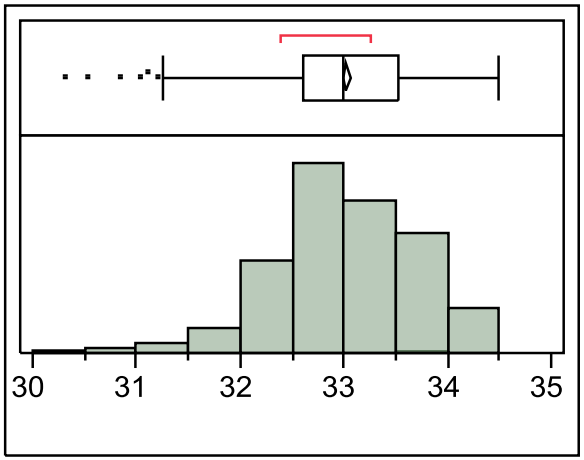
The Semprius CPV module—high performance, manufactured consistently

Up to η = 35.6% independently verified



Distributions

Module Efficiency (%)



Quantiles

100.0%	maximum	34.49
99.5%		34.4185
97.5%		34.1463
90.0%		33.89
75.0%	quartile	33.5225
50.0%	median	33
25.0%	quartile	32.6
10.0%		32.24
2.5%		31.73
0.5%		31.0545
0.0%	minimum	30.31

Moments

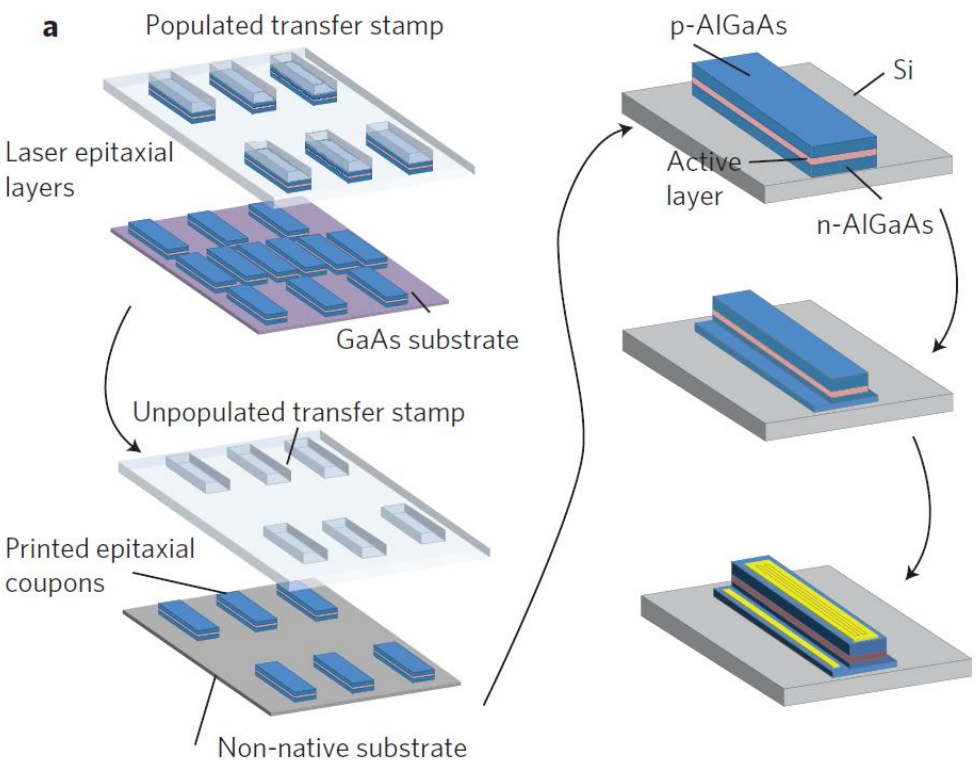
Mean	33.028759
Std Dev	0.640705
Std Err Mean	0.0224567
Upper 95% Mean	33.072839
Lower 95% Mean	32.984679
N	814

Semprius projects

Heterogeneous Integration of Lasers on Silicon

Tyndall National Institute

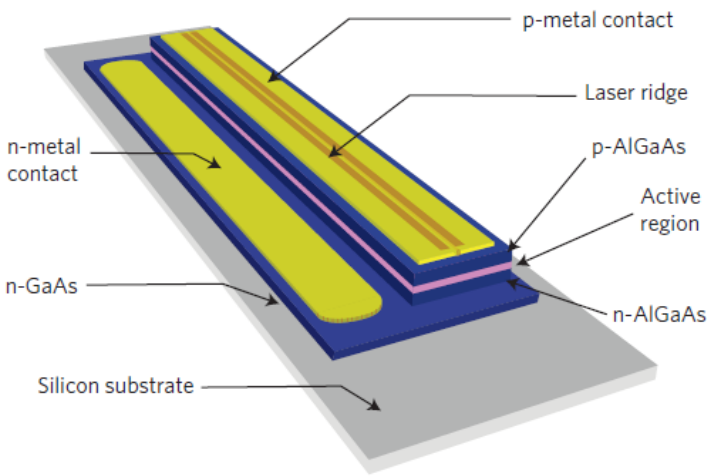
Seagate



nature photonics LETTERS
PUBLISHED ONLINE: 19 AUGUST 2012 | DOI: 10.1038/NPHOTON.2012.204

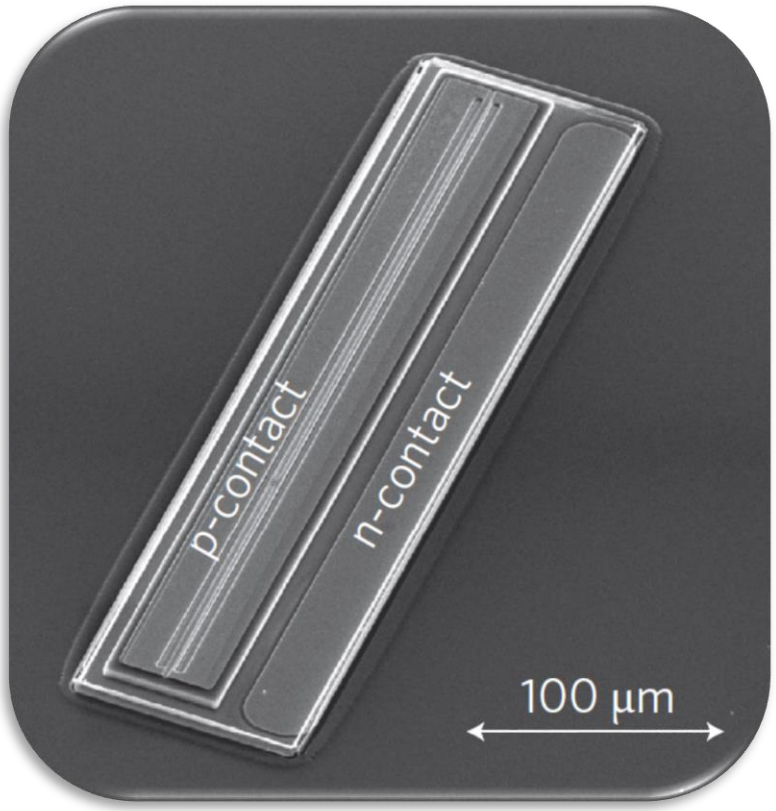
Wafer-scale integration of group III–V lasers on silicon using transfer printing of epitaxial layers

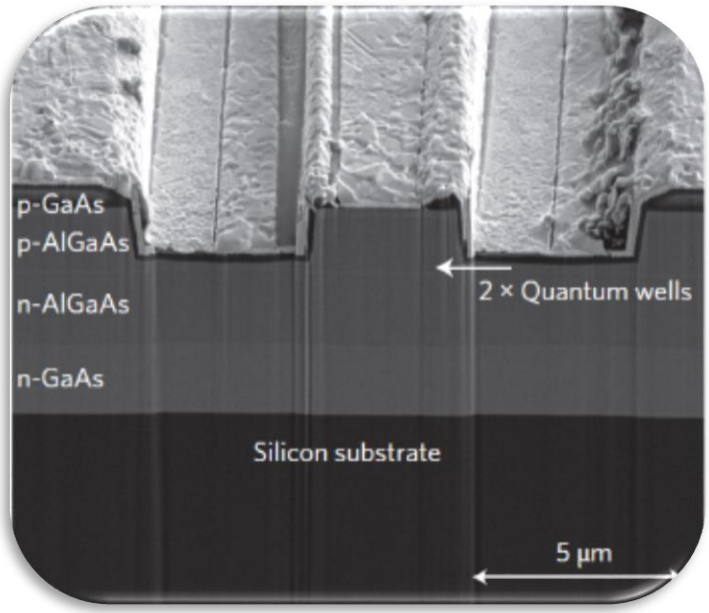
John Justice[1]*, Chris Bower[2], Matthew Meitl[2], Marcus B. Mooney[3], Mark A. Gubbins[3] and Brian Corbett[1]*



X-Celeprint

Heterogeneous Integration of Lasers on Silicon

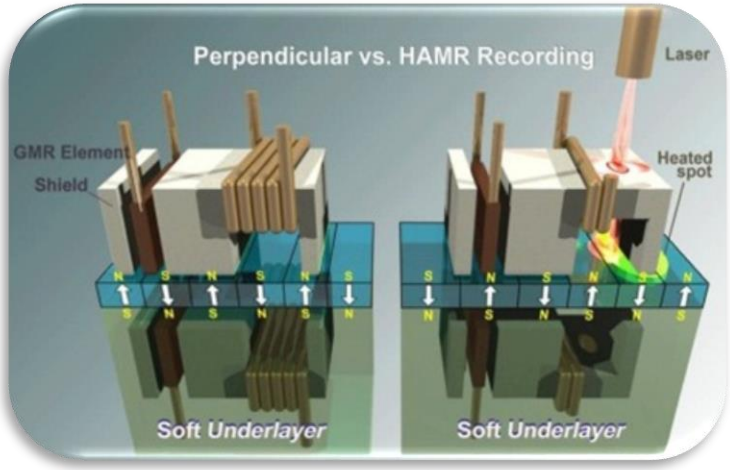




- adhesiveless “direct” printing
- laser fabricated post printing
- etched facet laser
- optical power of 15mW per facet at room temperature

Applications for Printed Lasers

- Heat Assisted Magnetic Recording (HAMR)

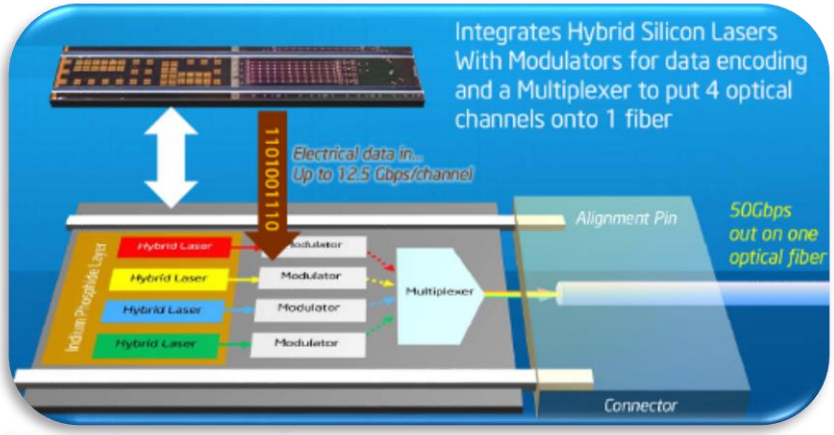


COMPUTERS

Seagate demonstrates HAMR hard drive technology that promises 60 TB HDDs

By Darren Quick
March 19, 2012
10 Comments

- Silicon Photonics

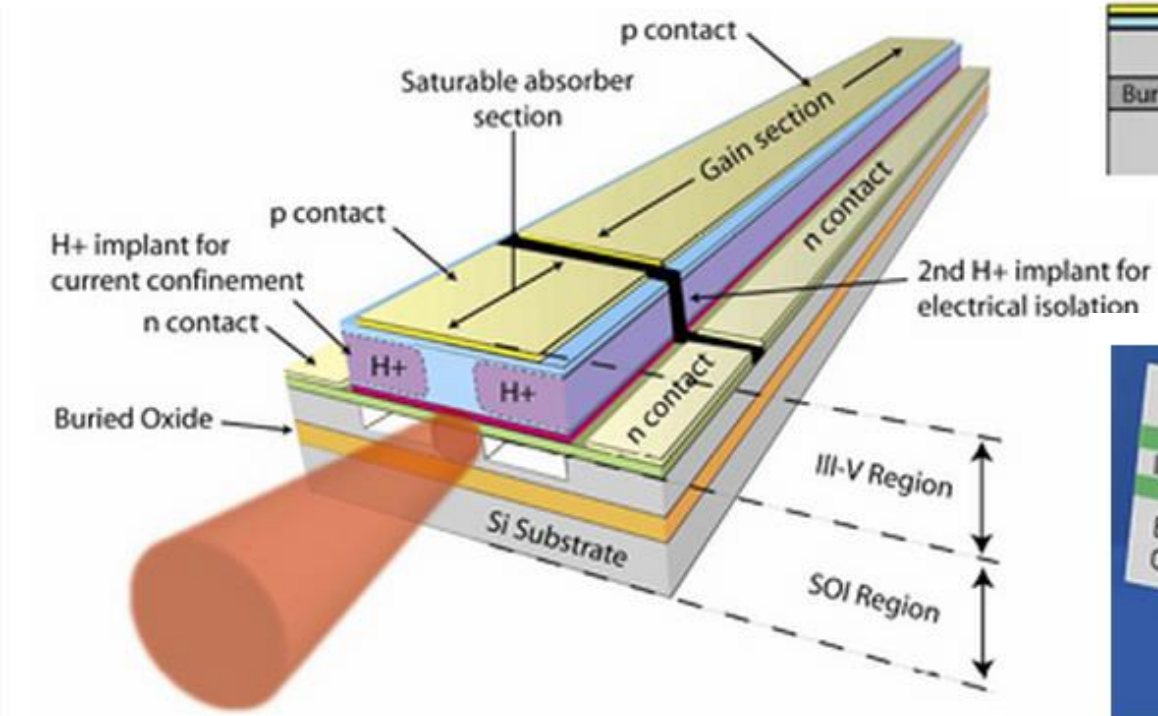


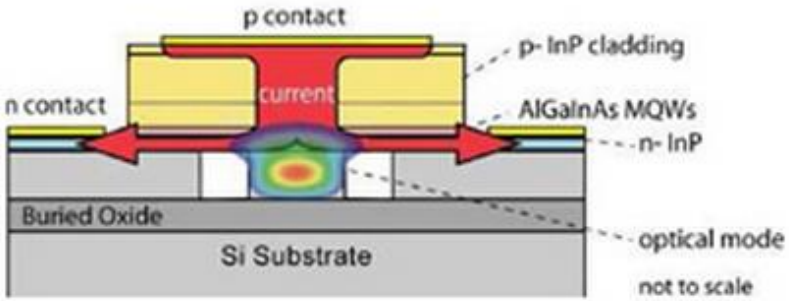
Intel talks lasers on silicon again

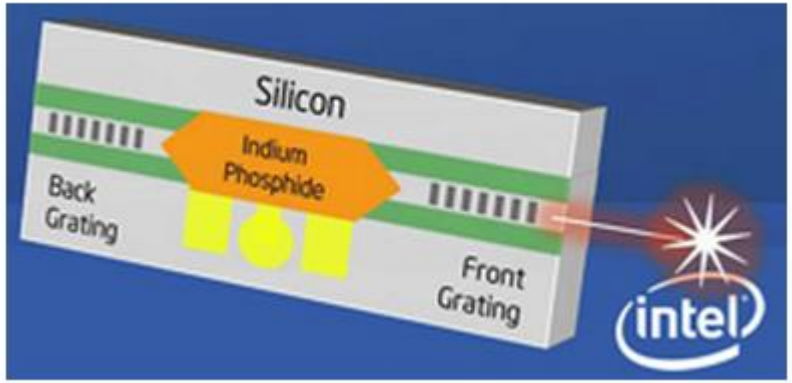
50Gbps and a new connector

Jul 27, 2010 by Charlie Demerjian

Silicon Photonics





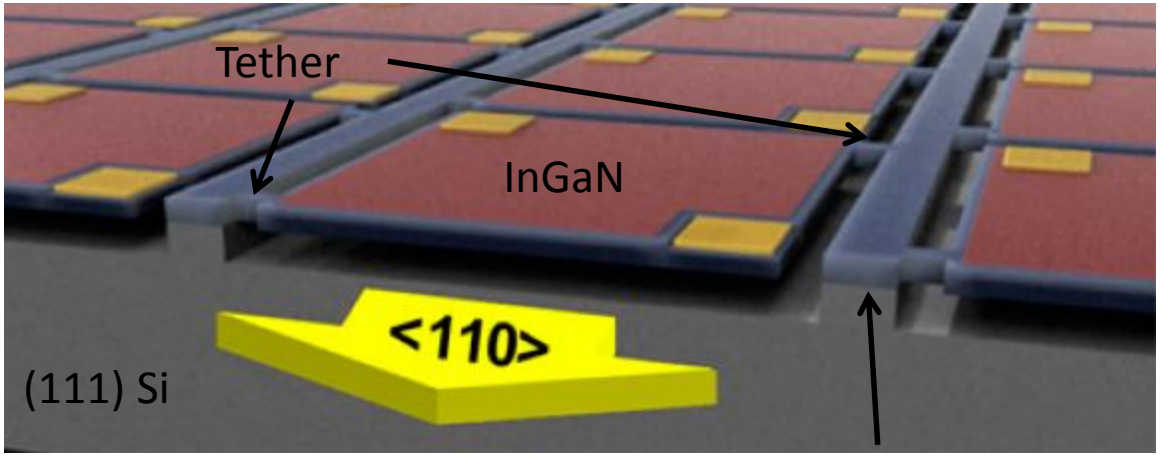


http://www.semiconductor-today.com/news_items/2010/AUG/INTEL_050810.htm

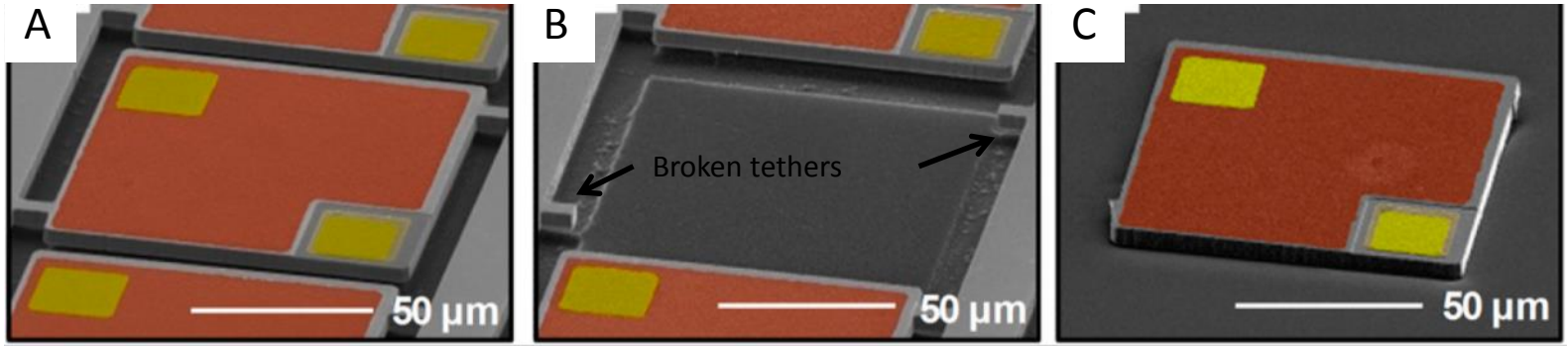
- A good laser remains a challenge for silicon photonics
- UCSB, Intel and others have demonstrated promising “hybrid” lasers that require III-V materials to be coupled to an underlying silicon waveguide
- µTP represents a cost-effective solution for sparse integration of this III-V gain media

Printable Gallium Nitride

Rogers, J. A., et al. (2011). Unusual strategies for using indium gallium nitride grown on silicon (111) for solid-state lighting, PNAS



The anisotropic nature of the Si etchant is utilized to anchor the material to the wafer



A. "ready-to-print" InGaN LED

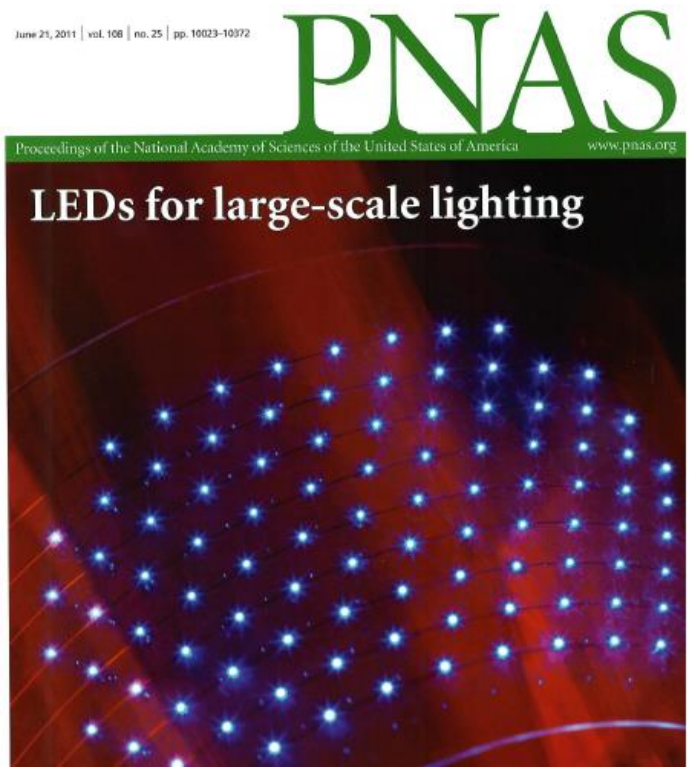
B. After pick-up

C. Printed InGaN LED on plastic

GaN-based materials or devices (LEDs, etc…) grown on (111) Si are also printable. A thin layer of silicon can be removed from underneath the device layer.

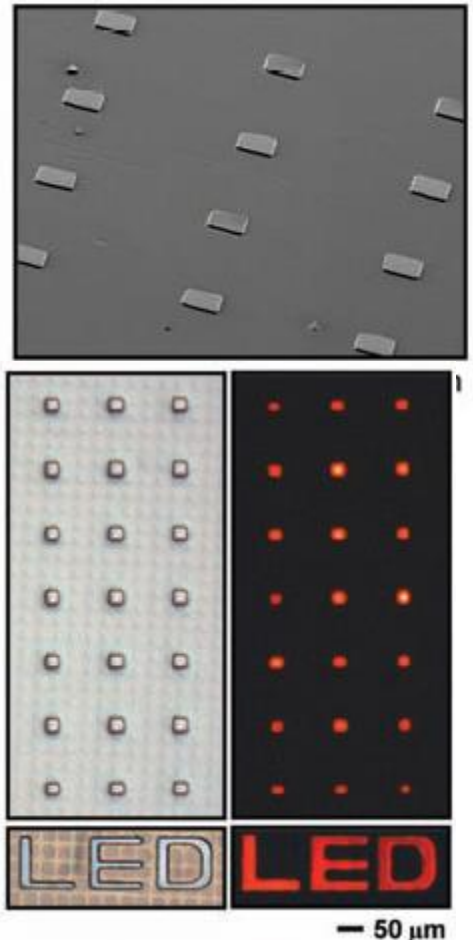
Application: Printed iLEDs

Flexible GaN-based iLED Arrays



http://rogers.matse.illinois.edu

Flexible GaAs-based (red) iLED Arrays

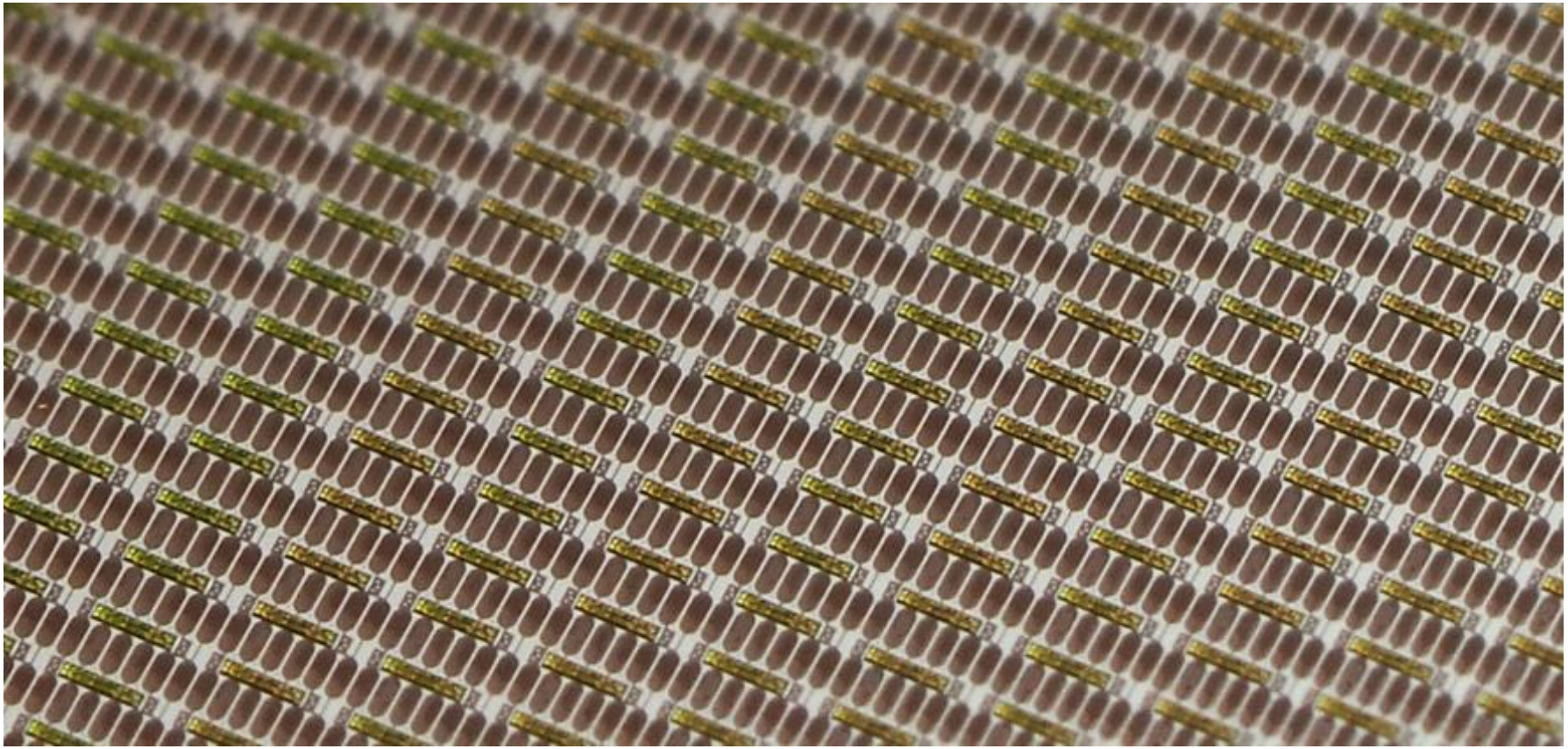


SCIENCE VOL 325 21 AUGUST 2009

Summary

- µTP allows manipulation of objects that are too small, numerous, fragile, or otherwise difficult to handle by other means
- µTP provides mature electronic materials on non-native substrates with integration-ready solutions for many applications
- X-Celeprint is ready to support interested end-users with application specific development, technology transfer and hardware

Thank You! Questions?



Acknowledgements: John Rogers, UIUC → original inventors and many examples shown here
Semprius → developed Micro-Transfer-Printing technology, printable 3J solar cells and printable ICs
XFAB, Tyndall National Institute, Seagate, CDT

cbower@X-Celeprint.com

X-Celeprint