IEEE

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

CPMT
IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY
ORANGE COUNTY CHAPTER

IEEE Components, Packaging and Manufacturing Technology Society

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Thursday, August 23, 2012 Tutorial

Fundamentals of Signal Integrity, Power Integrity and EMI/EMC for Microelectronic Packaging and System Design

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OVERVIEW:
This course will teach the fundamentals of IC Package Electrical Performance metrics such as Signal Integrity, Power Integrity and Electromagnetic Compatibility and how to apply that knowledge to an advanced IC Package design. Common EMI related problems found in chassis design will be discussed along with examples. This often complex content will be delivered at a level that should be understandable to common IC package, PCB and System Designers.

WHO SHOULD ATTEND:
IC Packaging engineers, PCB Designers, EMC test & design engineers, Signal and Power Integrity engineers who wish to refresh their fundamental understanding of SI/PI/EMC principles and Managers responsible Interconnect Design teams

TOPICS:

- The basic principles of interconnect electromagnetics, including RLC parasitics and transmission line behavior
- Relationship between common signal integrity and power integrity design issues and system level EMC
- Interconnect related design challenges such as signal reflections, crosstalk, SSN and PDN resonances.
- Electrical performance concerns for typical wafer level, flip chip and wire bonded packages on laminate / build-up substrates
- Common problems found in chassis design

HOSTING and LAB TOUR:
The event is hosted by Intertek (www.intertek.com) in Lake Forest, CA and will include a visit to Intertek's state-of-the-art EMC compliance test labs for a demonstration of common EMI/EMC phenomena.

ABOUT THE INSTRUCTORS:

Sam Karikalan is a Senior Principal Engineer at the Package Eng Group of Broadcom Corporation, Irvine, CA. His responsibilities include IC Package Electrical Design, covering SI, PI & EMC performance requirements. Sam started his career 25 years ago as an EMC Scientist at SAMEER-Center for Electromagnetics in Chennai, India. He then moved to AMD to work on Microelectronics EMC and Signal Integrity. Before joining Broadcom in 2005, he also worked at Primarion and STATS ChipPAC on IC Package Electrical Design. He holds five issued US patents and several pending US and International patents, in the area of Component level EMC measurements and IC Package Design.

David O'Reilly is currently the Lab Manager and Engineering Team Leader for Intertek's EMC lab in Lake Forest. His work history includes working as an EMC Compliance Engineer for Extron Electronics with expertise in design for compliance, for A/V, ITE, Medical, and related products, and 12 years at the Canon R&D center where he was responsible for EMC compliance for Canon products at the R&D level.

Date:	**Thursday, August 23rd, 2012**	**VERY LIMITED NUMBER OF SEATS ONLY**
Location:	**Intertek, 25791, Commercentre Drive, Lake Forest, CA 92630**	
Time:	**8:30am: Registration, 9:00am – 5:00pm: Short Course (including lunch & lab tour)**	
Registration Fee:	**IEEE members - $250; Non-members of IEEE - $400; Student IEEE members - $75; Student Non-IEEE Members - $125** (includes Sandwich Lunch & Training material) Register at http://www.eventbrite.com/event/3812268598.	

For more information, please contact Kimberly Hawkins at kimberly.hawkins@intertek.com or Sam Karikalan at samkarikalan@ieee.org.