

IEEE Components, Packaging and Manufacturing Technology Society Orange County Chapter

Tuesday, November 15, 2011 Tutorial

Short Course on Thermal Design and Modeling of IC Packages

Dr. Sam Z. Zhao

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OVERVIEW:

This short course will provide a systematic approach to the understanding of IC package-related thermal issues, thermally enhanced packages, industry standard thermal tests, IC package thermal modeling techniques, and system thermal design using IC package compact and detailed thermal models. Students completing this class should gain basic understanding of IC package thermal characteristics, improve their ability and understanding to make appropriate IC package technology selection and system design decisions, and to achieve reliable performance of complex electronic devices.

WHO SHOULD ATTEND:

Packaging engineers, system engineers, thermal and mechanical engineers, PCB layout engineers, field support personnel, marketing personnel, design, process, failure analysis, reliability engineers, and material scientists.

TOPICS:

- Understanding IC Package Thermal Data
 - Theta-ja, Theta-jb, Theta-jc, Psi-jt
- IC Package Thermal Enhancement Design
 - Minimization of Theta-jc: Exposed Pad, Heat Spreader, TBGA, Flip Chip, Others
 - Minimization of Theta-jb: Exposed Pad on Board, Drop-in Heat Sink, Thermal Vias, Ground Balls
- JEDEC Standards for Package Thermal Characterization
 - Still Air Test, Wind Tunnel Test, Theta-jb Measurement Discussion
- Thermal Modeling of IC Packages
 - Computational Fluid Dynamics (CFD) Based Simulations
 - Heat Conduction Based Simulations
 - Example of a Package Level Simulation: JEDEC Thermal Characterizations
 - Example of a System Level Simulation using compact and detailed package models: Network Switching Box

ABOUT THE INSTRUCTOR:



Dr. Sam Z. Zhao is an Associate Technical Director at Broadcom Corporation, Irvine, CA. He received his Bachelor's and Master's degrees from Tsinghua University, Beijing, China, and his Ph.D. degree from the University of Illinois, Chicago. He did research at Cornell University in Ithaca, NY, and at the Swiss Federal Institute of Technology (ETH), Zurich in Switzerland. He has published more than 38 technical articles in peer-reviewed journals and conference proceedings. He has over 38 issued US patents.

Date: **Tuesday, November 15th, 2011**

Location: **Room 304 (Lunch Room), Henkel Electronic Materials, LLC, 14000 Jamboree Road, Irvine, CA 92606**

Time: **12:00-1:00pm: Lunch, 1:00-5:00pm Short Course**

Registration Fee: **IEEE members - \$40; Non-members of IEEE - \$50; Students - \$25** (includes Sandwich Lunch & Training material)
Register online at http://meetings.vtools.ieee.org/meeting_view/list_meeting/8851. Number of seats is limited to only 40. For questions on Registrations, please contact **Fan Yeung** at fyeung821@yahoo.com.

For more information please call any of the following officers of [the IEEE CPMT OC Chapter](#):

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