THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY ORANGE COUNTY CHAPTER

IEEE Components, Packaging and Manufacturing Technology Society

Orange County Chapter

Wednesday, October 12, 2011 Technical Meeting

3D IC/Si Integration Technology

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Abstract

3D integration consists of 3D IC packaging, 3D IC integration, and 3D Si integration, which will be discussed in this lecture. Emphases are placed on the key enabling technologies for 3D IC/Si integrations, such as TSV (through-silicon via) forming and filling, front and back-side metallization, RDL (redistribution layer), IPD (integrated passive devices), temporary wafer bonding, wafer thinning and handling, wafer de-bonding, thin chip/wafer strength measurement and improving, W2W bumpless bonding, lost-cost lead-free microbumping (≤15µm pitch) and assembly, low-temperature wafer bumping and C2C, C2W, and W2W bonding, and thermal management. Useful characterization and reliability data for 3D IC integration will also be provided.

The application of 3D IC integration such as CMOS image sensor, MEMS, LED, memory + logic, logic + logic, memory + microprocessor, active and passive interposers will be presented. More than 15 companies' passive interposers (samples not power-point engineering) used as substrates, stress relief (reliability) buffer, carriers, and thermal management tools will be presented and discussed. Furthermore, the critical issues of TSV and 3D IC integration will be given and some potential solutions or research topics will be recommended. Finally, several roadmaps of 3D IC/Si integration will be provided. All the materials are based on the technical papers and books published within the past 3 years by the lecturer and others.

Biography

Dr. John Lau has been an ITRI Fellow since January 2010. Prior to that, he was a visiting professor at HKUST for 1 year, Director of MMC Laboratory with IME in Singapore for 2 years and a Senior Scientist/MTS at HPL/Agilent in California, USA for more than 25 years. With more than 35 years of R&D and manufacturing experience, Dr Lau has published more than 350 peer-reviewed papers, 30 issued and pending US patents, given 270 lectures, workshops, and keynotes worldwide, published 16 textbooks on 3D MEMS packaging, 2D and 3D IC integrations, flip chip & WLP, high-density PCB, SMT, lead-free materials, soldering, manufacturing and reliability. John earned his PhD degree from the University of Illinois and three MASc degrees in North America. John received many awards, e.g., the best IEEE/ECTC Proceedings paper (1989) award, best ASME Transactions paper (Journal of Electronic Packaging, 2000) award, best IEEE Transactions paper (in CPMT, 2010) award, ASME/EEP Outstanding Technical Achievements award, IEEE/CPMT Manufacturing award, Outstanding Contribution award, and Outstanding Sustained Technical Contribution award. SME Total Excellence in Electronics Manufacturing award, and IEEE Meritorious Achievement in Continuing Education award. He is an elected ASME Fellow and has been an IEEE Fellow since 1994.

Date: **Wednesday, October 12th, 2011**

Location: **Broadcom Corporation, 5300 California Ave., Irvine, CA 92617 – Bldg. 2 Conf. Room 2-1037 (Salt Creek)**
Check in at the Security Gate and proceed to Bldg. 2. You will be escorted into the building.

Time: **5:30-6:00pm: Social time, 6:00-7:00pm: Presentation, 7:00pm: Dinner** (Pizza and Soda provided by CPMT OC Chapter)

RSVP: **IEEE members and non-members all are welcome to attend. Please RSVP at**
http://meetings.vtools.ieee.org/meeting_view/list_meeting/8511. Please be at Bldg. 2 entrance by 6:00 pm; no escorts after that. For questions regarding RSVP please contact Mehdi Saeidi (saeidi@ieee.org).

For more information please call any of the following officers of the IEEE CPMT OC Chapter: ***Follow us on LinkedIn.***

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