High-Density 3D Power Packaging with Heterogeneous Passive-Active Integration

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Heterogeneous Integration with Nanopackaging

- Power delivery in computing systems
  - Integrated voltage regulator
  - Capacitors and Inductors

- Medium-power packaging
  - Embedded-die packaging with die-attach materials
  - High-temperature organic packaging

- High-Power packaging:
  - Doubleside cooling
  - High-voltage passives

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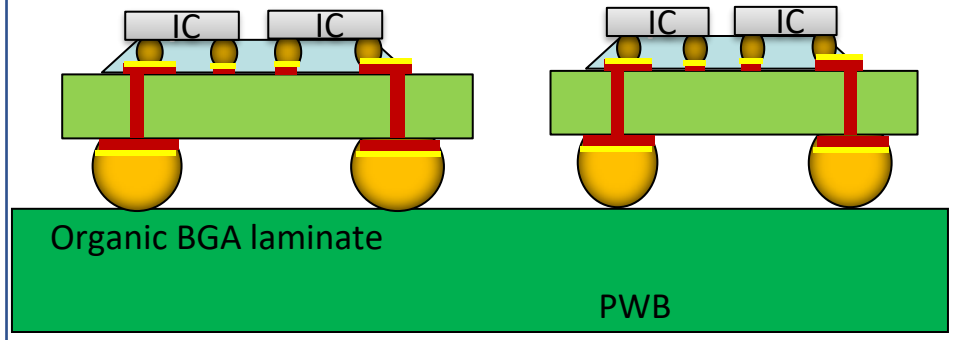
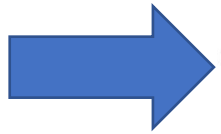
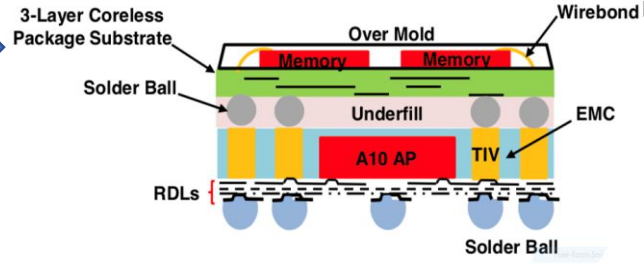
3D Heterogeneous Package Integration

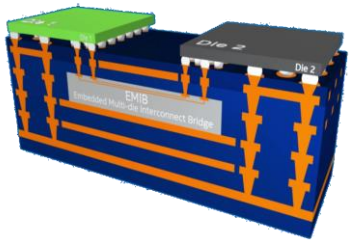




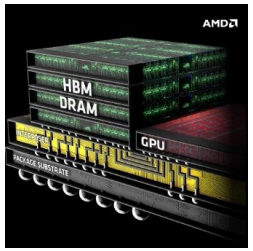
Apple/TSMC



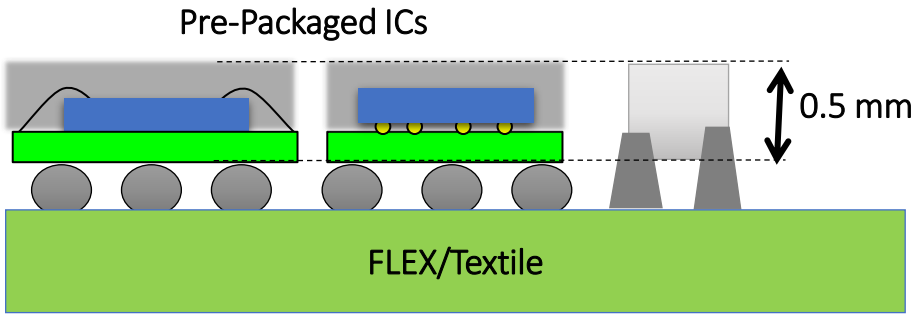
Intel

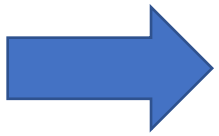


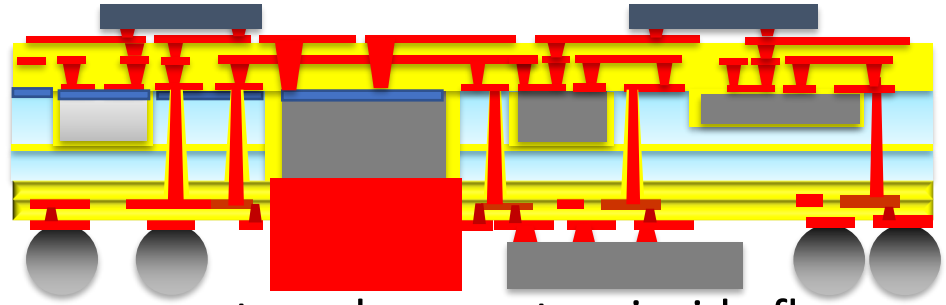
AMD



2D packaging to 3D high-density packaging







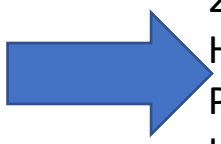
Pre-packaged components on flex to embedded components and connectors inside flex

Pre-packaged and molded devices

Large power components and RF interfaces

2D Surface assembly

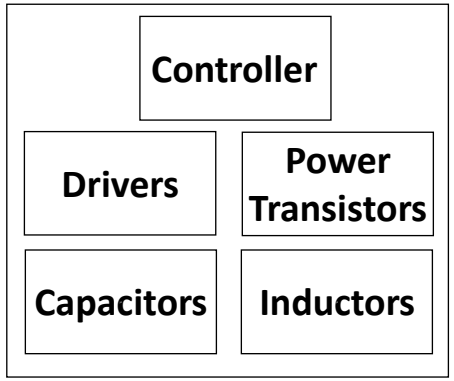
Traditional PCB processes



2.5D or 3D integration: logic-memory, transceiver-Antenna,
High-bandwidth interconnects with interposers and fan-out packages
Passive integration with actives
Integrated EMI, heat-spreaders, encapsulation

Power Delivery for Processors

Integrated Power Electronic Component (IPEC)



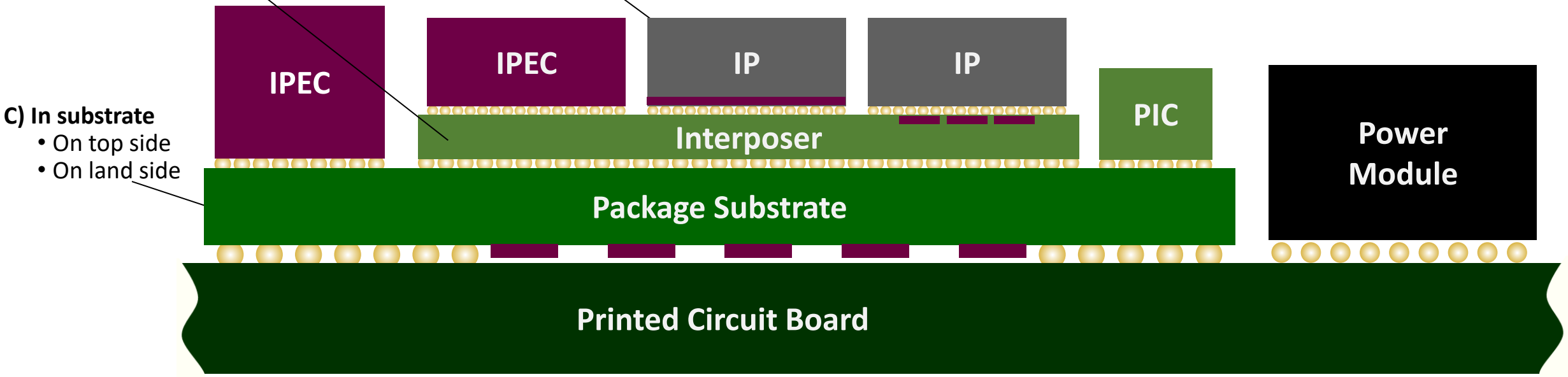
A) In load *(IP, HBM, PIC)*
- Monolithic integration
- Hybrid bonding

B) In interposer
- On top side
- Integrated in active interposer
- Embedded in organic interposer

C) In substrate
- On top side
- On land side

Inside SiP
Focus of this presentation

Outside SiP
A parallel initiative



IPECs may be partitioned and integrated in multiple ways, each potentially serving different parts of hybrid topologies

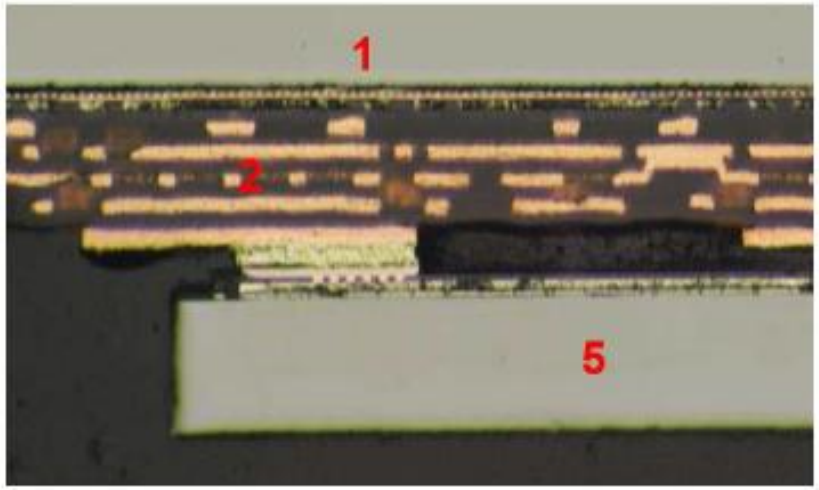
How to Partition the Power Components Around the Load?

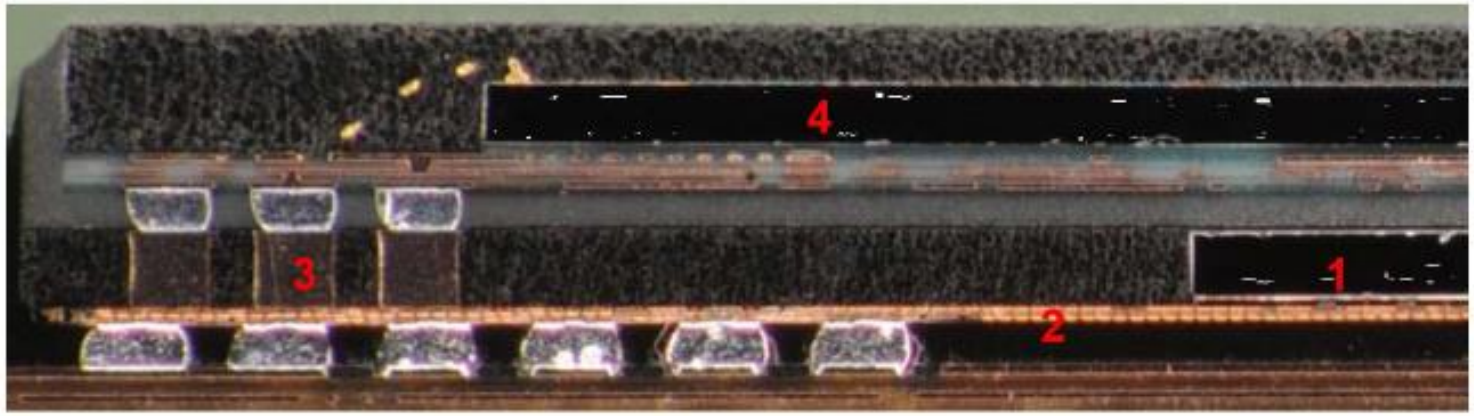
Apple iPhone 8 Application Processor/Memory in Fanout (Info) Package

Source: Prismark Partners October 2017

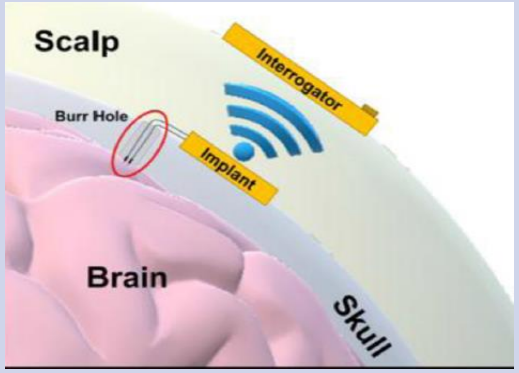
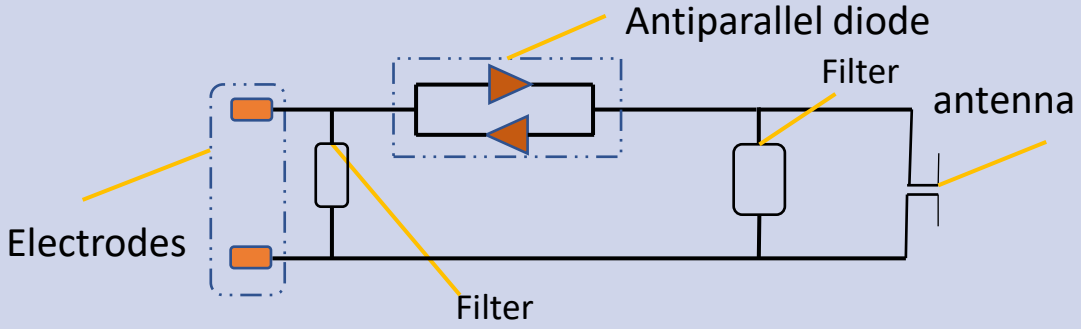
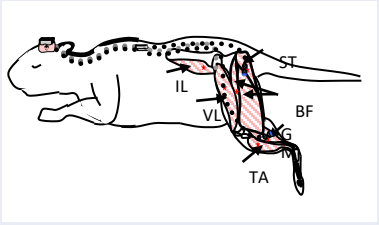
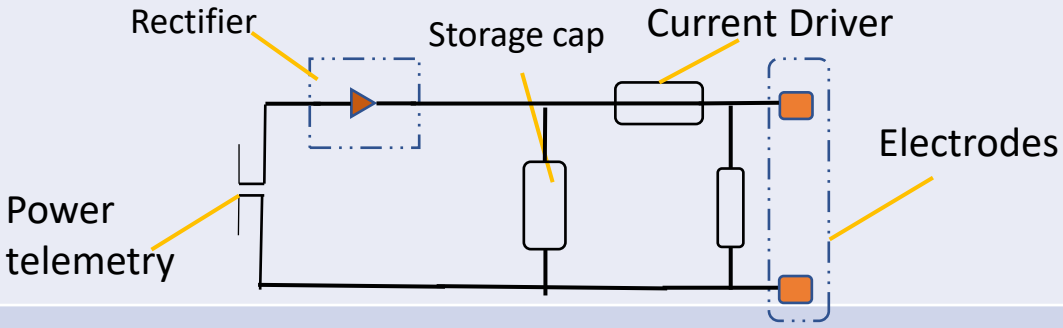
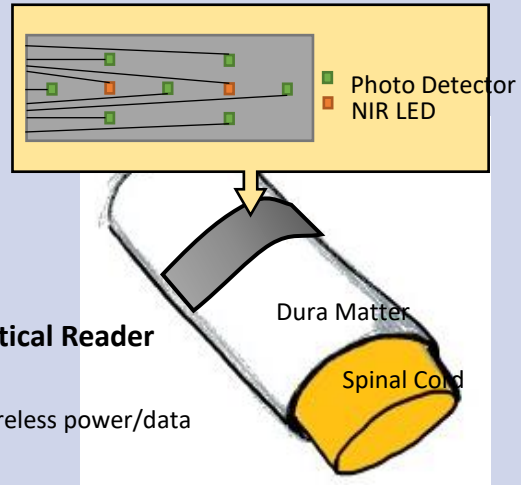
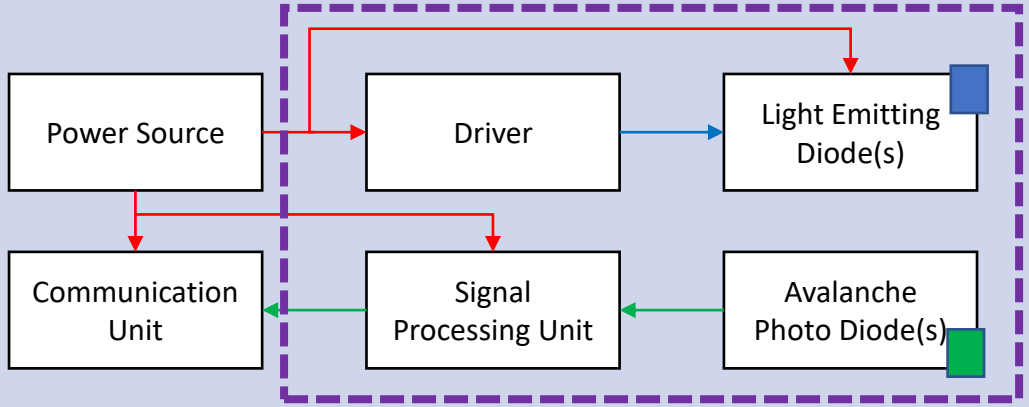
HETEROGENEOUS INTEGRATION ROADMAP

- 13.9 x 14.8mm InFO PoP Package
  - 8% smaller than A10
  - 790µm package height
- Memory package with SxS die
  - Die Thickness:140µm
  - 140µm EMC thickness over die
  - 3L substrate; 90µm thick
  - Underfill between packages
- Processor : ~10 x 8.7mm
  - 30% smaller than A10
  - 150µm thick; 15µm "top coat"
  - 50µm thick, four-metal-layer RDL

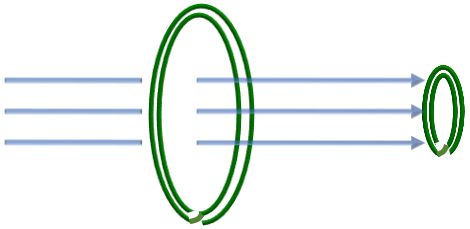




1 A11 Die
2 RDL
3 Vertical Connection
4 Memory
5 Capacitor

Medical Device Application	System Description
	• ***Neural recording System:*** • Piezomagnetic antenna to turn on the diode 
 	• ***Neural stimulation system*** • Piezomagnetic power telemetry to charge the storage capacitor 
	• ***Biophotonic system*** • Piezomagnetic power and data telemetry to power the photonics, drivers and RF interface 

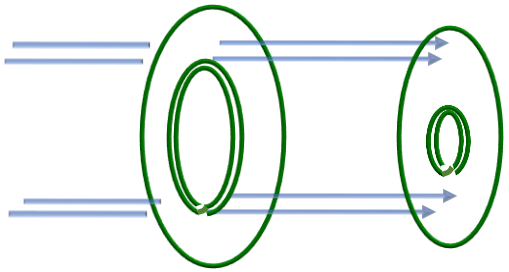
Power Telemetry – Wearable and Implantable



Two-Coil Inductive Link

Receiving coil should be large enough

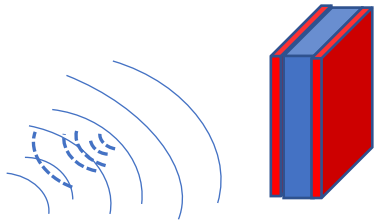
0.1 – 1 mW/mm^2



Multiple-Coil Inductive Link

Efficiency can be increased with larger separation distance

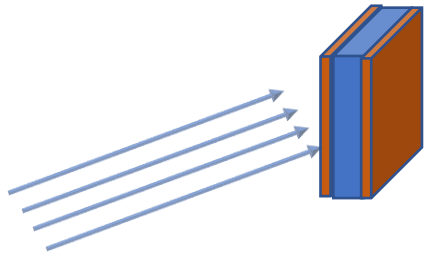
1 – 5 mW/mm^2



Piezoelectric power telemetry

Receiving link can be reduced to < 1 mm

0.1 – 1 mW/mm^3

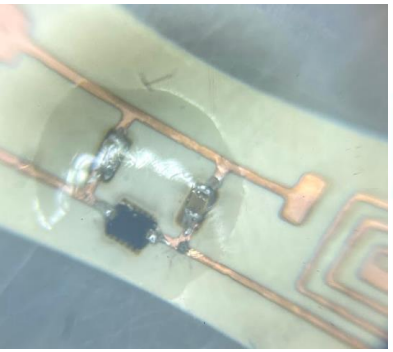


Piezo-magnetostrictive power

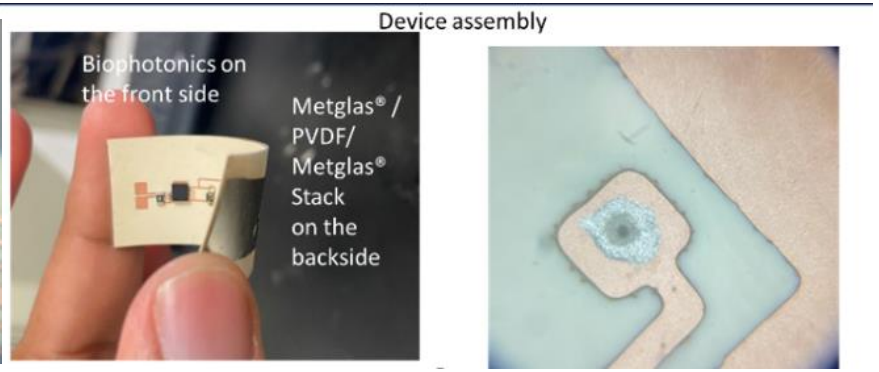
Higher power density can be achieved with smaller sub-mm receivers

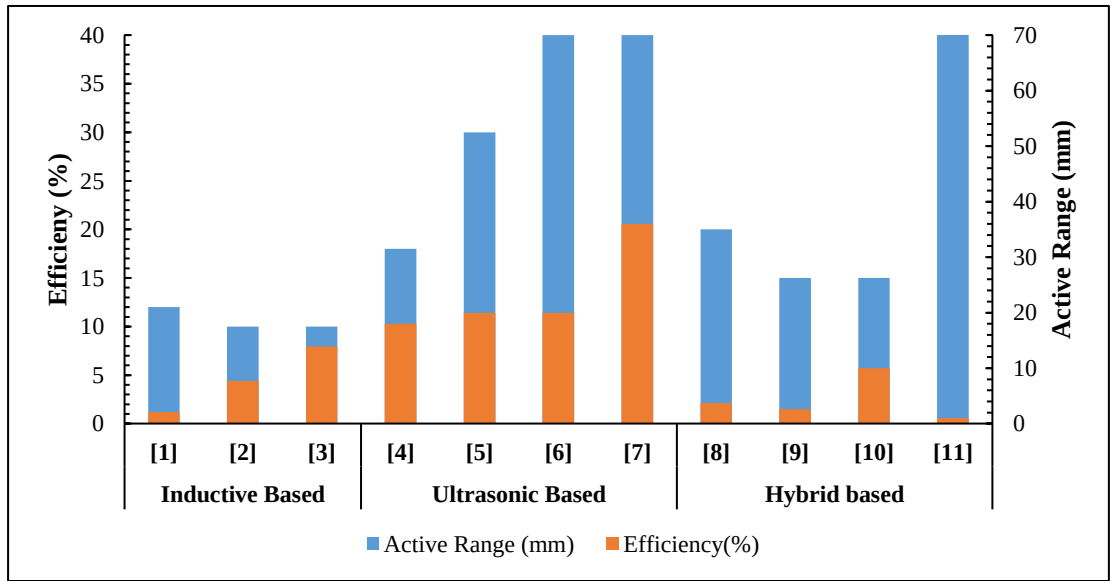
1 – 20 mW/mm^3

Inductive link

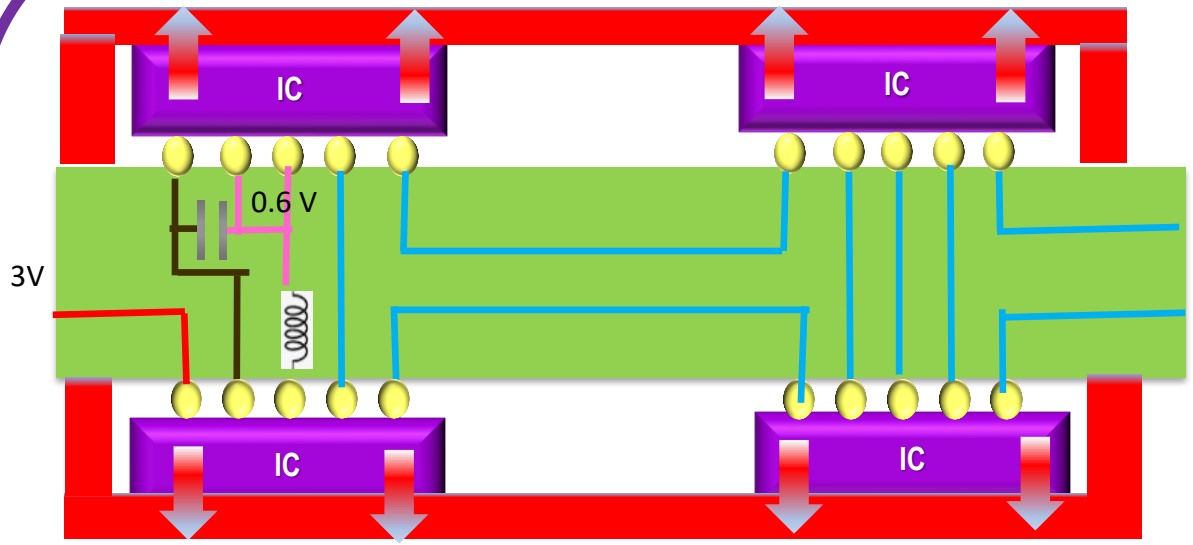


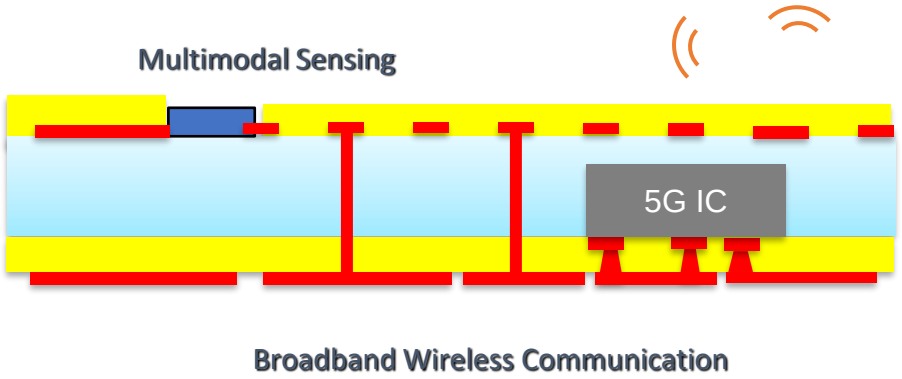
Piezo-magneto





Nanopackaging Drives Future Hardware

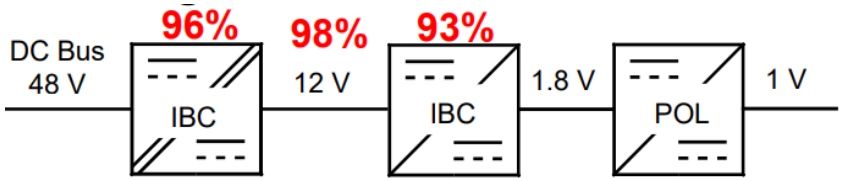




Power	**Nanocapcitors and inductors**
Thermal	**Cu-Graphene heat-spreaders**
Reliability	**ALD Inorganic films** **Humidity barriers**
RF	**Nanodielectrics and additive interconnects for 5G and wireless sensors**
Bioelectronics	**Electrodes** **Power and data telemetry** **Storage capacitors** **Remateable connectors**

https://ieeenano.org/nanopackaging-tc

Power Delivery



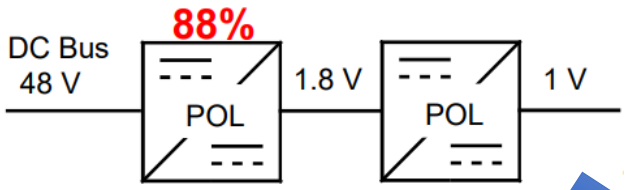
Utilize Advances in:

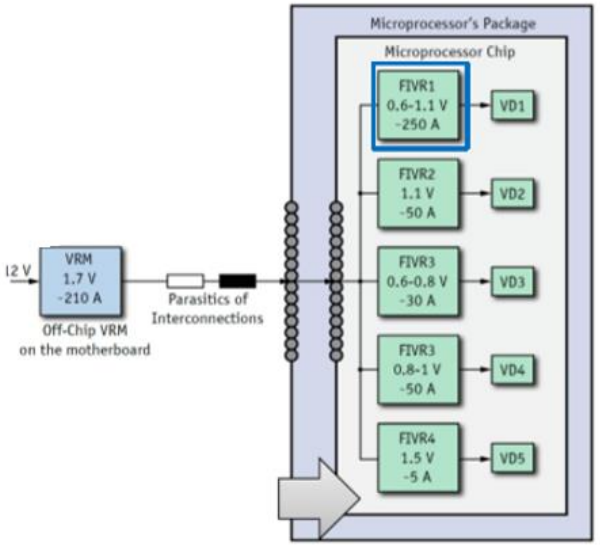
GaN

CMOS integration

Topologies

Passive components



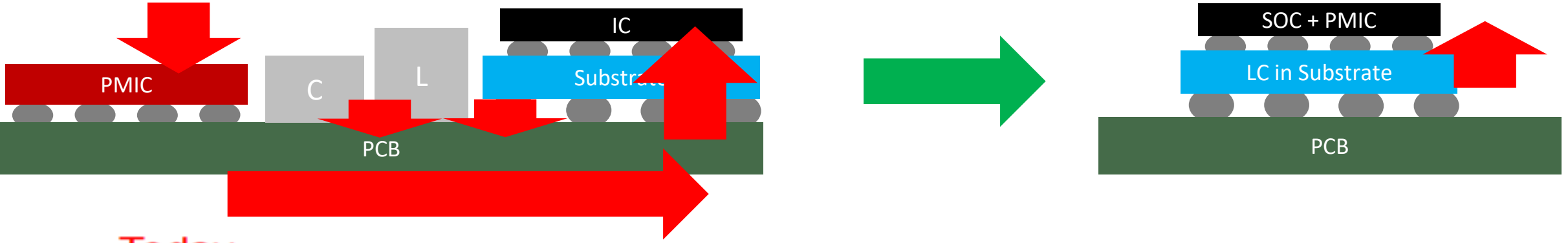


Minimize the stages of power conversion;

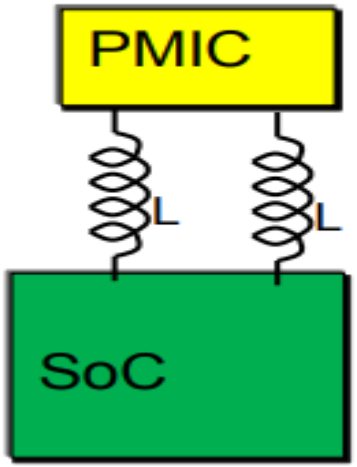
Perform power conversion right near the load;

Figures from EPC (Alex Lidow) and IBM Zurich (Arvind Sridhar)

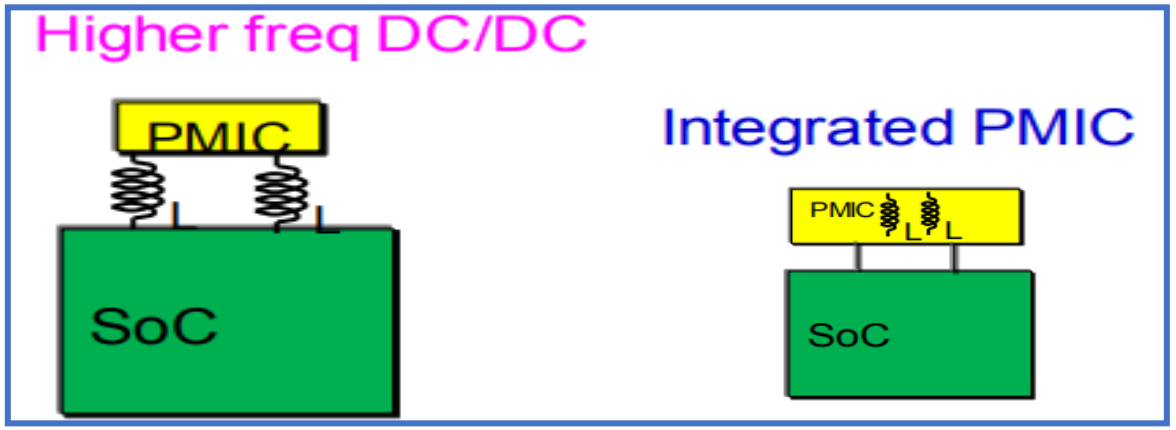
Role of PMIC in Power Delivery



Today



Enabled by advances in magnetics



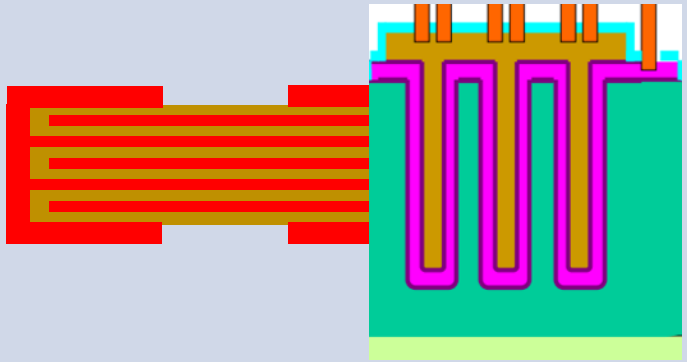
(Adapted from Indumuni Ranmuthu, PwrSOC 2016 [1])

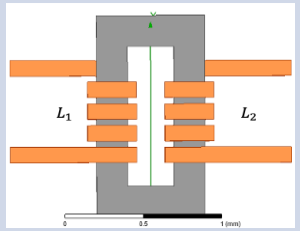
High-frequency power MOSFETS

Advanced Topologies

High-density integrated passives

R&D Needs

Capacitors 	Density	High K dielectrics; Enhance electrode surface area; New dielectrics and deposition processes
	Frequency stability	Electrodes and connectivity with lower parasitics
	Integration	Thinner form-factors; Substrate or wafer or fan-out embedding

Inductors  	Density	Higher permeability with saturation field and high resistivity
	Efficiency	Low coil DC losses ; Low core losses with low coercivity and eddy currents
	Integration	Substrate- or wafer-compatible process
	Current-handling	Design innovations; Scalability in thickness to handle higher current

Embedded Capacitors Roadmap

2000 | 2008 | 2016 | 2020 | 2025

Board or package embedding; I/O decoupling; 100 MHz

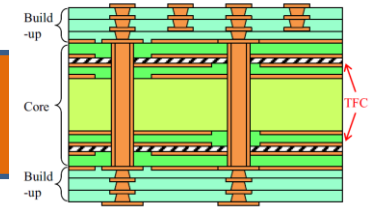
Embedded polymer laminate and dielectrics

0.1 nF/mm² Polymer laminate dielectrics

0.5 nF/mm² Polymer film dielectrics

1 nF/mm²

Embedded ceramic film



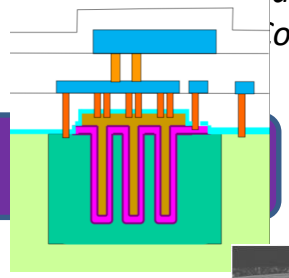
2-3 nF/mm² Thin oxides

20-30 nF/mm² BaTiO3 film

30-50 nF/mm2 enabled by new multicomponent oxides

Package embedding; Core and I/O decoupling; 100-500 MHz

Wafer-integrated capacitors



Silicon capacitors Deep trench

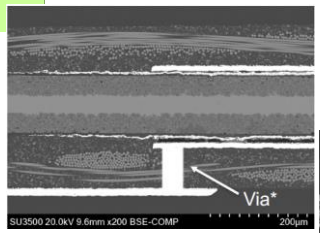
0.08 µF/mm² 0.25 µF/mm² 0.5 µF/mm²

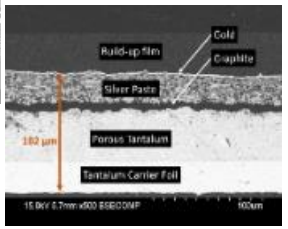
Ultra-high surface area silicon 1-2 µF/mm²

Multilayered dielectrics on deep trench

IVR; Embedded PoL 1-20 MHz

Embedded capacitors Panel

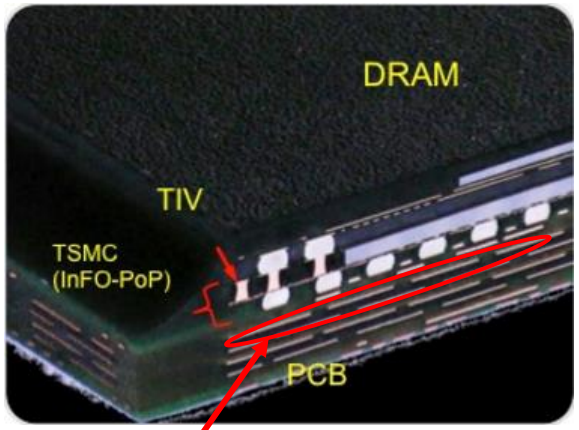


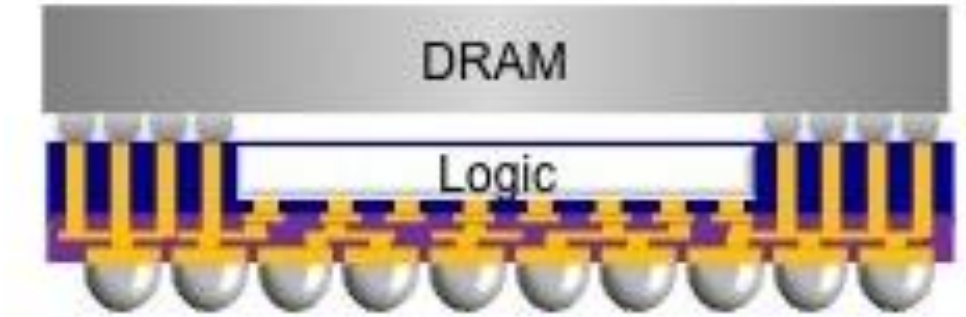


Adv. Nanotech. >3 µF/mm²

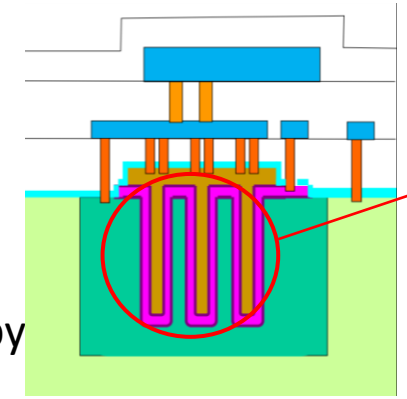
Deep Trench Land-Side Inserted Si Capacitors (TSMC)

Land-side on-Si capacitors for integrated fan-out packaging

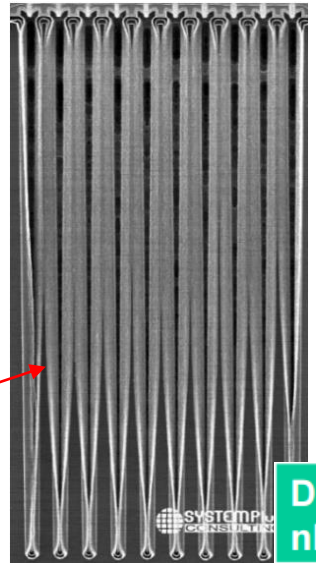




1 × 0.5 mm footprint Located underneath info-POP supported by extra PCB layer



Deep trench capacitor structure



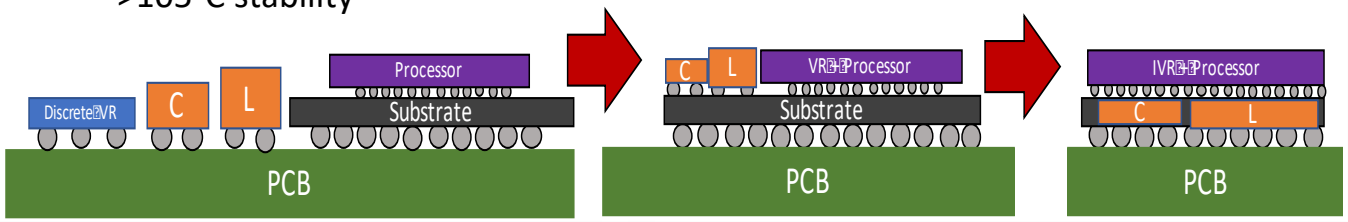
- Up to >500 nF/mm^2 density
- Superior VCC and TCC
- Comparable ESR to MLCCs
- Thickness as low as 100 µm

Density, nF/mm2	Breakdown Voltage, V	TDDB, V	Max Voltage rating, V
180	16.1	7.0	4.5
250	14.3	6.8	4.2
500	6.5	4.5	3.2
600-700	4.0	3.8	2.5-1.2

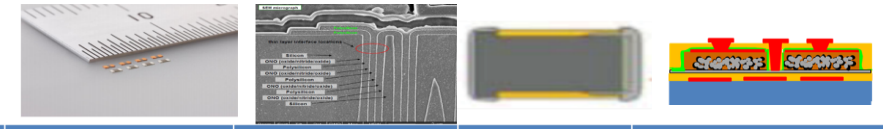
High-Density Capacitors for Integrated Voltage Regulators

Objectives

- Ultra-high density capacitors:
  - >1 µF/mm² at 1 MHz,3-48 V, & 50 mΩ ESR
  - 1 nA/µF leakage current
  - Simpler processing on wafer or package
  - 100 µm thickness
  - >105°C stability

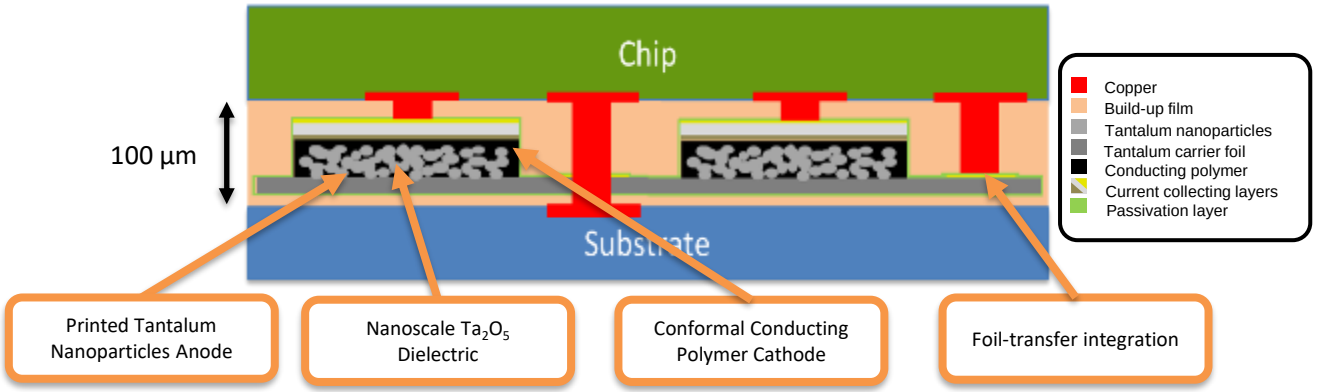


Prior Art



	MLCC	Trench Caps	Ta Chip	Emerging Need
Volumetric Density	20 µF/mm³	1 µF/mm³	~10 µF/mm³	50-100 µF/mm³
Thickness	100 µm	100 µm	600 µm	50-100 µm
Freq. Stability	10-100 MHz	>1-10 MHz	0.2 -1 MHz	>10 MHz
ESR	~10 mΩ	50 mΩ x µF	>100 mΩ x µF	~50 mΩ x µF
% ΔC/V	-13 % to -70% (1 to 4 V)	~ 0 %	~ 0 %	~ 0 %
Max. Temp	85° C	150° C	125° C	>125° C
	PICK AND PLACE			FILM EMBEDDING WAFER OR PANEL INTERCONNECTS

Unique Approach



Printed Tantalum Nanoparticles Anode

- High-surface area at ultra-thin form-factor
- Scalable to any design need

Nanoscale Ta_2O_5 Dielectric

- Paraelectric for DC bias and temperature stability
- Amorphous for low leakage current

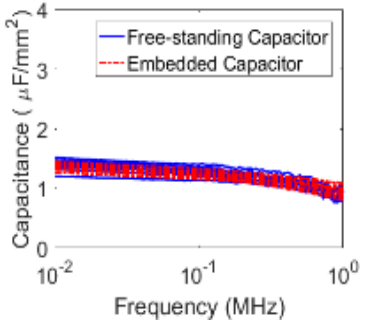
Conformal Conducting Polymer Cathode

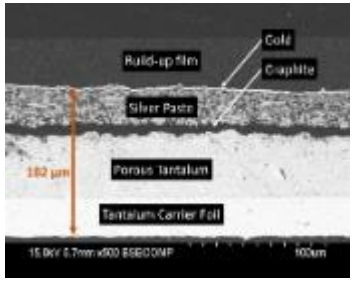
- Low-resistivity and thick coating for low ESR
- Self-healing for low leakage current

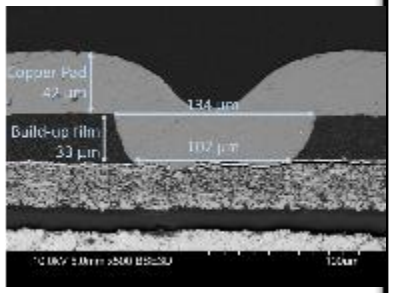
Foil-transfer integration

- Thin-film lamination
- Ultra-short copper interconnections for reduced impedance
- Low-cost, panel-scale, 3D approach

Major Accomplishments

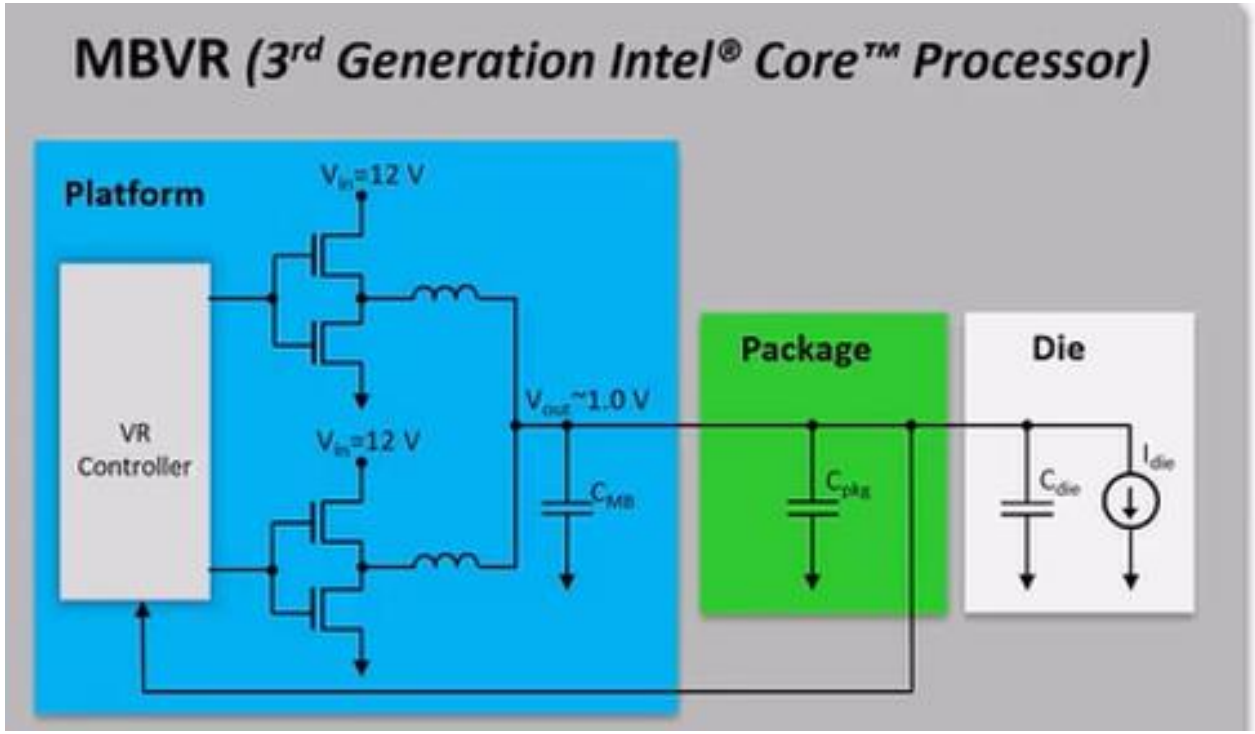


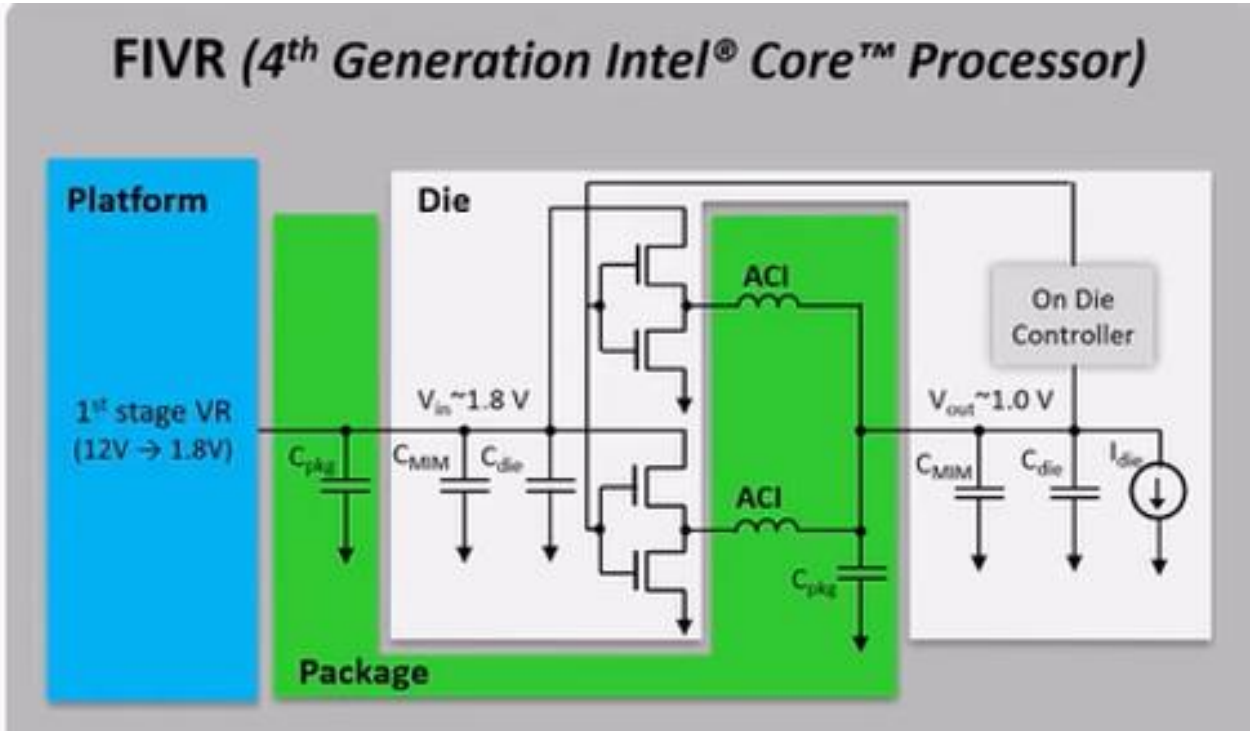




>1µ F/mm² up to 1 MHz at 5 V with low ESR, low leakage current, and 100 µm component thickness

Integrated Power Delivery in the Package
Key for High-Performance in Computing





Previously Voltage regulator is designed on the PCB

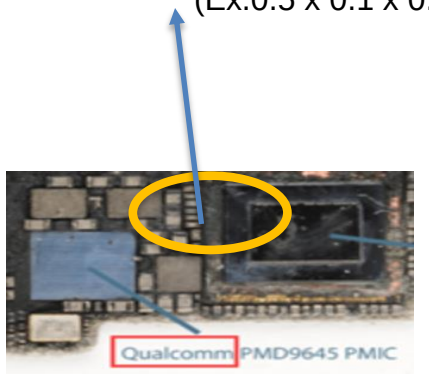
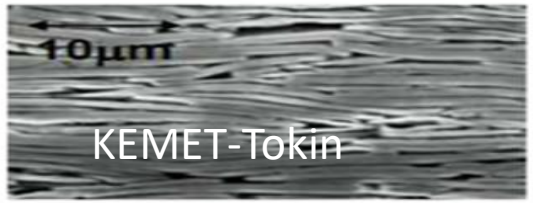
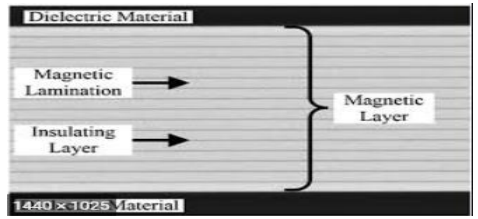
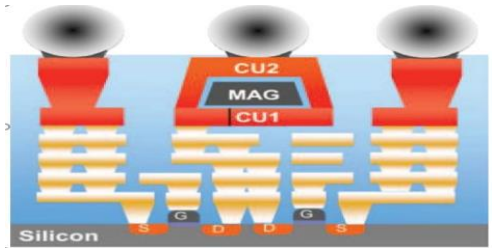
Few filter capacitors in package

Now, Voltage regulator is moving into the package

More filter capacitors moving into the package

Intel, ECTC 2020

Inductor Technologies

	Discrete (Ferrite or Metal powder)	Magnetic composites –substrate-embedding	Nanomagnetic films: On-chip	Need
L/Rdc nH/milliohm	15-25	5-10	0.1-0.2	>>10
Q	>20	<10	5	>20
Current-handling A/mm2 Thickness	0.01 – 0.1 200- 500 microns	0.1 – 1 50 - 200 microns	5-10 A/mm2 25 microns	5-10 A/mm2 25-50 microns core
Cost	Low	Low	High	Low
	Discrete (Ex.0.5 x 0.1 x 0.5 m 	  Substrate-embedded inductors Magnetic Core (0.5 - 0.6 mm)	  Intel and Ferric	

FIU FLORIDA INTERNATIONAL UNIVERSITY

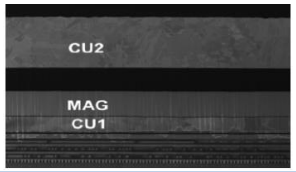
Prior Art- Inductor Integration

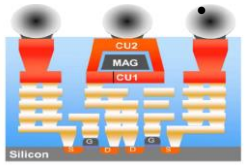
Fe

On-Chip IVR

Monolithic integration
- Magnetic-core inductor
  - CoZrTaB
  - Ms: 1.5 T
  - Hc: 0.39 Oe
- Switching frequency
  - 80 to 100 MHz
- Inductance
  - 300 nH/mm^2

- Peak Q Factor > 20 @ ~100MHz
- Peak Inductance Density ~300nH/mm2
- L/RDC >200nH/Ω for L > 100nH
- L/RDC of 120nH/Ω for L ~ 10nH
- Current Density exceeding 12A/mm2 for coupled inductors
- Saturation Current exceeding 1.5A for single inductors
- Cross wafer inductance variability σ < 3%
- Other Devices in development: Transformers, improved inductor designs

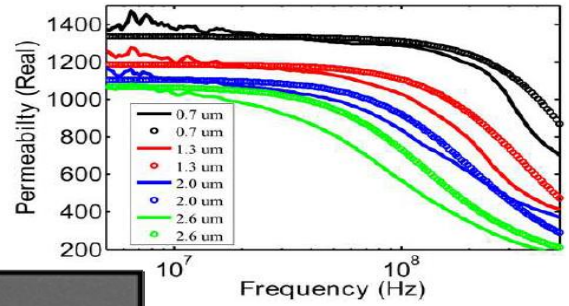


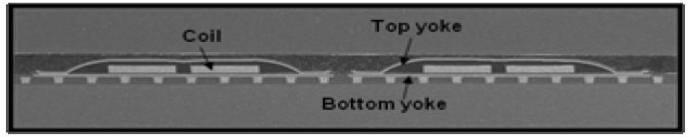


On-Chip IVR

- Monolithic integration
  - Magnetic-core inductor
    - $Ni_{45}Fe_{55}$
    - Ms: 1.6 T
    - Hc: 0.2 Oe
  - Switching frequency
    - 50 to 200 MHz
  - Inductance
    - 130 nH/mm^2

IBM

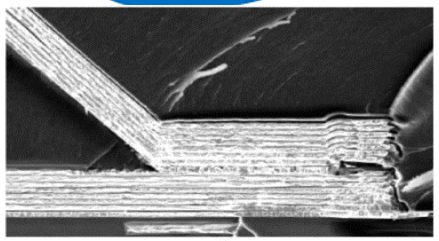


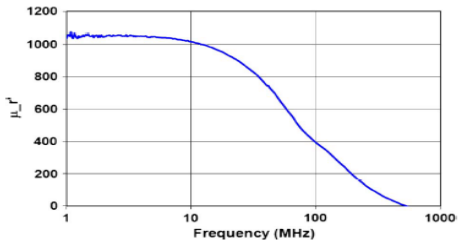


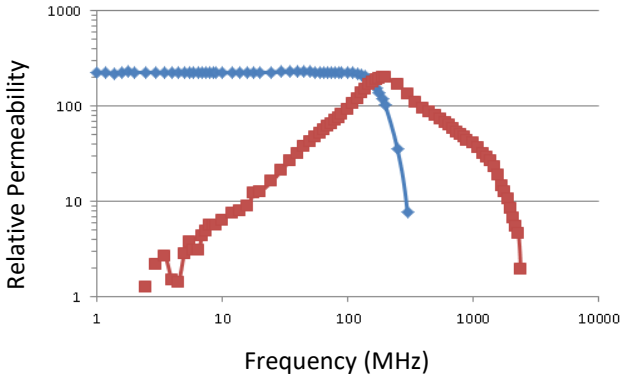
On-Chip

Monolithic integration
- Magnetic-core inductor
  - $Ni_{80}Fe_{20}$
- Switching frequency
  - 30 MHz to 140 MHz
- Inductance
  - 17 nH
- 16 inductors in 2.8 mm^2
  - Inductor size: 0.17 mm^2
- Current: 1.5 A

intel





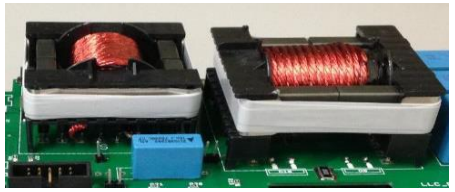


- Material sample thickness = >40um
  High deposition rate – high throughput and low cost
  IC or glass substrate- compatible
  Deposition thickness capability up to 50um
  μ_r= 200, Bsat= 1.3 T, Q @ 5 MHz>90, Q@ 20 MHz=30
  0.5 microhenries; Isat of 2 Amp on 6 inch;
  Toroid and solenoid inductors

Georgia Tech PACKAGING RESEARCH CENTER

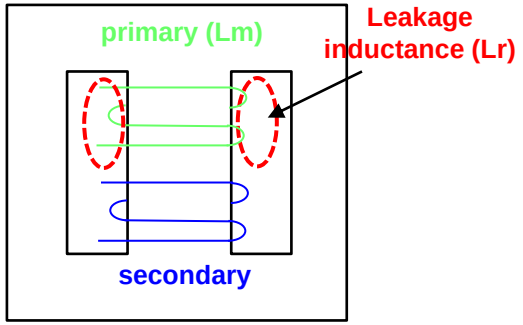
Magnetic Components: Integration

- Planar transformers with windings implemented on PCB are gaining momentum in R&D and production

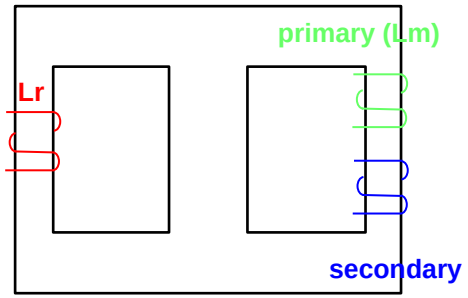
Component	Method	Conventional Wire-wound	Wire-wound integrated	PCB winding planar core
	Structure	 [1]	 [2]	 [3]
	Power	3.3kW	192W	5 kW
	Profile	> 45 mm	> 30 mm	20 mm
	Leakage inductor	Discrete	Integrated	Integrated
	Process	Manual (Litz wire)	Manual (Litz wire)	Thick Cu PCB
	Repeatability	Low	Low	High

- Monolithic integration of transformer and inductors on single core to minimize part count

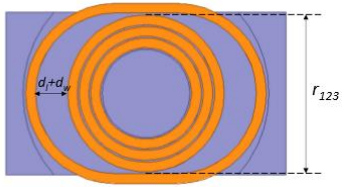
Transformer + inductor



Additional winding

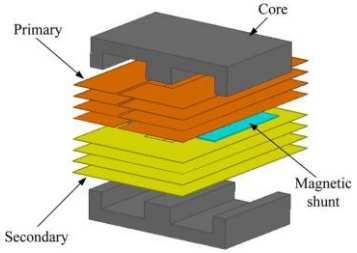


Air gap control



Source: Virginia Tech, APEC 2015

Magnetic shunt insertion



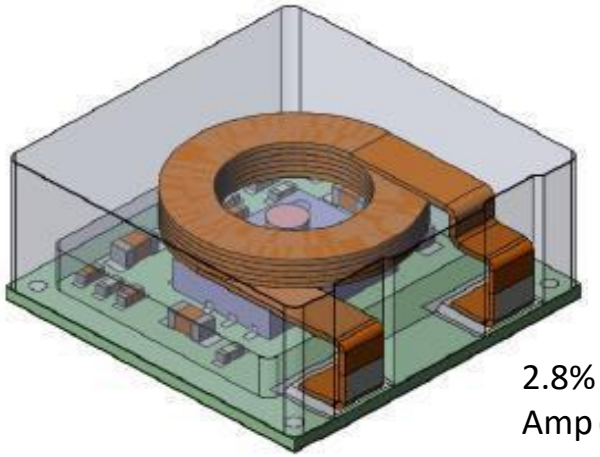
Source: NUI Galway

Haksun Lee, GT

Medium Frequency – Medium Power: Inductor Advances

sumida

PSI2: Inductor in package molding



Better thermal, shielding,

High current-handling and efficiency

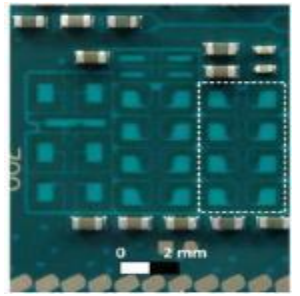
2.8% increase in efficiency with 3-5 Amp current

Package IVR: Integrated Voltage Regulator

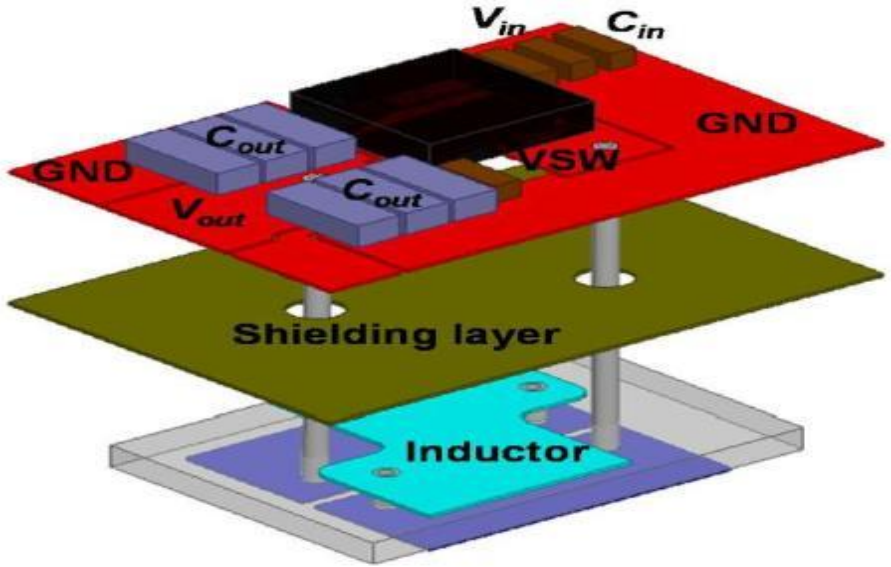
intel

Inductors integrated in substrates

- Air-core inductors
- Multiple domains
  - High-current: >20 A
  - Medium-current: 5-20 A
  - Low-current: <5 A
- Switching frequency: 140 MHz



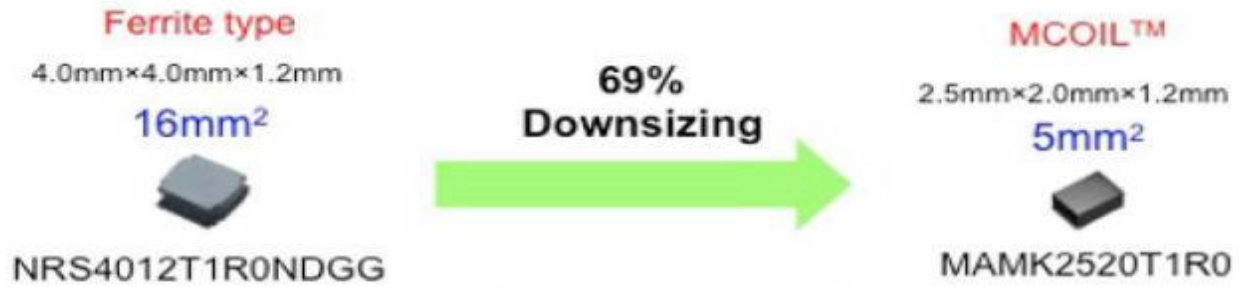
Virginia Tech: Inductor in PCB Substrate



PCB-embedded ferrite and metal flake composites

TAIYO YUDEN

Inductor in package



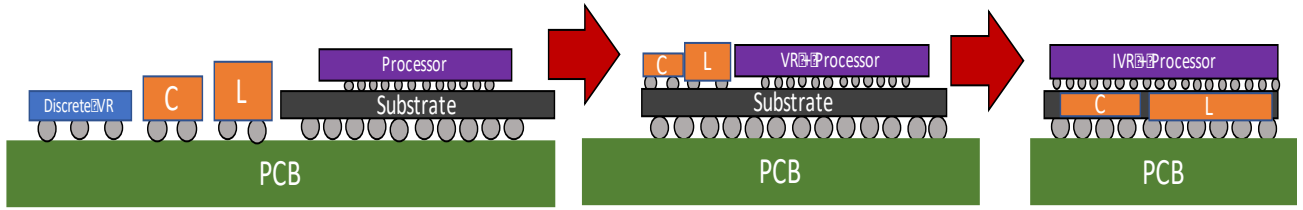
4X increase in current-handling with metal compacts compared to ferrites

High-Density Embedded Inductors for Integrated Voltage Regulators

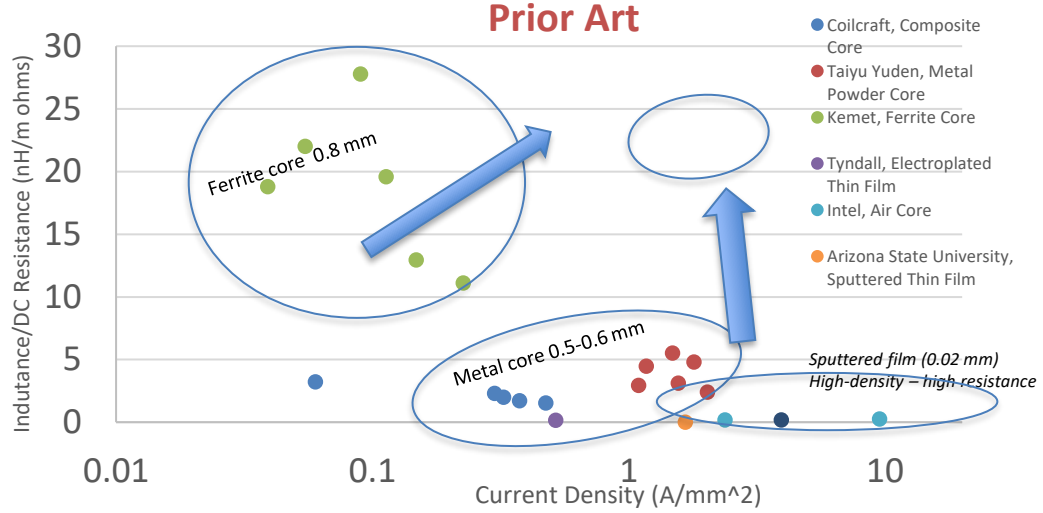
Objectives

- Embedded inductors for power converters:

Target
20 nH/milliohm
2 A/mm2
20-50 microns

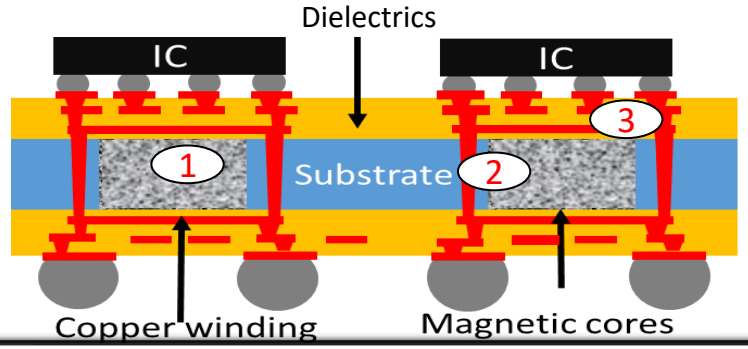


Prior Art



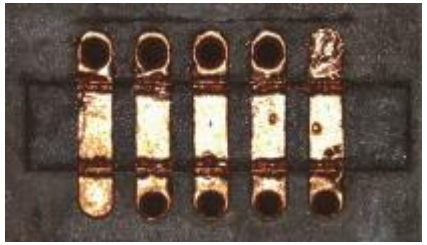
Unique Approach

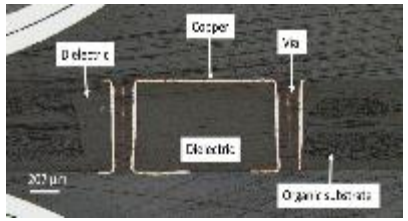
1. Substrate-compatible magnetic composites with high permeability
   - High permeability for high-inductance density
2. Embedded solenoid inductors
   - Embedding for miniaturization
   - Design for high-current density
3. Substrate design rules to fabricate thick copper
   - Low resistance

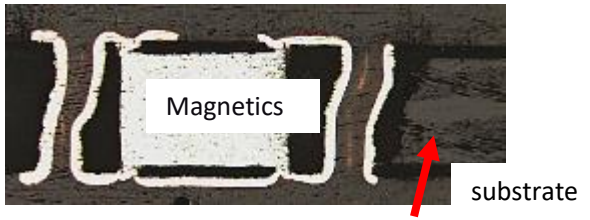


Major Accomplishments

- Embedding of high current density and high-efficiency inductors embedded in organic substrates. Current status:
  - Thickness: 500 um
  - Inductance: 8nH/mm^2,
  - Current: Projected to 1 A/mm^2
  - Resistance: projected to <10 m Ω







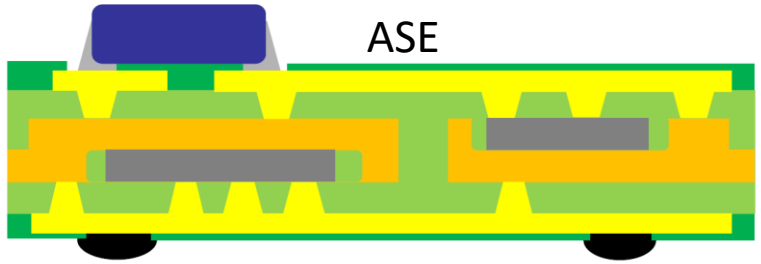
3D Power Packaging

- Multiphysics converter design (topology & hardware co-design)
- Advanced GaN devices & high-temp passives

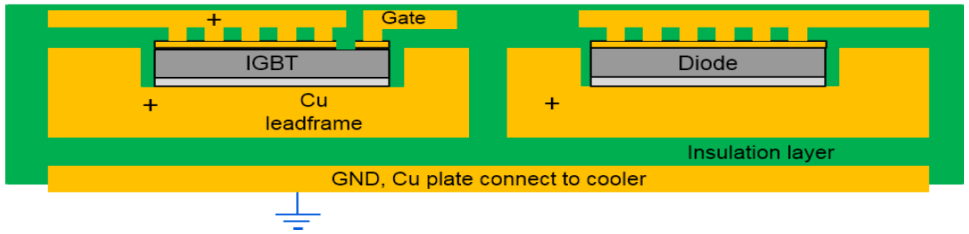
- Structure and process innovations
- Doubleside wafer plating
- Panel-scale embedding of power devices
- High-temperature materials with enhanced interfaces for Hi-Rel

Infineon

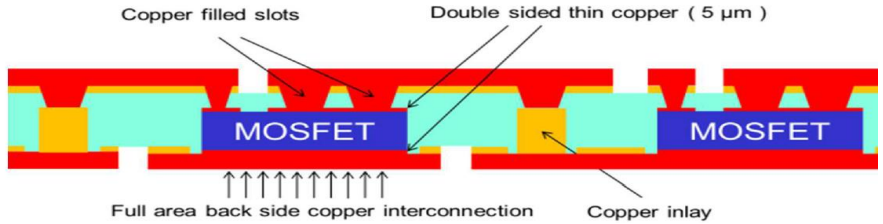
ASE



Schweizer



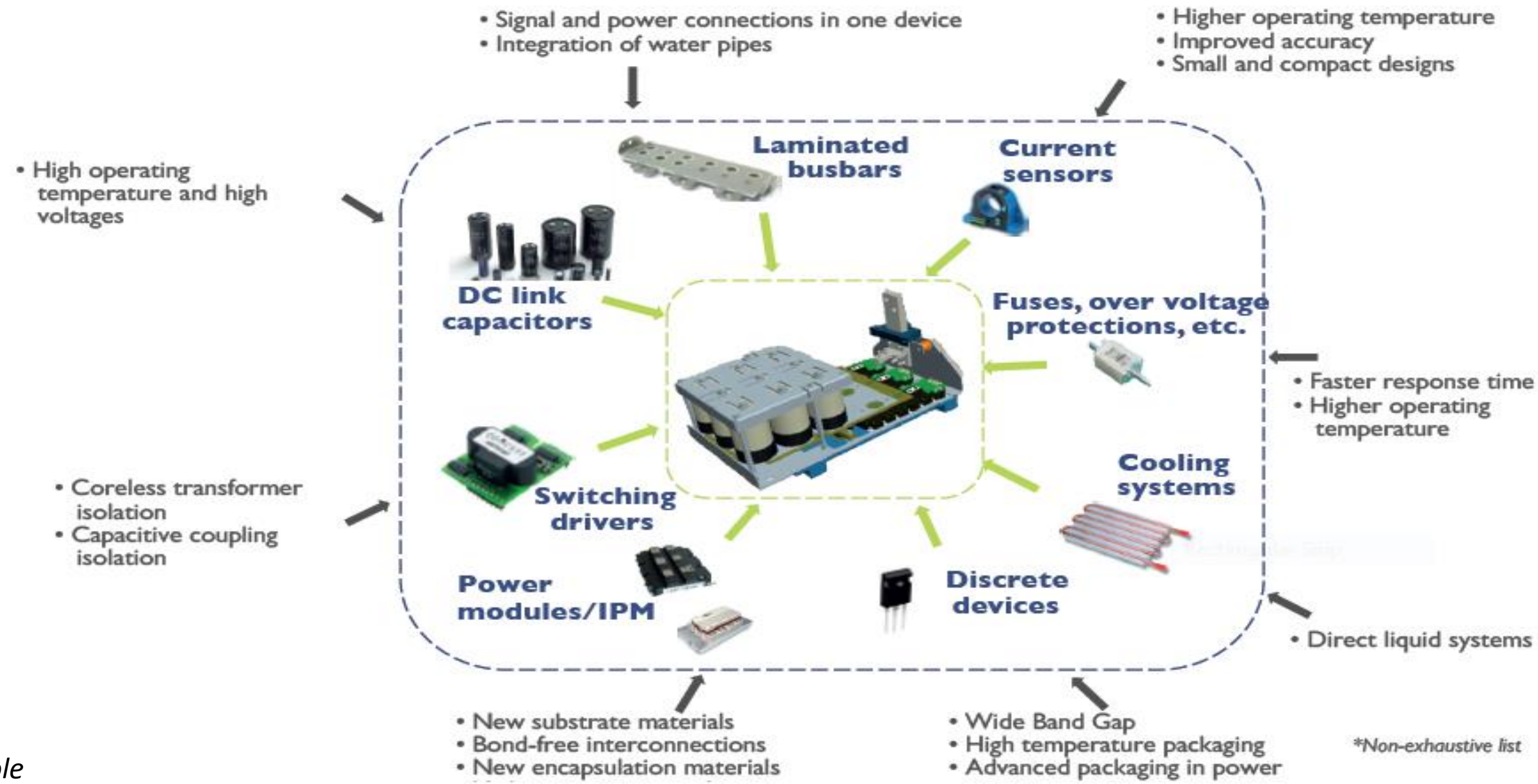
AT&S



- Sintered copper interconnections between devices, IMS or leadframe and PCB
- Barriers for oxygen and moisture
- Advanced encapsulants

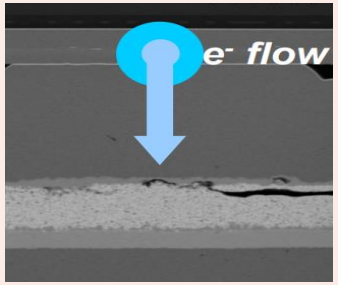
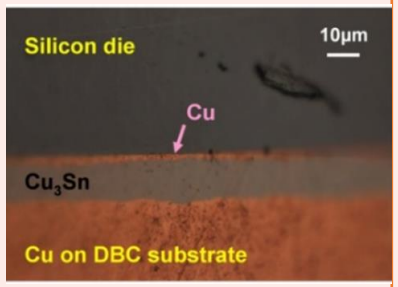
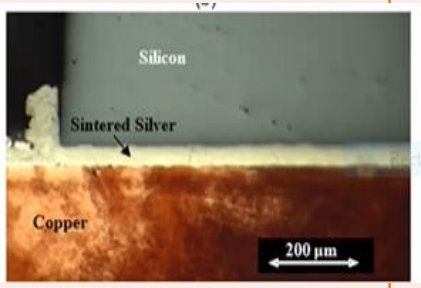
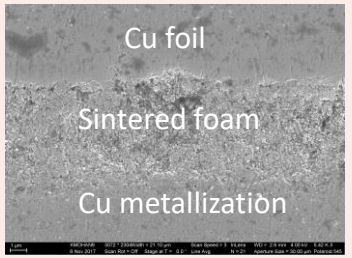
- Advanced cooling loop with temp uniformity
- System-level thermomechanical and electrical reliability:

Improvement trends* for different system components



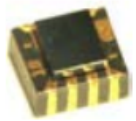
Yole

Evolution of Die-Attach Materials

	High-lead solders	Transient Liquid Phase Sintering	Nanosilver	Nanocopper	Nanocopper-microwire-graphene multilayers
	 Koduri, Texas Instruments Current is not needed for lateral GaN die-attach)	 Infineon	 Jiang Li (TI, Virginia Tech)	 Vanessa Smet, Georgia Tech	
Pressureless assembly capability	Pressureless		Requires pressure	Requires more pressure	Pressureless with reactive nanosurfaces
Electrical and thermomechanical reliability performance	Moderate with low homologous temperature	Moderate with kirkendall voids	Microstructural instabilities and diffusion	Die shear strength is low with smooth backside metallization	
Safety	Lead-based				
Cost			High	Moderate	Low, because of design and process flexibility

Low Power (Consumer Electronics) to High Power

1.2W , 900W/in^3



2MHz

Micro power module

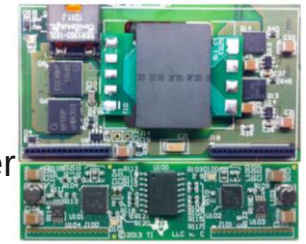
Consumer

10W , 350W/in^3

780kHz

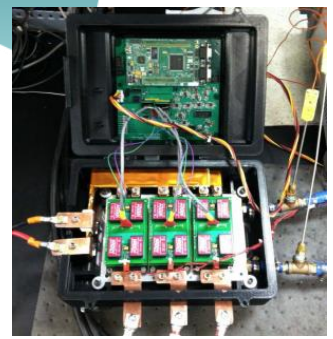
Step down converter

500W , 308W/in^3



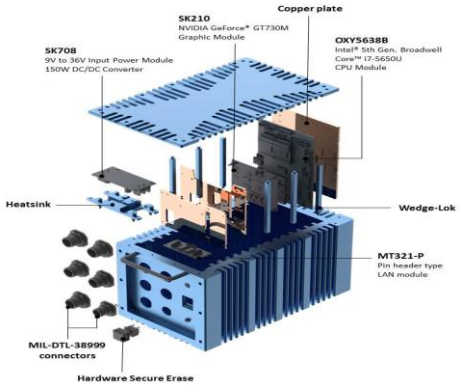
GaN DC-DC converter

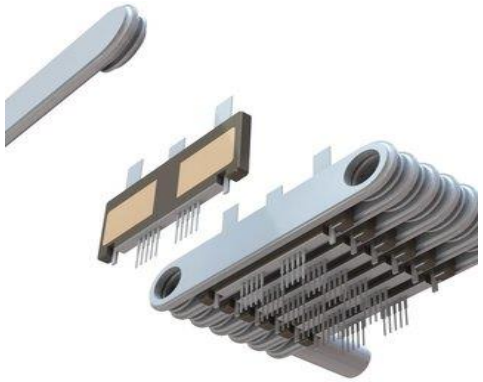
30kW , 81W/in^3



30kW all SiC inverter

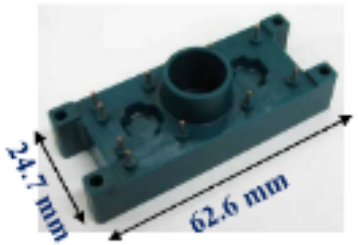
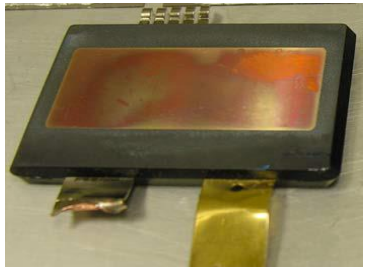
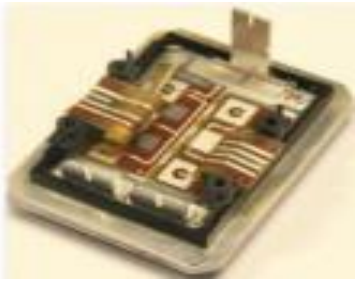
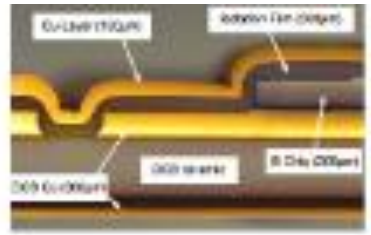
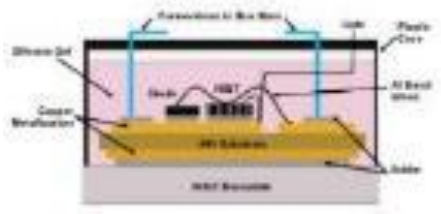
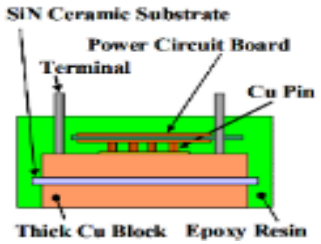
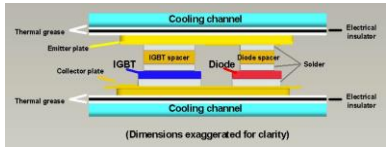
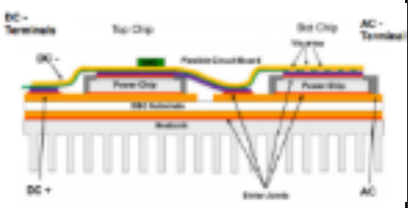
High Power





- Higher frequencies
- Higher power densities
- More integration
- Single package solutions

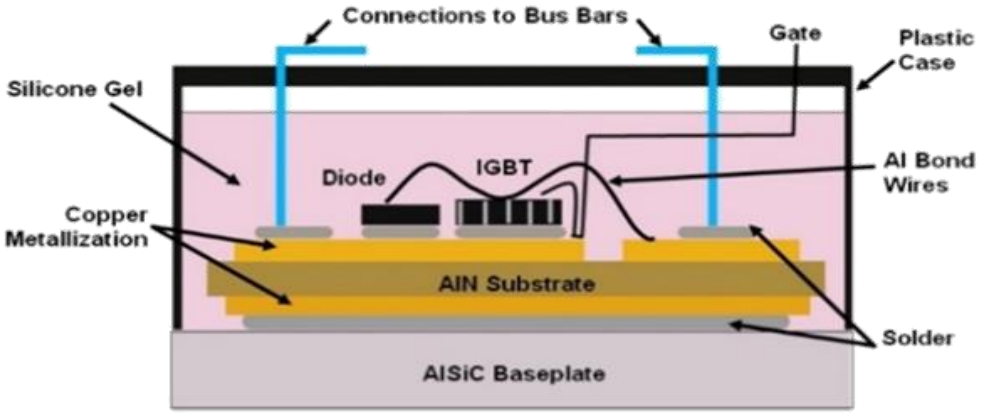
High-Power Packages – Leading-edge Products

Package	Standard wire bond package	Cu pin interconnect w/ thick Cu DBC	Double-sided liquid cooling	Cu traces on flexible foil w/ sintered joints	Planar interconnect using Cu plating
	Conventional	Fuji Electric	Denso	Semikron SKiN	Siemens SiPLIT
Package structure					
Cross-section					
Parasitic inductance					
Thermo-mechanical					
Note	• Wire bond • Solder die attach	• Cu pin joints • Gel replaced with epoxy	• Double sided cooling • Double DBC	• FPCB Gate drive integrated • Ag sintered joints	• Area joints by Cu electroplating

Not Available | Very bad | Bad | Good | Very Good

Haksun Lee, GT

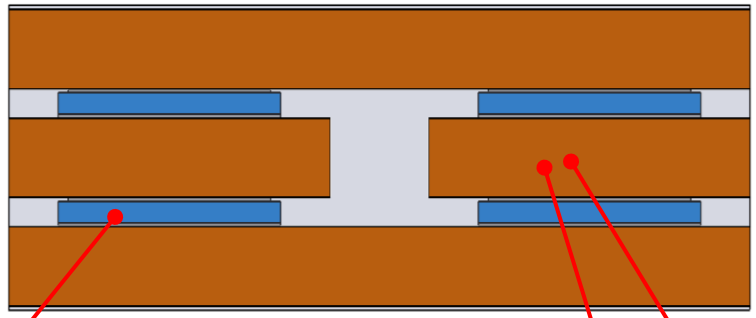
Traditional to 3D Power Packaging



- Reliability challenges with nanocopper and nanosilver
- Thick packages
- Large electrical inductance and high thermal resistance

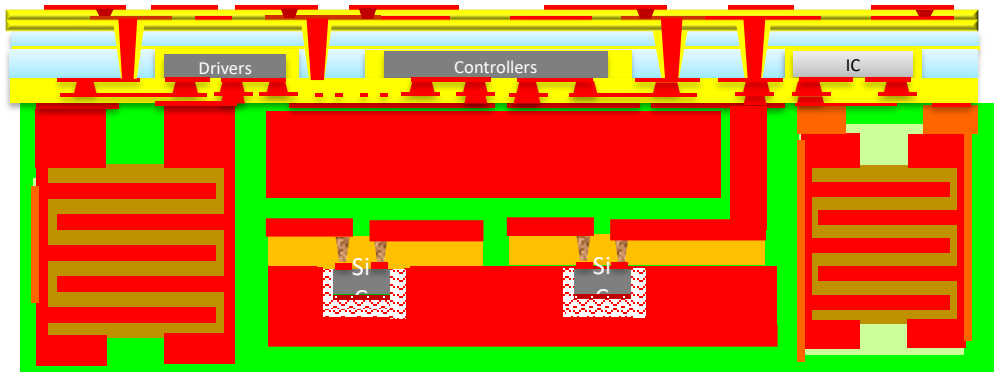
Leadframe Fan-Out Packaging

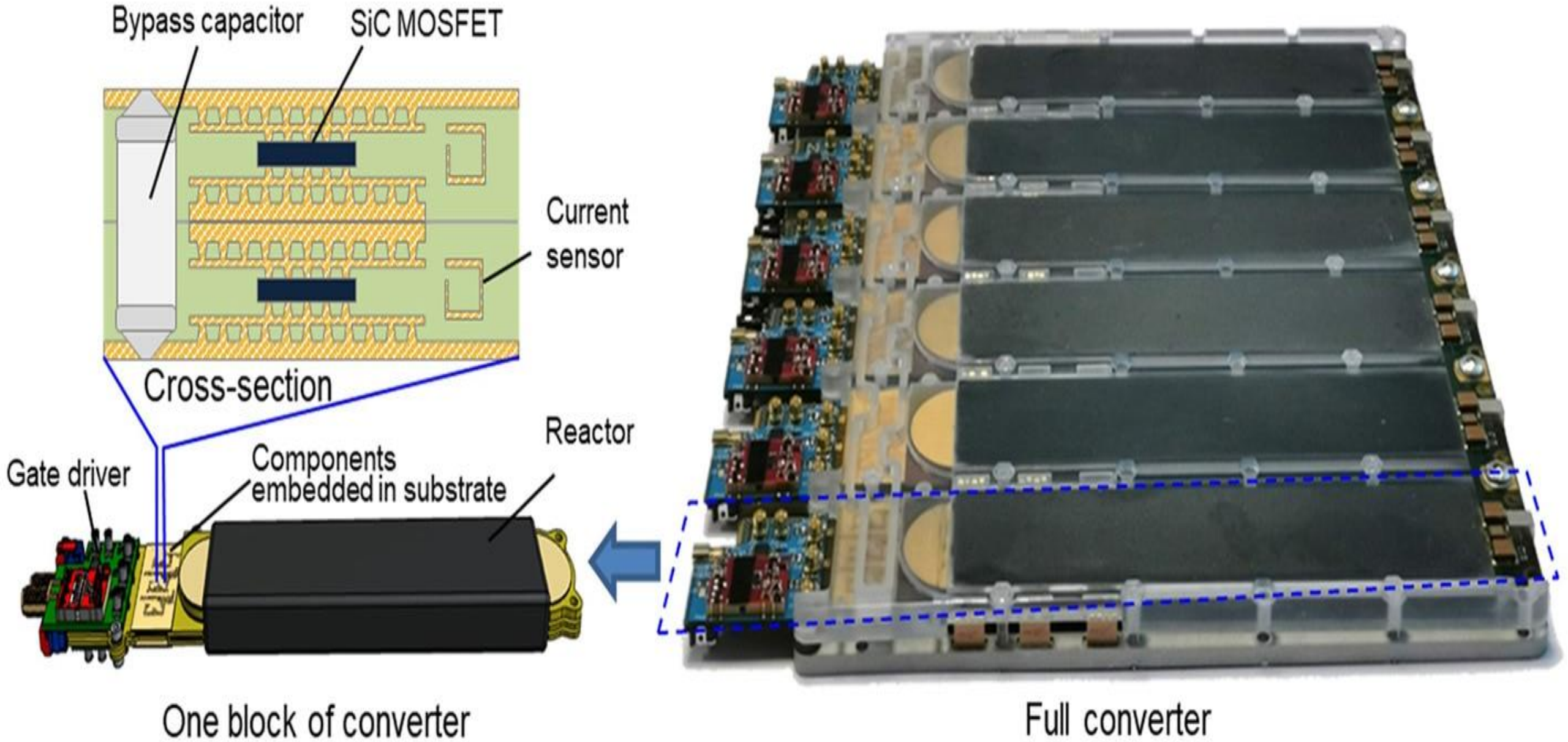
- **No reliability challenges with nanocopper**
- **(Bonding layers are in compression)**
- **Thin packages**
- **Lower electrical inductance and thermal resistance**



Heat generation
100 W

Heat transfer coefficient
10,000~50,000 W/m^{2}K

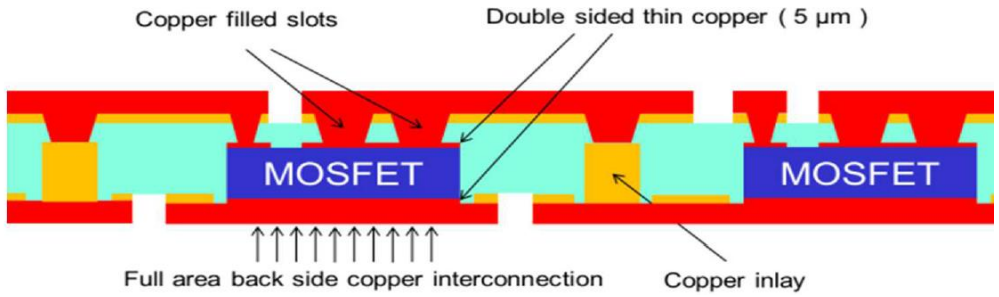




Mitsubishi Electric

3D Power Packaging: AT&S and GaN Systems

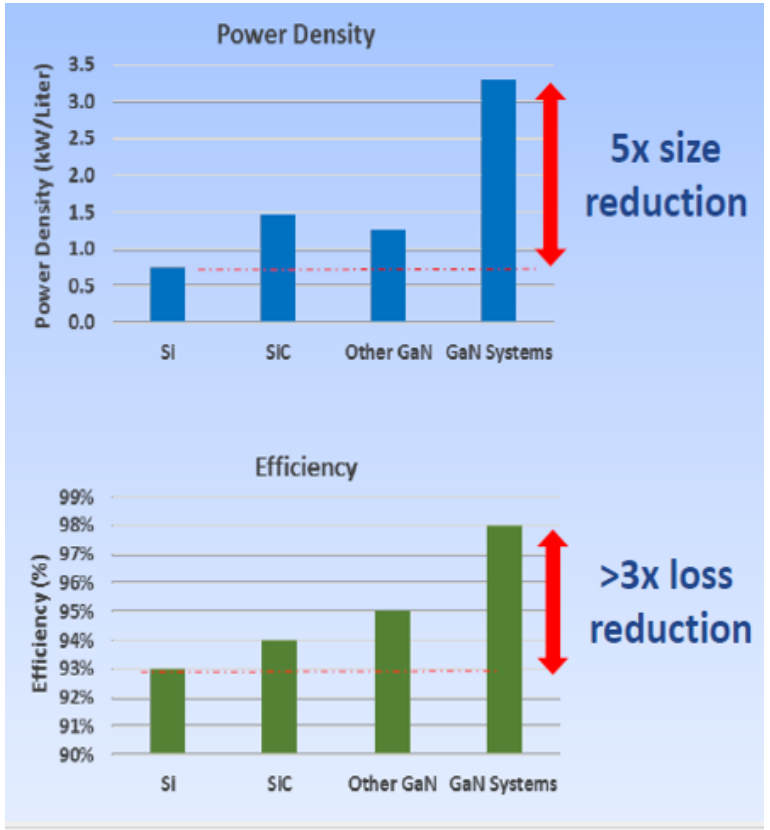
AT&S



- Planar Surface-embedded components (PARSEC)

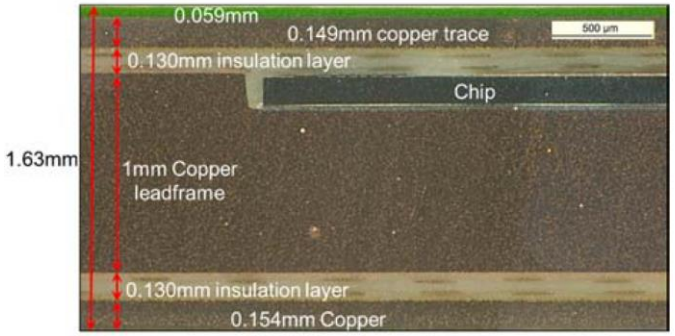
- 250-450 V; 200 A: 50 kW inverter
- IMS PCB with thermal-conducting prepregs
- Better partitioning, faster switching, reduced switching losses

GaN Systems
7 KW, Level 2 EV Charger



3D Power Packaging - Schweizer

- Thick lead-frame heat-spreader with cavity for die placement
- Laser-drilled and plated-vias for top interconnect on top side (logic integration possible)
- Power embedded PCB offers improved electrical, thermal performance with increased power density



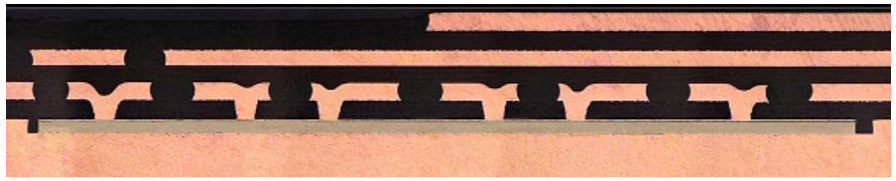
Kearney et al., ABB Corporate research

- Improved switching behavior
- Reduced losses
- Optimized heat dissipation
- Control & power co-integration

P2Pack Half-bridge with embedded shunt:

- No die-attach reliability concerns
- Laminate temp: 175-220 C
- 38% reduction in losses for power PCB
  - Over 100-500 Amp

- 50% improvement in performance
- 4.5-9W ; 3-5 K rise in temperature;
- 0.05 -0.1 milliohm resistance



Reliability Challenges

- Cracking of thick vias
- Dielectric cracking at stress-intensive points

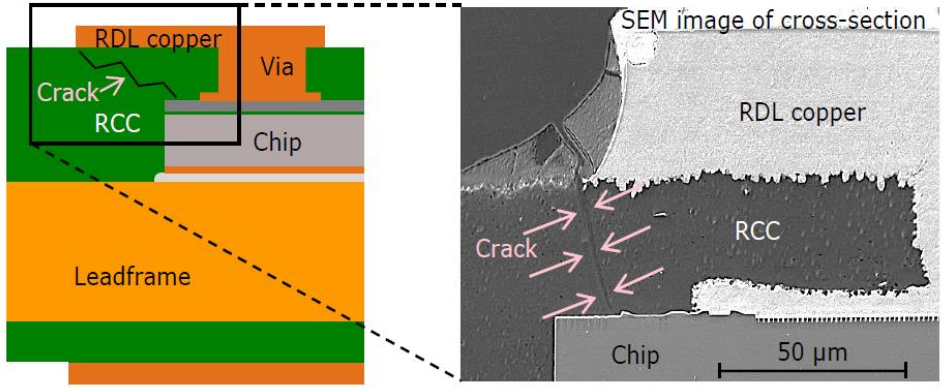
- Partial discharge:
  - 41-50 kVrms/mm before aging
  - 32-36 kVrms/mm after aging

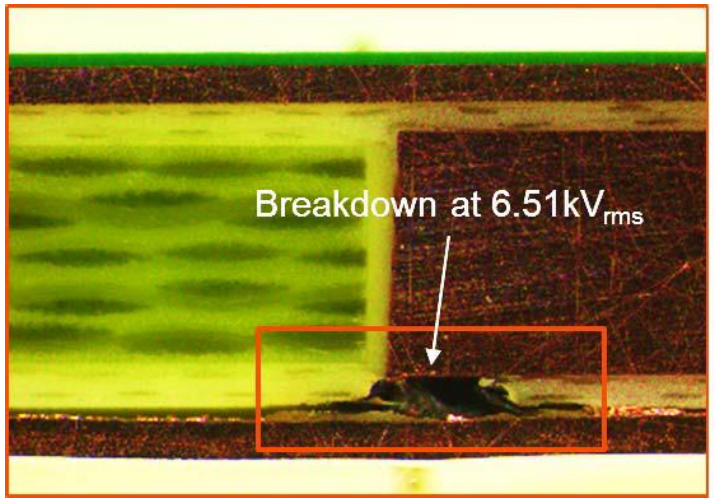
  Lifetime = C/E^n

  n = 10-11

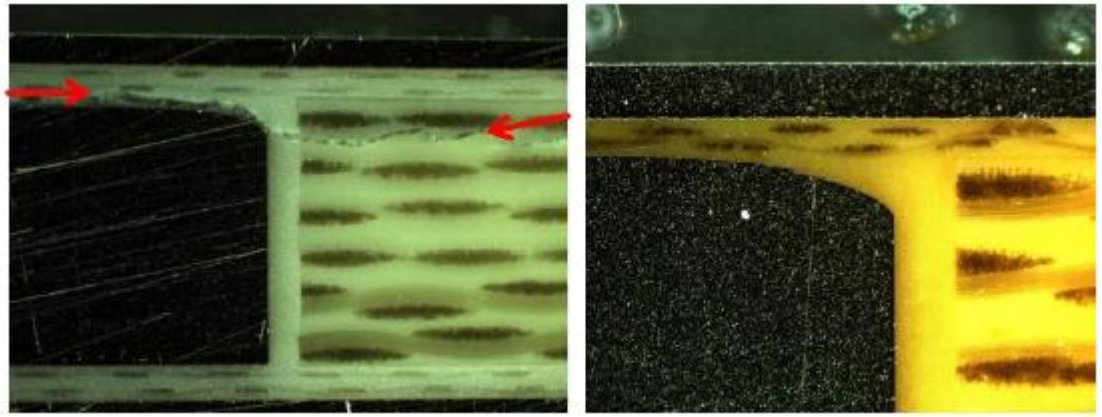
  n = 14-16

Infineon power module (low CTE, high Tg, high fillers or fibers





ABB/Schweizer
Example of electrical breakdown at high fields

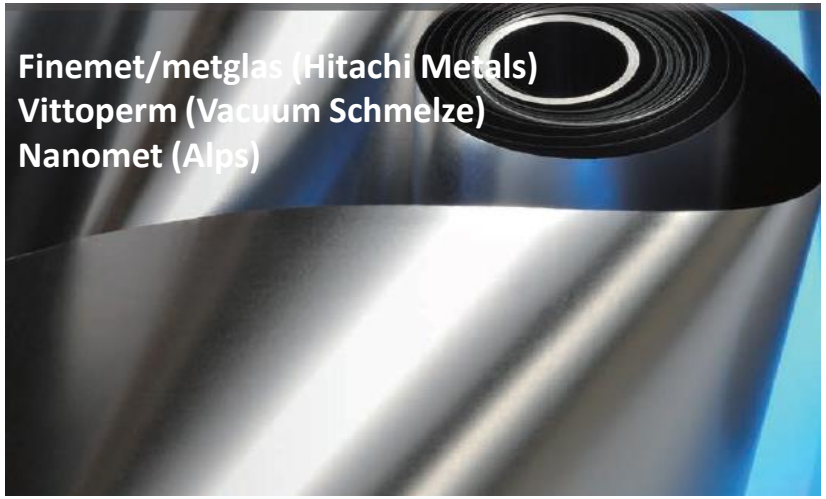


Bosch/Schweizer/Isola
Resin cracking in standard resins (left), no cracking with advanced epoxies

Low-Frequency - High-Power Magnetics

- Ferrite 3C90:
  - 500 kHz: 0.1 T peak; 700 mW/cc;
  - 1 MHz; 0.02 T; 70 mW/cc;
- Ferrite 3F5 MnZn:
  - 1 MHz; 0.02 T; 30 mW/cc
- Sumida's ferrite:
  - 1.5 MHz; 0.02 T; 37 mW/cc
  - 1 MHz; 0.02 T; 70 mW/cc;
  - 200 kHz; 0.1 T; 250 mW/cc

Nanocrystalline films

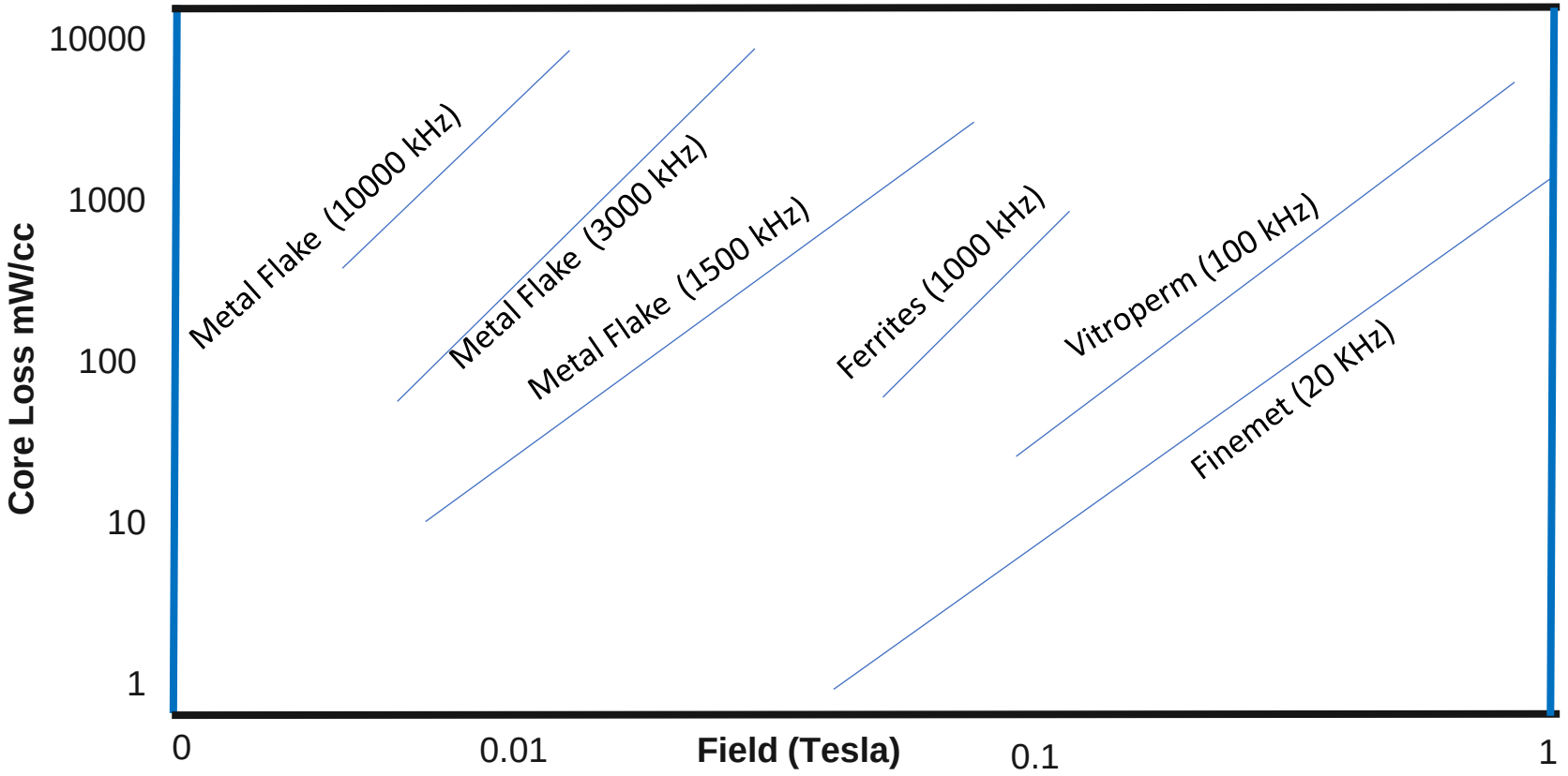


Vitrovac (Co_{67} Fe_4 B_{11} Si_{16} Mo_2) amorphous flakes:
100 kHz; 0.1 Tesla, 30 mW/cc;
100 kHz; 0.2 Tesla: 200 mW/cc;

Hitachi metals: Finemet - FT-3L and FT-3M:
20 kHz; 0.1 Tesla; 2 mW/cc
20 kHz; 0.2 Tesla; 15 mW/cc
20 kHz; 1 Tesla; 300 mW/cc

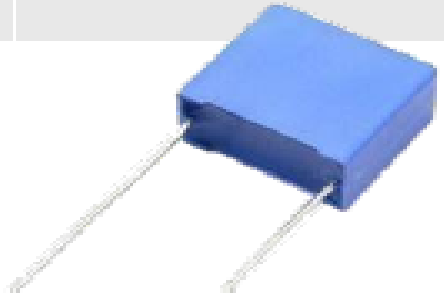
Permeability of
10,000 to 100,000
20 kHz x 50 mT << 500 W/cc

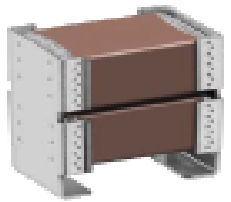
Ms: 1.5 – 2 Tesla;
1-5 A/m of Coercivity
<100 kHz

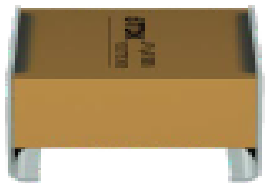


Comparison of DC capacitors of nominal 1µF/400V_{op}

	MKP film capacitor	BTO Class 2 MLCC (e.g. X7T)	CeraLink™
Nominal / rated capacitance	100 %	100 %	100 %
No bias voltage 0.5 V_{RMS}, 25°C	100%	100 %	35 %
DC link voltage 0.5 V_{RMS}, 25°C	100 %	35 %	60 %
DC link voltage 20 V_{RMS}, 25°C	100 %	35 %	100 %
Typical capacitance density @ DC link voltage 20 V_{RMS}, 25°C	0.7 µF/cm³	2.5 µF/cm³	★ **4.9 µF/cm³**
Typical current rating per capacitance @ 100 kHz, 105°C	<1 A/µF	<4.5 A/µF	★ **12 A/µF**







Heterogeneous Integration with Nanopackaging

- Power delivery in computing systems
  - Integrated voltage regulator: power conversion closer to the load
  - Capacitors and Inductors: >10 MHz; Impedance < 1 milliohms
- Medium-power packaging
  - Integrated copper carriers
  - Embedded-die packaging with die-attach materials: Silver to nanocopper
  - High-temperature organic packaging
- High-Power packaging:
  - Doubleside cooling, lower parasitics
  - High-voltage passives: 1000 V, planar and higher power densities

FIU
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