IEEE 30TH INTERNATIONAL SYMPOSIUM ON THE PHYSICAL AND FAILURE ANALYSIS OF INTEGRATED CIRCUITS (IPFA)

24 JULY 2023 - 27 JULY 2023 | BAYVIEW BEACH RESORT, BATU FERRINGHI, PENANG

CALL FOR PAPERS

IPFA 2023 is devoted to the fundamental understanding of the electrical and physical characterization techniques and associated technologies that assist in probing the nature of wear-out and failure in conventional and new CMOS devices. The Technical Program Committee is inviting papers related, but not limited to, the following areas:

Package-Level Failure Analysis: Wire-bond, 2.xD/3D/SiP package FA, wafer & panel level, IC / acoustic applications, 2.xD/3D X-ray, TDR, EOTPR, Lock-in thermography, FTIR, material analysis.

Product Test and Diagnostics: Embedded BIST and DFT test and diagnosis, reliability testing, defect-oriented testing, protocol-aware testing, Test-to-Design feedback, mixed signal and analog tests, silicon failure debug by test and yield engineering methodologies, yield analysis and optimization.

Sample Preparation, Metrology and Defect Characterization: Device de-processing, Ion beam / TEM sample preparation, Metrology, Defect inspection.

Case Studies on Fault Isolation: Die / Board / System-level physical FA, Design for manufacturing, Construction Analysis, Reverse engineering.

Case Studies on Physical Failure Analysis: Die / Board / System-level physical FA, Design for manufacturing, Construction Analysis, Reverse engineering.

Advanced Electrical Fault Isolation Techniques: Advanced methodologies in photon and laser-based microscopy techniques, Advanced sample thinning, Dynamic techniques, Magnetic imaging, Nanoprobing, AFP, EBAC/EBIC, scan chain diagnosis, next-generation backside power-rail imaging.

Advanced Physical Failure Analysis Techniques: Advanced methodologies in PFA, Advanced optical/Ion beam approaches, Plasma/Laser FIB, Spectroscopy (EDX / EELS / SIMS) techniques, Scanning probe microscopy, Circuit-edits, De-layering recipes and innovations, Tomography.

Hardware Assurance: Semi-Invasive and Invasive Analysis for attack of encryption system, Die-Level Reverse Engineering, Counterfeit Electronics Detection, Hardware Trojan localization.

FPGA, Reconfigurable Computing, Embedded system, system-on-Chip (SoC) Validation and Pre-Silicon Debug: Application, Architecture, Hardware Description Language (HDL) coding, Hardware/Software co-design, Power Efficiency, Real-time System.

VLSI Design on Analog, Digital, RF, Sensor, MEMS and Post-Silicon Debug: bio-sensors, bio-electronics, RF design and validation on test chips, MEMS and MOEMS, microwave devices & 5G circuit.

Photonic Devices (Display, Lighting and Photovoltaic) Reliability and Failure Analysis: LED, OLED, GaN on GaN, Solar cells, CdTe, CIGS, organic materials, multi-junction, perovskite etc., Degradation studies on display modules, Infrared photodetectors, TFT, Waveguides, Transceiver, Optical-IO devices.

Transistor and Non-Volatile Memory Reliability: Gate oxide/High-κ reliability, PBTI/NBTI, Hot carrier, Random telegraph noise and single dopant effects, Self-Heating in sub-5 nm CMOS, GAA FET / RFSOI/ HBM/stack DRAM device reliability, Process and stress-induced reliability issues and variability, Non-volatile memory reliability (PCRAM, RRAM, STT-MRAM, Ferroelectric devices, MRAM), 2D material, device reliability, and yield.

High Power Electronics / Wide Bandgap Device Reliability & Failure Analysis: Reliability of devices based on GaAs, GaN, SiC and Ga2O3 systems, IGBT, Thyristor, Wide Bandgap, Power Electronic System, Trap-related degradation, Materials-related defect characterization, Process variability, III-V/Si integration.

AI for Failure Analysis and Reliability: Artificial intelligence (AI) for FA – fault detection, Visual / image analytics, Pattern recognition, Signal Processing, Machine learning for prognosis and reliability. Exploring reliability assessment and quantification for new applications (e.g. neuromorphic devices and AI accelerator).

ESD, Latchup, Interconnect and Packaging Reliability: Component and system level ESD design: modeling and simulation TDDB dielectrics, Electromigration, stress migration, cracking, corrosion, and fatigue in bond pads, Reliability of 3DIC / TSV / MEMS, Heterogeneous Integration in SiP, Thermo-mechanical stress, Power dissipation issues, Wafer warpage, Wire bonding, Wafer bonding technology, chip-package interaction, yield & reliability.

Abstract Submission
15 Nov 2022 – ~~31 Jan 2023~~
Extended 15 February 2023

Notification of Abstract Acceptance
~~01 March 2023~~
Extended 15 March 2023

Submission format: Extended abstract (**minimum of 2** pages to a **maximum of 6** pages including text and figures) of your original research work. Details on abstract submission, template and other information are available at ***https://www.ipfa-ieee.org/2023/***.

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