Issues and Solutions for Advanced CMOS Circuits

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Summary

Though advanced scaled CMOS technologies have attractive features in speed, power and density, they have also difficulties in circuit design, such as PVT variations, aging and soft errors. These effects are not always possible to be taken into account in the conventional circuits based on the synchronous model. These effects often result in intermittent errors as delay faults, and sometimes fatal faults in circuit operations. Addition to the variation and aging problems, analog circuits are also facing difficulties caused by the low voltage operation in the scaled CMOS circuits. The dynamic range degradation is a typical example. Also, the power supply noise is a common issue both for digital and analog circuits.

In this lecture, first, issues in design of advanced CMOS circuits are reviewed. For mitigating these issues in digital circuits, an evolutional view of synchronization method will be introduced. Namely, full-synchronous, pseudo-synchronous and self-synchronous circuits will be presented, including results of our research group for the self-synchronous circuits. For analog circuits, a new paradigm called time-domain will be introduced. After theoretical and numerical comparison of the conventional voltage-domain and the new time-domain, typical examples of basic elements in the time-domain will be presented, such as time-difference-amplifiers and time-to-digital converters, along with applications for PLL and CDR. Finally, research results in the power supply noise issue will be presented quickly.

Keywords-PVT variation, aging, synchronous system,self-synchronous system, self-synchronous FPGA, dynamic range,voltage domain circuit,time-domain circuit, time diffrenceamplifier, time-to-digital-converter, soft-thermometer code, PW-PLL, CDR, power integrity

Kunihiro Asada received the B. S., M. S., and Ph.D. from University of Tokyo in 1975, 1977, and 1980, respectively. In 1980 he joined the Faculty of Engineering, University of Tokyo. From 1985 to 1986 he stayed at Edinburgh University as a visiting scholar. From 1990 to 1992 he served as the Editor of IEICE Transactions on Electronics. In 1996 he established VDEC in University of Tokyo. He served as the Chair of IEEE/SSCS Japan Chapter in 2001-2002 and the Chair of IEEE Japan Chapter Operation Committee in 2007-2008. He is currently professor, director of VDEC. His research interest is design and evaluation of integrated systems and component devices. He is a member of IEEE, IEICE and IEEJ.