Spring 2016 Tech Seminar Series

#1 Designing PCB’s
For First Version Working Assemblies

Series Presenters: Jim Groves & Mike Joyner

Presentation Sponsored By:
Ithaca IEEE Chapter & Cornell IEEE Chapter

Phillips Hall RM#213 Tuesday, Feb. 23, 5:30pm - 7:00pm
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Series Presenters:

Jim Groves
IC Design Manager at Kionix, Inc.
Linkedin page: https://www.linkedin.com/in/jim-groves-a51811a

Mike Joyner
President/CEO at Town Line Technologies, LLC
Linkedin page: https://www.linkedin.com/in/mike-joyner-90026815
You can have Rev A working boards all the time

- Not a myth
- Mitigate cost impacts, schedule delays.
- Avoid undesired conversations with investors/management
- DFM
- DFT
- Six Sigma Quality, not just a slogan
• **From napkin to schematic to PCB’s**
  
  – Hand Drawn > Manual Layout
  
  – CAD (Mechanical) Schematic > Layout?
    
    - Connectivity?
    - Library Parts?
    - ECO?
  
  – CAE Schematic > Layout
    
    - Netlists, Libraries, ECO capabilities
    - Compare, constraint rules
Expensive fuse testers and table coasters
  – Manual vs Compare/Crosschecking
  – Part Foot Prints
  – Mechanical missteps
  – 3D collisions
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• CAD/CAE Tools
  – KiCad
  – Dip Trace
  – Circuit Maker
  – CS Eagle
  – Altium
  – Mentor Pads
  – Mentor Expedition
  – Orcad
  – Zuken
  – Cadence Allegro
• Freeware can be very expensive
  – Not a criticism, complex software distributed freely
  – Limited CAE capabilities
  – Limited rule checking capabilities
  – In some cases unable to handle large complex parts
• **#Net Lists matter**
  - Learn the characteristics of your tool flow
  - Due diligence before accepting exceptions
  - Manually confirm any and all exceptions
  - Multiple GND’s, sometimes a workaround
• **Board fab vs 3d mechanical milling**
  - Feature size/space
  - Through hole types
  - Solder masks
  - Concept to pcb in hand
Spend time on tape outs. Check gerbers independently

- Independent Gerber viewing editing tool is a must.
- GC-Prevue & Cam350 are a couple of examples
- Print to PDF driver
- Viewing in tool plots
• Assume nothing, Always check standards
  – Standard JEDEC footprints anything but.
  – Noting exceptions for parts you have history with, always confirm against manufacture data sheets
  – IPC.org
  – Confirm capabilities of board fab, and especially assembly
  – Double check critical nets for power not just speed
  – Saturn PCB Toolkit is a great freeware tool for calculations
• Use Data Sheets, standard packages are anything but.
  – SOT, SO8 are common examples
  – Build Part Foot Prints with a capable library tool
  – PCB Library Expert is a good tool example
- **Vias may or may not be your friend**
  - Placement is everything
  - Preplan fan outs for minimal layer changes
  - FPGA’s allow for robust pin swapping
  - Blind vias, buried vias, via-in-pad ups your board cost substantially
  - Setup vias with a low priority with auto routers
  - If using an auto router you can go back and clean up/remove a substantial number of unneeded or redundant vias.
2 layer vs 4 layer vs N# layers

- Determine signal integrity/speed issues before costs
- Design for return path first
- No mention of single layer?
- 2 layer vs 4 layer
- Work with board fab on material type/stackups
• Get out of jail cards
  – Test points
  – Jumpers
  – Multiple package types
  – Spare parts, logic, small FPGA
  – Design in redundant circuitry/power margin/glue logic
  – Optimize during productization, goal is for first off working prototype
Vendor Examples