Space FPGA Mitigation Effects, Challenges and Trends

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Space provides a challenge environment for FPGAs. Some space-grade FPGAs have been hardened-by-process. They are fabricated using a CMOS silicon-o- -insulator process, or use an epitaxial layer to protect against radiation-induced latch-up. FPGAs allows partial read back and configuration .It facilitates efficient repair of configuration memory. Bit-flipping is done in the memory elements, the configuration logic itself is vulnerable to radiation not just the data is the common fault caused by radiation.

Radiation Environment

Radiation environment comprises of beam interactions, residual gas interactions and Beam losses.Single Event Effects are produced by heavy ion striking a transistor and creating charge along its path. In the Single Event Upset (SEU), State change, due to the charges collected by the circuit sensitive node, if higher than the critical charge. For each device there is a critical LET.But in the Single Event Functional Interrupt (SEFI), Special SEU, which affects one specific part of the device and causes the malfunctioning of the whole device. In Single Event Latch-up, Parasitic PNPN structure gets triggered, and creates short between power lines and in Single Event Gate Rupture (SEGR), destruction of the gate oxide in the presence of a high electric field during radiation.

Figure 1. Environment

Single Event Effect induced upsets

Single Event Effect induced upsets in the Xilinx SRAM based FPGAs can be divided into three categories such as configuration upsets, functional upsets in user logic, and architectural upset. Configuration upsets occurs in the configuration memory and can be detected by read back of the programmed configuration memory. There are normally more than a million configuration bits stored and the cross-section per bit for heavy ions and protons is low. For SEU detection, the readback function is an efficient means. Particle penetrates the susceptible portion of a configuration memory cell .It alters its state, a readback and verification of the configuration data will detect the upset. To perform verification, the configuration data is readback from the device and compared to the configuration memory bitstream. Programmable nature of the FPGA presents a new sensitivity due to the configuration memory bitstream. As the bitstream is downloaded to the device, the functionality is determined. The changing of this data which changes the design's function. The user logic which contains elements those are not directly testable for upset through the configuration memory bit stream. The elements are block memory, logic-block flip-flops and I/O flip-flops. Observability is limited unless the user design can capture an event. Architectural upsets occur in the control elements of the FPGA SEUs in these elements are often only detectable indirectly by observing an upset signature and associating it with a control element function. This type of upset is also referenced as Single Event Functional Interrupts.Half-latch which generate many of the constant "0" and "1" values used by Xilinx designs, are susceptible to SEUs. During upset, the output values of these circuits will remain inverted until the device is fully reprogrammed. They are used across the device to drive constants. Partial configuration cannot restore the original state. Latch can recover due to the leakage of the pull-up transistor, after several seconds. Mitigation requires the removal of the half-latches. Full configuration can refresh everything. SET mitigation is achieved due to increased area and power consumption of the final circuit implementation. For the latest, deep-submicron FPGAs, although CMOS scaling has helped to overcome these disadvantages, increased logic density and lower operating voltages have reduced the critical charge necessary to generate an SET. Hardening-by-process provide SET mitigation by limiting the amount of charge that can be collected at sensitive logic nodes preventing the formation of pulses. SET filter uses a chain of inverters.It is used to

delay the signal along one path and a guard-gate to pass only those transients with widths exceeding the delay. The designer has to balance electrical performance with radiation hardness: the wider the pulse, the lower the maximum frequency of operation.

Typical Work flow

We needs to make sure that we understand the requirements and the Simulation of the environment is essential. We try to select the components/technologies and pay attention to the requirements, test the components and find some information about the selected components. We needs to try to assess the risk.SEU may not be critical, or it can be catastrophic.

- Environment simulation
- Component testing
- Mitigation
- Verification

Selection of Space grade FPGA

There are sufficient logic resources to meet the mission's processing needs, unit cost, legacy of use, the suitability of the package, its size and pin pitch, ease of assembly onto a PCB and the qualification of the mounting to withstand shock and vibration, prototyping options, the number of supply rails, the design of the power-distribution architecture, the number and type of I/O and the configuration architecture. .

Challenges for FPGA in Space

Space FPGAs need to be able to deal with the aspects of harsh environment conditions. These devices must survive the high mechanical and acoustic vibration during the rocket launch, and withstand high temperature ranges due to the vacuum in space, in which industry or military temperature grade devices, using appropriate packaging technology, are able to work safely.There are multiple parameters that determine what makes one group of techniques more or less suitable in each case.

- We need to define the radiation environment that can affect your IC.
- We needs to define the reliability targets
- We needs to identify the candidate IC technologies or existing parts and collect data on their sensitivity to TID and SEE.
- We need to identify and quantify all the effects of mitigation techniques which can be introduced at the various levels.
- We need to choose the best compromise of mitigation that allows meeting the reliability targets while also respecting the rest of the requirements. In doing this, the expected levels of final fault tolerance are estimated by analysis.
- Once implemented, validate the selected approach by fault-injection and/or radiation testing.

Three rad-hard device families are NG-MEDIUM, NG-LARGE, and NG-ULTRA, with increasing fabric size and number of logic resources. A combination of radiation hardening by process, layout, architecture (EDAC), and circuit design , together with a background scrubber to preserve the integrity of the internal configuration, are used to provide a rad-hard fabric.

Challenges of Mitigation

SEU mitigation has become more challenging as increased logic densities require less overall charge to disrupt sensitive locations. Some space-grade FPGAs have been hardened-by-process, fabricated using a CMOS silicon-o- -insulator process, or use an epitaxial layer to protect against radiation-induced latch-up. There are mitigation techniques such as SM encoding, memory protection, reconfiguration, TRM etc.Flash-based FPGAs are non-volatile devices. They can be re-programmed in-orbit..

An SET is the voltage pulse resulting from the charge deposited by an ionizing particle passing through a sensitive area of a circuit. Each SET has an unique shape, polarity, amplitude and duration which is dependent on the location and energy of the impact, device biasing and output loading conditions. SETs can propagate in the asynchronous, combinatorial logic .They are found within FPGAs and subsequently be clocked by a flip-flop becoming an SEU.Logical masking occurs when an SET generated by a particle is not propagated to an output due the logic value on the input of a gate. Electrical masking occurs when an SET is attenuated because of the capacitive loading as it propagates along the signal path until it is no longer able to affect the output of a circuit .Temporal masking occurs if an SET reaches a memory element at an instant other than the triggering window's setup and hold requirements. Hardware redundancy duplicates or triplicates the combinational and/or sequential logic with the final output being a final decision.

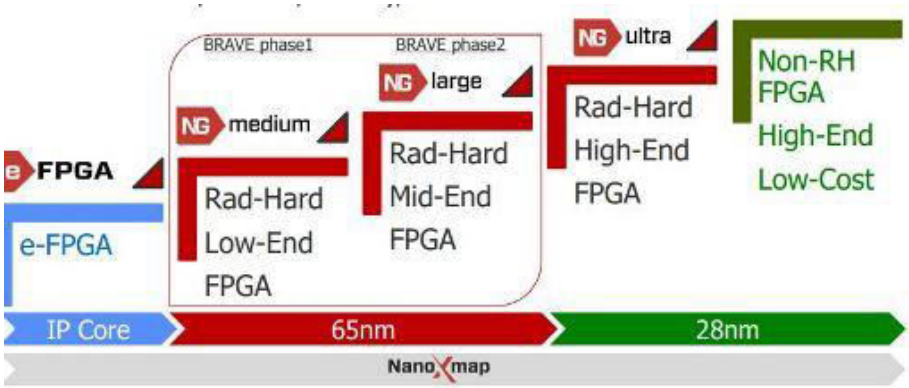

Figure 2. From eFPGA to BRAVE & beyond

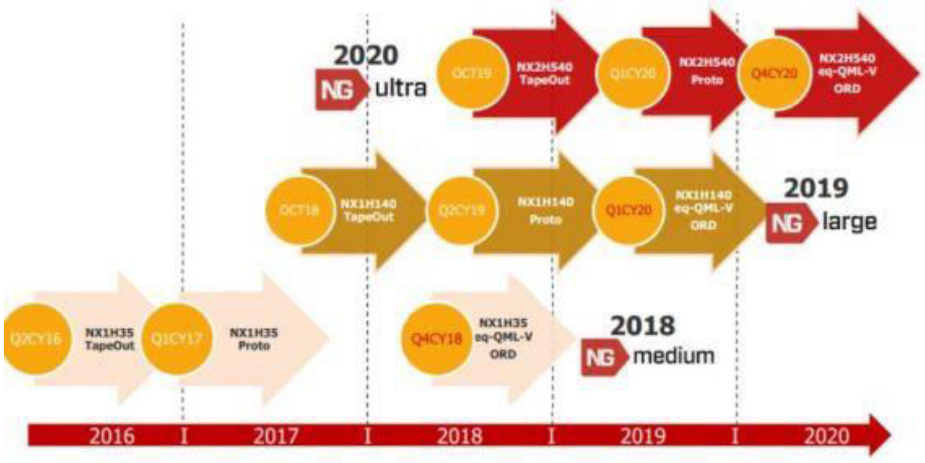

Figure 3-1. FPGA Schedule

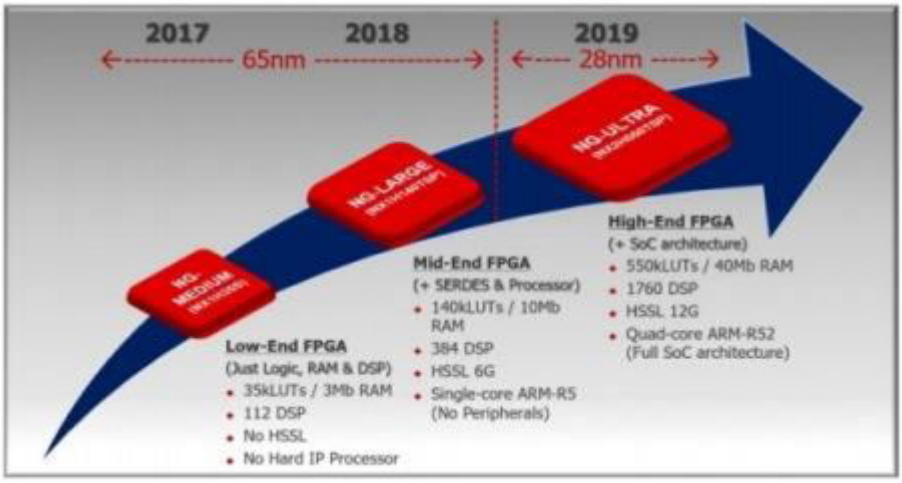

Figure 3-2. FPGA Schedule

About the author

Mr. V. P. Sampath works as a consultant that develops hardware/software co-design tools. Among his publications are technical articles and papers on FPGA and Embedded systems and methods as well as textbooks. He is an active Senior Member of IEEE and Member of Institution of Engineers. He is a mentor for the semiconductor industries. He has a passion to build India as a super power. He is currently a patron for Semiconductor Federation of India.