



**IEEE GREECE CASS/SSCS  
JOINT CHAPTER**

## **Invited Lecture**

The IEEE Greece CAS/SSC joint Chapter, in the frame of the IEEE Circuits and System Society **Distinguished Lecturer Program**, is inviting you in the lecture of:

**Dr. Vivek De\***

Intel Fellow, Director of Circuit Technology Research, Intel Labs,  
Hillsboro, Oregon, USA

**entitled:**

**“Variation-Tolerant & Error-Resilient Many-Core SoCs  
with Fine-Grain Power Management”**

The lecture will be given on **Thursday, Oct. 1, 2020, at 12:00,**  
**in the Amphitheater III of KEDEA, Aristotle University of Thessaloniki.**

**(There will be live webcasting and recording of the event)**

**Information:** Prof. Alkis Hatzopoulos, tel. +302310-996305, 2310-996221, [alkis@ece.auth.gr](mailto:alkis@ece.auth.gr)

*\*Abstract and lecturer's short bio are following.*

# Variation-Tolerant & Error-Resilient Many-Core SoCs with Fine-Grain Power Management

By

**Dr. Vivek De**

Intel Fellow, Director of Circuit Technology Research, Intel Labs,  
Hillsboro, Oregon, USA

## **Abstract:**

Many-core system-on-chip (SoC) architecture & design challenges & opportunities spanning edge devices to cloud computing systems in scaled CMOS process are presented. Key techniques for robust and variation-tolerant logic, embedded memory arrays and on-die interconnect fabrics are discussed. Fine-grain multi-voltage design and power management techniques, featuring integrated voltage regulators for wide dynamic voltage-frequency operating range and flexible platform power control across multi-threaded high-throughput near-threshold voltage (NTV) to single-threaded burst performance modes, are elucidated. Smart variation-aware workload mapping, runtime self-adaptation and error detection & recovery schemes to mitigate impacts of process-voltage-temperature (PVT) variations & aging, and achieve maximum performance under stringent thermal and energy constraints, are presented. Latest advances in design and process/package for realization of monolithic & heterogeneous 2D/3D-integrated compact, efficient, low supply noise, fine-grain, high-bandwidth & fast response power converters & voltage regulators, essential for implementing intelligent system-level power management and adaptation schemes across hardware and software, are also highlighted. Real SoC examples are used to demonstrate leading-edge practical systems.

## **Bio:**

Vivek De is an Intel Fellow and Director of Circuit Technology Research in Intel Labs. He is responsible for providing strategic technical directions for long term research in future circuit technologies and leading energy efficiency research across the hardware stack. He has 300 publications in refereed international conferences and journals with a citation H-index of 79, and 227 patents issued with 32 more patents filed (pending). He received an Intel Achievement Award for his contributions to an integrated voltage regulator technology. He is the recipient of the 2019 IEEE Circuits and System Society (CASS) Charles A. Desoer Technical Achievement Award for “pioneering contributions to leading-edge performance and energy-efficient microprocessors & many-core system-on-chip (SoC) designs” and the 2020 IEEE Solid-State Circuits Society (SSCS) Industry Impact Award for “seminal impact and distinctive contributions to the field of solid-state circuits and the integrated circuits industry”. He received the 2017 Distinguished Alumnus Award from the Indian Institute of Technology (IIT) Madras. He received a B.Tech from IIT Madras, India, a MS from Duke University, Durham, North Carolina, and a PhD from Rensselaer Polytechnic Institute, Troy, New York, all in Electrical Engineering. He is a Fellow of the IEEE.