



**IEEE GREECE CASS/SSCS  
JOINT CHAPTER**

## **Invited Lecture**

The IEEE Greece CAS/SSC joint Chapter, in the frame of the IEEE Circuits and System Society **Distinguished Lecturer Program**, is inviting you in the lecture of:

**Prof. Keshab K. Parhi\***

Department of Electrical and Computer Engineering,  
University of Minnesota, Minneapolis, USA

**entitled:**

**“Machine Learning Systems: Low-Energy VLSI Architectures and Applications”**

The lecture will be given at:

**Aristotle University of Thessaloniki  
on Monday, March 9, 2020, at: 12:00,  
in the lecture room 8 of the ECE Department.**

**Information:** Prof. Alkis Hatzopoulos, tel. 2310-996305, 2310-996221, e-mail: [alkis@ece.auth.gr](mailto:alkis@ece.auth.gr)

*(There will be live webcasting and recording of the event  
Link: <https://www.auth.gr/video/27741> )*

\* Abstract and lecturer's short bio are following.

# “Machine Learning Systems: Low-Energy VLSI Architectures and Applications”

by

**Prof. Keshab K. Parhi**

Dept. of Electrical & Computer Engineering

University of Minnesota, Minneapolis

Email: [parhi@umn.edu](mailto:parhi@umn.edu)

<http://www.ece.umn.edu/~parhi>

**Abstract:** Machine learning and data analytics continue to expand the fourth industrial revolution and affect many aspects of our lives. The first part of the talk will explore hardware accelerator architectures for deep learning applications. I will talk about our recent work on Perm-DNN based on permuted-diagonal interconnections in deep convolutional neural networks and how structured sparsity can reduce energy consumption associated with memory access in these systems. I will then talk about reducing latency and memory access in accelerator architectures for training by gradient interleaving using systolic arrays. In the second part of the talk, I will describe machine learning applications in data-driven neuroscience applications and their low-energy implementations. I will talk about use of machine learning to find biomarkers for epilepsy using electroencephalogram (EEG). I will talk about approaches for energy-efficient implementations and about the roles of feature ranking and incremental-precision approaches to reduce energy consumption.

**Bio:** **Keshab K. Parhi** received the B.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur, in 1982, the M.S.E.E. degree from the University of Pennsylvania, Philadelphia, in 1984, and the Ph.D. degree from the University of California, Berkeley, in 1988. He has been with the University of Minnesota, Minneapolis, since 1988, where he is currently Distinguished McKnight University Professor and Edgar F. Johnson Professor of Electronic Communication in the Department of Electrical and Computer Engineering. He has published over 650 papers, is the inventor of 31 patents, and has authored the textbook *VLSI Digital Signal Processing Systems* (Wiley, 1999) and coedited the reference book *Digital Signal Processing for Multimedia Systems* (Marcel Dekker, 1999). His current research addresses VLSI architecture design of machine learning systems, hardware security, data-driven neuroscience and molecular/DNA computing. Dr. Parhi is the recipient of numerous awards including the 2017 Mac Van Valkenburg award and the 2012 Charles A. Desoer Technical Achievement award from the IEEE Circuits and Systems Society, the 2004 F. E. Terman award from the American Society of Engineering Education, the 2003 IEEE Kiyo Tomiyasu Technical Field Award, the 2001 IEEE W. R. G. Baker prize paper award, and a Golden Jubilee medal from the IEEE Circuits and Systems Society in 2000. He served as the Editor-in-Chief of the IEEE Trans. Circuits and Systems, Part-I during 2004 and 2005. He was elected a Fellow of IEEE in 1996 and a Fellow of the American Association for Advancement of Science (AAAS) in 2017.