IEEE GREECE CASS/SSCS
JOINT CHAPTER

Invited Lecture

The IEEE Greece CAS/SSC joint Chapter, in the frame of
the IEEE Circuits and System Society **Distinguished Lecturer Program**,
is inviting you in the lecture of:

Dr. Arindam Basu *

Associate professor at Nanyang Technological University, Singapore

entitled:

"Designing Low-power "Intelligent" Chips in the face of Statistical Variations of Nanoscale Devices: The Neuromorphic Solution"

The lecture will be given on **Thursday, October 19, 2017, at: 12:00,**
in the Amphitheater III of KEDEA, **Aristotle University of Thessaloniki.**

(There will be live webcasting and recording of the event.

Link: *http://www.auth.gr/video/24549*)

Information: Prof. Alkis Hatzopoulos, tel. +302310-996305, 2310-996221, alkis@eng.auth.gr

**Abstract and lecturer's short bio are following.*

Designing Low-power “Intelligent” Chips in the face of Statistical Variations of Nanoscale Devices: The Neuromorphic Solution”

by

Dr. Arindam Basu *

Associate professor at Nanyang Technological University, Singapore

Abstract: As CMOS technology has been scaling down over the last decade, the effect of statistical variations (or component mismatch) and their impact on circuit design have become increasingly prominent. Further, new nanoscale devices like memristors and spin-mode devices like domain wall memories have emerged as possible candidates for neuromorphic computing at energy levels lower than CMOS—however, they also suffer from issues of variability and mismatch. In this talk, I will present some of the work done by our group where we take inspiration from neuroscience and show new approaches to perform machine learning with low energy consumption using low-resolution mismatched components. First, I will talk about “combinatoric learning” using binary or 1-bit synapses—an alternative to weight based learning in neural networks that is inspired by structural plasticity in our brains. Second, I will present an example of utilizing component mismatch to perform part of the computation—an example of algorithm-hardware co-design involving random projection algorithms like Reservoir Computing or Extreme Learning Machine. Lastly, I will show an application of such a low-power machine learner to perform intention decoding in low-power brain-machine interfaces.

Bio: Dr. Arindam Basu received the B.Tech and M.Tech degrees in Electronics and Electrical Communication Engineering from the Indian Institute of Technology, Kharagpur in 2005, the M.S. degree in Mathematics and PhD. degree in Electrical Engineering from the Georgia Institute of Technology, Atlanta in 2009 and 2010 respectively. Dr. Basu received the Prime Minister of India Gold Medal in 2005 from I.I.T Kharagpur (awarded to the top student). In the summer of 2008, he worked at Texas Instruments, Dallas and developed automatic tuning strategies for LNAs designed in 45nm and 65nm. He joined Nanyang Technological University as an Assistant professor in June 2010. He is currently an Associate Editor of IEEE Sensors journal (2015-17) and IEEE Transactions on Biomedical Circuits and Systems (2016-18). He is also Guest Editor of two Special Issues in IEEE Trans. on Biomedical Circuits and Systems for selected papers from ISCAS 2015 and BioCAS 2015 conferences.

Dr. Basu received the best student paper award at Ultrasonics symposium, 2006, best live demonstration at ISCAS 2010 and a finalist position in the best student paper contest at ISCAS 2008. He was awarded MIT Technology Review's inaugural TR35@Singapore award in 2012 for being among the top 12 innovators under the age of 35 in SE Asia, Australia and New Zealand. He is a technical committee member of the IEEE CAS societies of Biomedical Circuits and Systems, Neural Systems and Applications (Secretary Elect) and Sensory Systems. His research interests include bio-inspired neuromorphic circuits, non-linear dynamics in neural systems, low power analog IC design and programmable circuits and devices.